Hitachi semiconductor

MAR. 1992

DATA BOOK

HITACHI IC Memory No.1

SRAM, SRAM Module, PSRAM, AS Memory and ECL RAM

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HITACHI

ADE-403-001H

CONTENTS

Wide Temperature Range Line Up

Hitachi provides wide temperature range devices. The following are their type number, temperature, characteristics.

Type No.	Access time	Temperature range	Characteristics
HM628128PI/LPI-8	80 ns	–40°C to +85°C	I_{CC} = 45 mA, I_{CC1} = 80 mA, I_{CC2} = 40 mA, V_{IH} = 2.4 V, V_{IL} = 0.6 V (Topr, Tbias, –40 to +85°C)
HM628128PI/LPI-10	100 ns		
HM628128PI/LPI-12	120 ns		
HM628128FPI/LFPI-8	80 ns		
HM628128FPI/LFPI-10	100 ns		
HM628128FPI/LFPI-12	120 ns		
HM62256API/LPI-10	100 ns	–40°C to +85°C	I_{CC} = 20 mA, V_{IH} = 2.4 V, V_{IL} = 0.6 V I_{CC2} = 15 mA, t_{WR} = 15 ns I_{SDI} = 200 µA (Only L-versions) I_{CCDR} = 100 µA (Only L-versions)
HM62256API/LPI-12	120 ns		
HM62256API/LPI-15	150 ns		
HM62256AFPI/LFPI-10T	100 ns		
HM62256AFPI/LFPI-12T	120 ns		
HM62256AFPI/LFPI-15T	150 ns		
HN58C65PJ-25	250 ns	–40°C to +85°C	V_{CC} = 5 V ± 10%, t_{DH} = 30 ns
HN58C65FPI-25	250 ns		
HN58C256FPI-20	200 ns		V_{CC} = 5 V ± 10%
HN27C256HGJ-85	85 ns		V_{CC} = 5 V ± 5%
HN27C256HGJ-10	100 ns		
HN27C1024HGJ-10	100 ns		V_{CC} = 5 V ± 10%, V_{IH} = 2.4 V, V_{IL} = 0.45 V
HN27C101AGI-12	120 ns		V_{IH} = 2.4 V
HN27C101AGI-15	150 ns		
HN27C101AGI-23	230 ns		
HN27C301AGI-12	120 ns		
HN27C301AGI-15	150 ns		
HN27C301AGI-23	230 ns		
HN27C4096GI-12	120 ns		V_{IH} = 2.4 V, V_{IL} = 0.45 V
HN27C4096GI-15	150 ns		

	80 ns	100 ns	120 ns
t_{WR1}	10 ns	10 ns	15 ns
t_{WR2}	15 ns	15 ns	15 ns
t_R	50 ns*		

* V_{CC} rising time less than 50 ns. When V_{CC} rising time is less 50 ns, t_R must be 50 ns or more.

Type No.	Access time	Temperature range	Characteristics
HN27C4096CCI-12	120 ns	–40°C to +85°C	V_{IH} = 2.4 V, V_{IL} = 0.45 V
HN27C4096CCI-15	150 ns		
HN27C4096CPI-12	120 ns		
HN27C4096CPI-15	150 ns		
HN27C4001GI-12	120 ns		
HN27C4001GI-15	150 ns		
HN623257	150 ns	–40°C to +85°C	V_{IH} = 2.4 V, V_{IL} = 0.6 V
HN623258	200 ns		
HN62321	150 ns		
HN62321B	200 ns		
HN62321E	200 ns		
HN62321A	150 ns		
HN62321G	150 ns		
HN62302B	200 ns		
HN62412	200 ns		
HN62442B	100 ns		V_{IH} = 2.4 V, V_{IL} = 0.45 V
HN62334B	150 ns		V_{IH} = 2.4 V, V_{IL} = 0.6 V
HN62314B	200 ns		
HN62434	150 ns		
HN62414	200 ns		
HN62444	100 ns		V_{IH} = 2.4 V, V_{IL} = 0.45 V
HN62444B	120 ns		
HN62318B	150 ns		V_{IH} = 2.4 V, V_{IL} = 0.6 V
HN62328B	200 ns		
HN62418	150 ns		
HN62428	200 ns		
HN624116	200 ns		

Refer to Hitachi IC Memory Data Book No.2 regarding EEPROM, Flash Memory, EPROM, OTPROM, and Mask ROM and Hitachi IC Memory Data Book No. 3 regarding DRAM and DRAM Module.

Quick Reference Guide to Hitachi IC Memories

MOS RAM

Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Static	16 k-bit	HM6716-25	Bi-CMOS (with $\overline{OE}$)		25	25	24							●					
		HM6716-30			30	30								●					
		HM6268-25	CMOS	4096×4	25	25	20	●											
		HM6268-35			35	35		●											
		HM6268-45			45	45		●											
		HM6268L-25			25	25		●											
		HM6268L-35			35	35		●											
		HM6268L-45			45	45		●											
		HM6267-35		16384×1	35	35		●											
		HM6267-45			45	45		●											
		HM6267-55			55	55		●											
		HM6267L-35			35	35		●											
		HM6267L-45			45	45		●											
		HM6267L-55			55	55		●											
	18 k-bit	HM6719-25	Bi-CMOS	2048×9	25	25	24							●					
		HM6719-30			30	30								●					
	64 k-bit	HM6264A-10	CMOS	8192×8	100	100	28	●	●					●					
		HM6264A-12			120	120		●	●					●					
		HM6264A-15			150	150		●	●					●					
		HM6264AL-10			100	100		●	●					●					
		HM6264AL-12			120	120		●	●					●					
		HM6264AL-15			150	150		●	●					●					
		HM6264AL-10L			100	100		●	●					●					
		HM6264AL-12L			120	120		●	●					●					
		HM6264AL-15L			150	150		●	●					●					

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Static	64 k-bit	HM6289-25	CMOS	16384×4	25	25	24											●	
		HM6289-35			35	35												●	
		HM6289L-25			25	25												●	
		HM6289L-35			35	35												●	
		HM6789HA-12	Bi-CMOS	16384×4 (with OE)	12	12								●				●	
		HM6789HA-15			15	15								●				●	
		HM6288-25	CMOS	16384×4	25	25	22,24 (SOJ)	●										●	
		HM6288-35			35	35		●										●	
		HM6288L-25			25	25		●										●	
		HM6288L-35			35	35		●										●	
		HM6788HA-12	Bi-CMOS		12	12	22							●					
		HM6788HA-15			15	15								●					
		HM6287-45	CMOS	65536×1	45	45	22,24 (SOJ)	●											
		HM6287-55			55	55		●											
		HM6287-70			70	70		●											
		HM6287L-45			45	45		●											
		HM6287L-55			55	55		●											
		HM6287L-70			70	70		●											
		HM6287H-25			25	25		●										●	
		HM6287H-35			35	35		●										●	
		HM6287HL-25			25	25		●										●	
		HM6287HL-35			35	35		●										●	
		HM6787HA-12	Bi-CMOS		12	12	22,24							●				●	
		HM6787HA-15			15	15								●				●	
	256 k-bit	HM62256-8	CMOS	32768×8	85	85	28	●	●										
		HM62256-10			100	100		●	●										

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Static	256 k-bit	HM62256-12	CMOS	32768×8	120	120	28	●	●										
		HM62256-15			150	150		●	●										
		HM62256L-8			85	85		●	●										
		HM62256L-10			100	100		●	●										
		HM62256L-12			120	120		●	●										
		HM62256L-15			150	150		●	●										
		HM62256L-10SL			100	100		●	●										
		HM62256L-12SL			120	120		●	●										
		HM62256L-15SL			150	150		●	●										
		HM62256A-8			85	85	28,32	●	●					●					
		HM62256A-10			100	100		●	●					●					
		HM62256A-12			120	120		●	●					●					
		HM62256A-15			150	150		●	●					●					
		HM62256AL-8			85	85		●	●	●	●			●					
		HM62256AL-10			100	100		●	●	●	●			●					
		HM62256AL-12			120	120		●	●	●	●			●					
		HM62256AL-15			150	150		●	●	●	●			●					
		HM62256AL-8SL			85	85		●	●	●	●			●					
		HM62256AL-10SL			100	100		●	●	●	●			●					
		HM62256AL-12SL			120	120		●	●	●	●			●					
		HM62256AL-15SL			150	150		●	●	●	●			●					
		HM62832H-25			25	25	28	●										●	
		HM62832H-35			35	35		●										●	
		HM62832H-45			45	45		●										●	
		HM62832HL-25			25	25		●										●	
		HM62832HL-35			35	35		●										●	
		HM62832HL-45			45	45		●										●	

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Static	256 k-bit	HM62832UH-15*3	CMOS	32768×8	15	15	28	●										●	
		HM62832UH-20*3			20	20		●										●	
		HM62832UHL-15*3			15	15		●										●	
		HM62832UHL-20*3			20	20		●										●	
		HM67832SH-10*4	Bi-CMOS		10	10												●	
		HM67832SH-12*4			12	12												●	
		HM6709A-15		65536×4	15	15												●	
		HM6709A-20			20	20												●	
		HM6709A-25			25	25												●	
		HM6208H-25	CMOS		25	25	24	●										●	
		HM6208H-35			35	35		●										●	
		HM6208H-45			45	45		●										●	
		HM6208HL-25			25	25		●										●	
		HM6208HL-35			35	35		●										●	
		HM6208HL-45			45	45		●										●	
		HM6708SH-10*4	Bi-CMOS		10	10												●	
		HM6708SH-12*4			12	12												●	
		HM6209SH-10*4		65536×4 (with OE)	10	10	28											●	
		HM6209SH-12*4			12	12												●	
		HM6708A-15	Bi-CMOS	65536×4	15	15	24	●										●	
		HM6708A-20			20	20		●										●	
		HM6207H-25	CMOS	262144×1	25	25		●										●	
		HM6207H-35			35	35		●										●	
		HM6207H-45			45	45		●										●	
		HM6207HL-25			25	25		●										●	
		HM6207HL-35			35	35		●										●	
		HM6207HL-45			45	45		●										●	

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Static	256 k-bit	HM6707A-15	Bi-CMOS	262144×1	15	15	24											●	
		HM6707A-20			20	20												●	
	1 M-bit	HM628128-7	CMOS	131072×8	70	70	32	●	●	●	●								
		HM628128-8			85	85		●	●	●	●								
		HM628128-10			100	100		●	●	●	●								
		HM628128-12			120	120		●	●	●	●								
		HM628128L-7			70	70		●	●	●	●								
		HM628128L-8			85	85		●	●	●	●								
		HM628128L-10			100	100		●	●	●	●								
		HM628128L-12			120	120		●	●	●	●								
		HM628128L-7SL			70	70		●	●	●	●								
		HM628128L-8SL			85	85		●	●	●	●								
		HM628128L-10SL			100	100		●	●	●	●								
		HM628128L-12SL			120	120		●	●	●	●								
		HM628128L-7L			70	70				●	●								
		HM628128L-8L			85	85				●	●								
		HM628128L-10L			100	100				●	●								
		HM628128L-12L			120	120				●	●								
		HM624256-35		262144×4	35	35	28	●										●	
		HM624256-45			45	45		●										●	
		HM624256L-35			35	35		●										●	
		HM624256L-45			45	45		●										●	
		HM624256A-20			20	20		●										●	
		HM624256A-25			25	25		●										●	
		HM624256A-35			35	35		●										●	
		HM624256AL-20			20	20		●										●	
		HM624256AL-25			25	25		●										●	

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Static	1 M-bit	HM624256AL-35	CMOS	262144×4	35	35	28	●										●	
		HM624257-35			35	35	32											●	
		HM624257-45			45	45												●	
		HM624257L-35			35	35												●	
		HM624257L-45			45	45												●	
		HM624257A-20*3			20	20												●	
		HM624257A-25*3			25	25												●	
		HM624257A-35*3			35	35												●	
		HM624257AL-20*3			20	20												●	
		HM624257AL-25*3			25	25												●	
		HM624257AL-35*3			35	35												●	
		HM621100A-20		1048576×1	20	20	28	●										●	
		HM621100A-25			25	25		●										●	
		HM621100A-35			35	35		●										●	
		HM621100AL-20			20	20		●										●	
		HM621100AL-25			25	25		●										●	
		HM621100AL-35			35	35		●										●	
		HM628128A-5		131072×8	55	55	32	●		●	●							●	
		HM628128A-7			70	70		●		●	●							●	
		HM628128A-8			85	85		●		●	●							●	
		HM628128A-10			100	100		●		●	●							●	
		HM628128AL-5			55	55		●		●	●							●	
		HM628128AL-7			70	70		●		●	●							●	
		HM628128AL-8			85	85		●		●	●							●	
		HM628128AL-10			100	100		●		●	●							●	
		HM628128AL-5SL			55	55		●		●	●							●	
		HM628128AL-7SL			70	70		●		●	●							●	

(cont)

Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Static	1 M-bit	HM628128AL-8SL	CMOS	131072×8	85	85	32	●		●	●							●	
		HM628128AL-10SL			100	100		●		●	●							●	
		HM629128-5		131072×9	55	55		●		●	●							●	
		HM629128-7			70	70		◒		◒	◒							◒	
		HM629128-8			85	85		●		●	●							●	
		HM629128-10			100	100		●		●	●							●	
		HM629128L-5			55	55		●		●	●							●	
		HM629128L-7			70	70		●		●	●							●	
		HM629128L-8			85	85		●		●	●							●	
		HM629128L-10			100	100		●		●	●							●	
		HM629128L-5SL			55	55		●		●	●							●	
		HM629128L-7SL			70	70		●		●	●							●	
		HM629128L-8SL			85	85		●		●	●							●	
		HM629128L-10SL			100	100		●		●	●							●	
		HM62V8128-15		131072×8	150	150		●		●	●							●	
		HM62V8128L-15			150	150		●		●	●							●	
		HM62V8128L-15SL			150	150		●		●	●							●	
	4 M-bit	HM628512-5		524288×8	55	55		●	●										
		HM628512-7			70	70		●	●										
		HM628512-8			85	85		●	●										
		HM628512-10			100	100		●	●										
		HM628512L-5			55	55		●	●			●	●						
		HM628512L-7			70	70		●	●			●	●						
		HM628512L-8			85	85		●	●			●	●						
		HM628512L-10			100	100		●	●			●	●						
		HM628512L-5SL			55	55		●	●			●	●						
		HM628512L-7SL			70	70		●	●			●	●						

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Static	4 M-bit	HM628512L-8SL	CMOS	524288×8	85	85	32	●	●			●	●						
		HM628512L-10SL			100	100		●	●			●	●						
		HM621400-25		4194304×1	25	25						●						●	
		HM621400-30			30	30						●						●	
		HM621400-35			35	35						●						●	
		HM621400-45			45	45						●						●	
		HM621400L-30			30	30						●						●	
		HM621400L-35			35	35						●						●	
		HM621400L-45			45	45						●						●	
		HM624100-25		1048576×4	25	25						●						●	
		HM624100-30			30	30						●						●	
		HM624100-35			35	35						●						●	
		HM624100-45			45	45						●						●	
		HM624100L-30			30	30						●						●	
		HM624100L-35			35	35						●						●	
		HM624100L-45			45	45						●						●	
Static RAM module	256 k-bit	HB66B1616A-25		16384×16	25	25	36												●
		HB66B1616A-35			35	35													●
	1 M-bit	HM66203-10		131072×8	100	100	32												●
		HM66203-12			120	120													●
		HM66203-15			150	150													●
		HM66203L-10			100	100													●
		HM66203L-12			120	120													●

(cont)

Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Static RAM module	1 M-bit	HM66203L-15	CMOS	131072×8	150	150	32												●
		HM66204-12		131072×8 (with decoder)	120	120													●
		HM66204-15			150	150													●
		HM66204L-12			120	120													●
		HM66204L-15			150	150													●
	2 M-bit	HB66A2568A-25		262144×8	25	25	60												●
		HB66A2568A-35			35	35													●
	4 M-bit	HM66205L-85		524288×8	85	85	32												●
		HM66205L-10			100	100													●
		HM66205L-12			120	120													●
Pseudo static	256 k-bit	HM65256B-10		32768×8	100	160	28	●	●					●					
		HM65256B-12			120	190		●	●					●					
		HM65256B-15			150	235		●	●					●					
		HM65256B-20			200	310		●	●					●					
		HM65256BL-10			100	160		●	●					●					
		HM65256BL-12			120	190		●	●					●					
		HM65256BL-15			150	235		●	●					●					
	1 M-bit	HM65256BL-20		131072×8	200	310	32	●	●		●								
		HM658128AD-8			80	130		●	●	●	●								
		HM658128AD-10			100	169		●	●	●	●								
		HM658128AD-12			120	190		●	●	●	●								
		HM658128AL-8			80	130		●	●	●	●								
		HM658128AL-10			100	160		●	●	●	●								
		HM658128AL-12			120	190		●	●	●	●								
		HM658128AL-8L			80	130		●	●	●	●								
		HM658128AL-10L			100	160		●	●	●	●								
		HM658128AL-12L			120	190		●	●	●	●								

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Pseudo static	4 M-bit	HM658512L-8	CMOS	524288×8	80	130	32	●	●			●	●						
		HM658512L-10			100	160		●	●			●	●						
		HM658512L-12			120	190		●	●			●	●						
		HM658512L-8L			80	130		●	●			●	●						
		HM658512L-10L			100	160		●	●			●	●						
		HM658512L-12L			120	190		●	●			●	●						
		HM658512D-8			80	130		●	●			●	●						
		HM658512D-10			100	160		●	●			●	●						
		HM658512D-12			120	190		●	●			●	●						
		HM65V8512-12			120	190		●		●	●								
		HM65V8512-15			150	230		●		●	●								
		HM65V8512L-12			120	190		●		●	●								
		HM65V8512L-15			150	230		●		●	●								
		HM65V8512L-12L			120	190		●		●	●								
		HM65V8512L-15L			150	230		●		●	●								
Application specific memory	16 k-bit	HM63021-28		2048×8 Line memory	20	28	28	●	●										
		HM63021-34			25	34		●	●										
		HM63021-45			30	45		●	●										
	256 k-bit	HM53461-10		65536×4 Multiport	100	190	24	●							●			●	
		HM53461-12			120	220		●							●			●	
		HM53461-15			150	260		●							●			●	
		HM53462-10			100	190		●							●			●	
		HM53462-12			120	220		●							●			●	
		HM53462-15			150	260		●							●			●	
	1 M-bit	HM53051-34		262144×4 Frame memory	30	34	18,28	●	●										
		HM53051-45			35	45		●	●										
		HM53051-60			40	60		●	●										

(cont)

Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Application specific memory	1 M-bit	HM534251-10	CMOS	262144×4 Multiport	100	190	28								●			●	
		HM534251-11			100	190									●			●	
		HM534251-12			120	220									●			●	
		HM534251-15			150	260									●			●	
		HM534252-10			100	190									●			●	
		HM534252-11			100	190									●			●	
		HM534252-12			120	220									●			●	
		HM534252-15			150	260									●			●	
		HM538121-10		131072×8 Multiport	100	190	40											●	
		HM538121-11			100	190												●	
		HM538121-12			120	220												●	
		HM538121-15			150	260												●	
		HM538122-10			100	190												●	
		HM538122-11			100	190												●	
		HM538121-12			120	220												●	
		HM538122-15			150	260												●	
		HM534251A-6		262144×4 Multiport	60	125	28,32			●	●				●			●	
		HM534251A-8			80	150				●	●				●			●	
		HM534251A-10			100	180				◒	◒				◒			◒	
		HM534253A-6			60	125				●	●				●			●	
		HM534253A-8			80	150				●	●				●			●	
		HM534253A-10			100	180				●	●				●			●	
		HM538121A-6			60	125	40											●	
		HM538121A-8			80	150												●	
		HM538121A-10			100	180												●	

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(cont)

Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Application specific memory	1 M-bit	HM538123A-6	CMOS	131072×8 Multiport	60	125	28											●	
		HM538123A-7			70	135												●	
		HM538123A-8			80	150												●	
		HM538123A-10			100	180												●	
	2 M-bit	HM538253-7		262144×8	70	135	40					●	●					●	
		HM538253-8			80	150						●	●					●	
		HM538253-10			100	180						●	●					●	
		HM5316123-7		131072×16	70	135	64											●	
		HM5316123-8			80	150												●	
		HM5316123-10			100	180												●	
	18 k-bit	HM63921-20		2048×9 FIFO	20	30	28	●										●	
		HM63921-25			25	35		●										●	
		HM63921-35			35	45		●										●	
	128 k-bit	HM62A168-25		8192×16 Cashe	25	25	52										●		
		HM62A168-25R			25	25											●		
		HM62A168-35			35	35											●		
		HM62B168-25			25	25											●		
		HM62B168-35			35	35											●		
	144 k-bit	HM62A188-25		8192×18 Cashe	25	25											●		
		HM62A188-25R			25	25											●		
		HM62A188-35			35	35											●		
		HM62B188-25			25	25											●		
		HM62B188-35			35	35											●		
	163 k-bit	HM62A2017-17		8192×20 Cashe	17	17	68										●		
		HM62A2017-20			20	20											●		
		HM62A2017-25			25	25											●		
		HM62A2017-30			30	30											●		

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Application specific memory	288 k-bit	HM67B932-25	Bi-CMOS	32 k×9 Cashe	25	25	44										●		
	320 k-bit	HM62A2016-17	CMOS	16384×20 Cashe	17	17	52										●		
		HM62A2016-20			20	20											●		
		HM62A2016-25			25	25											●		
		HM62A2016-30			30	30											●		
	1 M-bit	HM62A9128-20		131072×9 (8) Cashe	10	20	32											●	
		HM62A8128-20			10	20												●	
Dynamic	1 M-bit	HM514256A-6		262144×4	60	120	20	●		●	●				●			●	
		HM514256A-7			70	130		●		●	●				●			●	
		HM514256A-8			80	160		●		●	●				●			●	
		HM514256A-10			100	190		●		●	●				●			●	
		HM514256A-12			120	220		●		●	●				●			●	
		HM514256AL-6			60	120		●		●	●				●			●	
		HM514256AL-7			70	130		●		●	●				●			●	
		HM514256AL-8			80	160		●		●	●				●			●	
		HM514256AL-10			100	190		●		●	●				●			●	
		HM514256AL-12			120	220		●		●	●				●			●	
		HM514258A-6			60	120		●							●			●	
		HM514258A-7			70	130		●							●			●	
		HM514258A-8			80	160		●							●			●	
		HM514258A-10			100	190		●							●			●	
		HM514258A-12			120	220		●							●			●	
		HM514266A-6			60	120		●		●	●				●			●	
		HM514266A-7			70	130		●		●	●				●			●	
		HM514266A-8			80	160		●		●	●				●			●	
		HM514266A-10			100	190		●		●	●				●			●	
		HM514266A-12			120	220		●		●	●				●			●	

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Dynamic	1 M-bit	HM511000A-6	CMOS	1048576×1	60	120	18,20	●		●	●				●			●	
		HM511000A-7			70	130		●		●	●				●			●	
		HM511000A-8			80	160		●		●	●				●			●	
		HM511000A-10			100	190		●		●	●				●			●	
		HM511000A-12			120	220		●		●	●				●			●	
		HM511000AL-6			60	120		●		●	●				●			●	
		HM511000AL-7			70	130		●		●	●				●			●	
		HM511000AL-8			80	160		●		●	●				●			●	
		HM511000AL-10			100	190		●		●	●				●			●	
		HM511000AL-12			120	220		●		●	●				●			●	
		HM511001A-6			60	145		●							●			●	
		HM511001A-7			70	155		●							●			●	
		HM511001A-8			80	190		●							●			●	
		HM511001A-10			100	210		●							●			●	
		HM511001A-12			120	245		●							●			●	
		HM511002A-6			60	120		●							●			●	
		HM511002A-7			70	130		●							●			●	
		HM511002A-8			80	160		●							●			●	
		HM511002A-10			100	190		●							●			●	
		HM511002A-12			120	220		●							●			●	
		HM574256-35R	Bi-CMOS	262144×4	35	75	28											●	
		HM574256-40			40	85												●	
		HM574256-45			45	90												●	
		HM571000-35R		1048576×1	35	75												●	
		HM571000-40			40	85												●	
		HM571000-45			45	90												●	

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Dynamic	1 M-bit	HM511664-7*3	CMOS	65536×16	70	125	40								●			●	
		HM511664-8			80	135									●			●	
		HM511664-10			100	170									●			●	
		HM511665-7*3			70	125									●			●	
		HM511665-8			80	135									●			●	
		HM511665-10			100	170									●			●	
		HM511664L-7*3			70	125									●			●	
		HM511664L-8			80	135									●			●	
		HM511664L-10			100	170									●			●	
		HM511665L-7*3			70	125									●			●	
		HM511665L-8			80	135									●			●	
		HM511665L-10			100	170									●			●	
		HM511666-7*3			70	125									●			●	
		HM511666-8			80	135									●			●	
		HM511666-10			100	170									●			●	
		HM511666L-7*3			70	125									●			●	
		HM511666L-8			80	135									●			●	
		HM511666L-10			100	170									●			●	
Dynamic	4 M-bit	HM514400A-6		1048576×4	60	110				●	●	●	●		●			●	
		HM514400A-7			70	130				●	●	●	●		●			●	
		HM514400A-8			80	150				●	●	●	●		●			●	
		HM514400A-10			100	180				●	●	●	●		●			●	
		HM514400AL-6			60	110				●	●	●	●		●			●	
		HM514400AL-7			70	130				●	●	●	●		●			●	
		HM514400AL-8			80	150				●	●	●	●		●			●	
		HM514400AL-10			100	180				●	●	●	●		●			●	
		HM514400ASL-6			60	110				●	●	●	●		●			●	

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package: Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Dynamic	4 M-bit	HM514400ASL-7	CMOS	1048576×4	70	130	20			●	●	●	●		●			●	
		HM514400ASL-8			80	150				●	●	●	●		●			●	
		HM514400ASL-10			100	180				●	●	●	●		●			●	
		HM514402A-6			60	110				●	●	●	●		●			●	
		HM514402A-7			70	130				●	●	●	●		●			●	
		HM514402A-8			80	150				●	●	●	●		●			●	
		HM514402A-10			100	180				●	●	●	●		●			●	
		HM514402AL-6			60	110				●	●	●	●		●			●	
		HM514402AL-7			70	130				●	●	●	●		●			●	
		HM514402AL-8			80	150				●	●	●	●		●			●	
		HM514402AL-10			100	180				●	●	●	●		●			●	
		HM514402ASL-6			60	110				●	●	●	●		●			●	
		HM514402ASL-7			70	130				●	●	●	●		●			●	
		HM514402ASL-8			80	150				●	●	●	●		●			●	
		HM514402ASL-10			100	180				●	●	●	●		●			●	
		HM514410A-6			60	110				●	●	●	●		●			●	
		HM514410A-7			70	130				●	●	●	●		●			●	
		HM514410A-8			80	150				●	●	●	●		●			●	
		HM514410A-10			100	180				●	●	●	●		●			●	
		HM514410AL-6			60	110				●	●	●	●		●			●	
		HM514410AL-7			70	130				●	●	●	●		●			●	
		HM514410AL-8			80	150				●	●	●	●		●			●	
		HM514410AL-10			100	180				●	●	●	●		●			●	
		HM514410ASL-6			60	110				●	●	●	●		●			●	
		HM514410ASL-7			70	130				●	●	●	●		●			●	
		HM514410ASL-8			80	150				●	●	●	●		●			●	
		HM514410ASL-10			100	180				●	●	●	●		●			●	

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Dynamic	4 M-bit	HM514412A-6	CMOS	1048576×4	60	110	20			●	●	●	●		●			●	
		HM514412A-7			70	130				●	●	●	●		●			●	
		HM514412A-8			80	150				●	●	●	●		●			●	
		HM514412A-10			100	180				●	●	●	●		●			●	
		HM514412AL-6			60	110				●	●	●	●		●			●	
		HM514412AL-7			70	130				●	●	●	●		●			●	
		HM514412AL-8			80	150				●	●	●	●		●			●	
		HM514412AL-10			100	180				●	●	●	●		●			●	
		HM514412ASL-6			60	110				●	●	●	●		●			●	
		HM514412ASL-7			70	130				●	●	●	●		●			●	
		HM514412ASL-8			80	150				●	●	●	●		●			●	
		HM514412ASL-10			100	180				●	●	●	●		●			●	
		HM514100A-6		4194304×1	60	110				●	●	●	●		●			●	
		HM514100A-7			70	130				●	●	●	●		●			●	
		HM514100A-8			80	150				●	●	●	●		●			●	
		HM514100A-10			100	180				●	●	●	●		●			●	
		HM514100AL-6			60	110				●	●	●	●		●			●	
		HM514100AL-7			70	130				●	●	●	●		●			●	
		HM514100AL-8			80	150				●	●	●	●		●			●	
		HM514100AL-10			100	180				●	●	●	●		●			●	
		HM514100ASL-6			60	110				●	●	●	●		●			●	
		HM514100ASL-7			70	130				●	●	●	●		●			●	
		HM514100ASL-8			80	150				●	●	●	●		●			●	
		HM514100ASL-10			100	180				●	●	●	●		●			●	
		HM514101A-6			60	110				●	●	●	●		●			●	
		HM514101A-7			70	130				●	●	●	●		●			●	
		HM514101A-8			80	150				●	●	●	●		●			●	

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Dynamic	4 M-bit	HM514101A-10	CMOS	4194304×1	100	180	20			●	●	●	●		●			●	
		HM514101AL-6			60	110				●	●	●	●		●			●	
		HM514101AL-7			70	130				●	●	●	●		●			●	
		HM514101AL-8			80	150				●	●	●	●		●			●	
		HM514101AL-10			100	180				●	●	●	●		●			●	
		HM514101ASL-6			60	110				●	●	●	●		●			●	
		HM514101ASL-7			70	130				●	●	●	●		●			●	
		HM514101ASL-8			80	150				●	●	●	●		●			●	
		HM514101ASL-10			100	180				●	●	●	●		●			●	
		HM514102A-6			60	110				●	●	●	●		●			●	
		HM514102A-7			70	130				●	●	●	●		●			●	
		HM514102A-8			80	150				●	●	●	●		●			●	
		HM514102A-10			100	180				●	●	●	●		●			●	
		HM514102AL-6			60	110				●	●	●	●		●			●	
		HM514102AL-7			70	130				●	●	●	●		●			●	
		HM514102AL-8			80	150				●	●	●	●		●			●	
		HM514102AL-10			100	180				●	●	●	●		●			●	
		HM514102ASL-6			60	110				●	●	●	●		●			●	
		HM514102ASL-7			70	130				●	●	●	●		●			●	
		HM514102ASL-8			80	150				●	●	●	●		●			●	
		HM514102ASL-10			100	180				●	●	●	●		●			●	
		HM514800-7		524288×8	70	130	28			●	●				●			●	
		HM514800-8			80	150				●	●				●			●	
		HM514800-10			100	180				●	●				●			●	
		HM514800L-7			70	130				●	●				●			●	
		HM514800L-8			80	150				●	●				●			●	
		HM514800L-10			100	180				●	●				●			●	

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Dynamic	4 M-bit	HM514260-7	CMOS	262144×16	670	130	40			●					●			●	
		HM514260-8			80	150				●					●			●	
		HM514260-10			100	180				●					●			●	
		HM514260L-7			70	130				●					●			●	
		HM514260L-8			80	150				●					●			●	
		HM514260L-10			100	180				●					●			●	
		HM514170-7			70	130									●			●	
		HM514170-8			80	150									●			●	
		HM514170-10			100	180									●			●	
		HM514170L-7			70	130									●			●	
		HM514170L-8			80	150									●			●	
		HM514170L-10			100	180									●			●	
		HM514190-7		262144×18	70	130									●			●	
		HM514190-8			80	150									●			●	
		HM514190-10			100	180									●			●	
		HM514190L-7			70	130									●			●	
		HM514190L-8			80	150									●			●	
		HM514190L-10			100	180									●			●	
	4.5 M-bit	HM514900-7		524288×9	70	130	28			●					●			●	
		HM514900-8			80	150				●					●			●	
		HM514900-10			100	180				●					●			●	
		HM514900L-7			70	130				●					●			●	
		HM514900L-8			80	150				●					●			●	
		HM514900L-10			100	180				●					●			●	
		HM514280-7		262144×18	70	130	40			●					●			●	
		HM514280-8			80	150				●					●			●	
		HM514280-10			100	180				●					●			●	

(cont)

Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Dynamic	4.5 M-bit	HM514280L-7	CMOS	262144×18	70	130	40			●					●			●	
		HM514280L-8			80	150				●					●			●	
		HM514280L-10			100	180				●					●			●	
	16 M-bit	HM5116100-6		16777216×1	60	110	24					●	●		●			●	
		HM5116100-7			70	130						●	●		●			●	
		HM5116100-8			80	150						●	●		●			●	
		HM5116100-10			100	180						●	●		●			●	
		HM5116400-6		4194304×4	60	110						●	●		●			●	
		HM5116400-7			70	130						●	●		●			●	
		HM5116400-8			80	150						●	●		●			●	
		HM5116400-10			100	180						●	●		●			●	
		HM5116101-6		16777216×1	60	110	24,28					●			●			●	
		HM5116101-7			70	130						●			●			●	
		HM5116101-8			80	150						●			●			●	
		HM5116101-10			100	180						●			●			●	
		HM5116102-6			60	110	24					●	●		●			●	
		HM5116102-7			70	130						●	●		●			●	
		HM5116102-8			80	150						●	●		●			●	
		HM5116102-10			100	180						●	●		●			●	
		HM5116180-7		1048576×18	70	130	42,44, 50					●	●					●	
		HM5116180-8			80	150						●	●					●	
		HM5116180-10			100	180						●	●					●	
		HM5116190-7			70	130						●	●					●	
		HM5116190-8			80	150						●	●					●	
		HM5116190-10			100	180						●	●					●	
		HM5116160-7		1048576×16	70	130						●	●					●	
		HM5116160-8			80	150						●	●					●	

(cont)

Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Dynamic	16 M-bit	HM5116160-10	CMOS	1048576×16	100	180	42,44, 50					●	●					●	
		HM5116170-7			70	130						●	●					●	
		HM5116170-8			80	150						●	●					●	
		HM5116170-10			100	180						●	●					●	
		HM5116800-7*4		2097152×8	70	130	32					●	●					●	
		HM5116800-8*4			80	150						●	●					●	
		HM5116800-10*4			100	180						●	●					●	
		HM5116900-7*4			70	130						●	●					●	
		HM5116900-8*4			80	150						●	●					●	
		HM5116900-10*4			100	180						●	●					●	
		HM5116402-6		4194304×4	60	110	24					●	●		●			●	
		HM5116402-7			70	130						●	●		●			●	
		HM5116402-8			80	150						●	●		●			●	
		HM5116402-10			100	180						●	●		●			●	
		HM5116410-6			60	110						●	●		●			●	
		HM5116410-7			70	130						●	●		●			●	
		HM5116410-8			80	150						●	●		●			●	
		HM5116410-10			100	180						●	●		●			●	
		HM5116412-6			60	110						●	●		●			●	
		HM5116412-7			70	130						●	●		●			●	
		HM5116412-8			80	150						●	●		●			●	
		HM5116412-10			100	180						●	●		●			●	
		HM5117400-6			60	110						●	●		●			●	
		HM5117400-7			70	130						●	●		●			●	
		HM5117400-8			80	150						●	●		●			●	
		HM5117400-10			100	180						●	●		●			●	

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(cont)

Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Dynamic RAM module	2 M-bit	HB56K25608-6	CMOS	262144×8	60	120	30												●
		HB56K25608-7			70	130													●
		HB56K25608-8			80	160													●
		HB56K25608-10			100	190													●
		HB56K25608-12			120	220													●
	2.35 M-bit	HB56K25609-6		262144×9	60	120													●
		HB56K25609-7			70	130													●
		HB56K25609-8			80	160													●
		HB56K25609-10			100	190													●
		HB56K25609-12			120	220													●
	8 M-bit	HB56G18-6		1048576×8	60	110													●
		HB56G18-7			70	130													●
		HB56G18-8			80	150													●
		HB56G18-10			100	180													●
		HB56G18-6L			60	110													●
		HB56G18-7L			70	130													●
		HB56G18-8L			80	150													●
		HB56G18-10L			100	180													●
		HB56G18F-7			70	130													●
		HB56G18F-8			80	150													●
		HB56G18F-10			100	180													●
		HB56G18F-7L			70	130													●
		HB56G18F-8L			80	150													●
		HB56G18F-10L			100	180													●
	9M-bit	HB56G19-6		1048576×9	60	120													●
		HB56G19-7			70	130													●
		HB56G19-8			80	160													●

(cont)

Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Dynamic RAM module	9 M-bit	HB56G19-10	CMOS	1048576×9	100	190	30												●
		HB56G19-6L			60	120													●
		HB56G19-7L			70	130													●
		HB56G19-8L			80	160													●
		HB56G19-10L			100	190													●
		HB56G25636-7		262144×36	70	130	72												●
		HB56G25636-8			80	150													●
		HB56G25636-10			100	180													●
		HB56G25636-7L			70	130													●
		HB56G25636-8L			80	150													●
		HB56G25636-10L			100	180													●
		HB56G19F-7		1048576×9	70	130	30												●
		HB56G19F-8			80	160													●
		HB56G19F-10			100	190													●
		HB56G19F-7L			70	130													●
		HB56G19F-8L			80	160													●
		HB56G19F-10L			100	190													●
	10 M-bit	HB56A25640-6		262144×40	60	120	72												●
		HB56A25640-7			70	130													●
		HB56A25640-8			80	160													●
		HB56A25640-10			100	190													●
	18 M-bit	HB56G51236-7		524288×36	70	130													●
		HB56G51236-8			80	150													●
		HB56G51236-10			100	180													●
		HB56G51236-7L			70	130													●
		HB56G51236-8L			80	150													●
		HB56G51236-10L			100	180													●

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(cont)

Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Dynamic RAM module	20 M-bit	HB56A51240-6	CMOS	524288×40	60	120	72												●
		HB56A51240-7			70	130													●
		HB56A51240-8			80	160													●
		HB56A51240-10			100	190													●
	32 M-bit	HB56D132R-7		1048576×32	70	130													●
		HB56D132R-8			80	150													●
		HB56D132R-10			100	180													●
		HB56D132R-7L			70	130													●
		HB56D132R-8L			80	150													●
		HB56D132R-10L			100	180													●
		HB56A48-7		4194304×8	70	130	30												●
		HB56A48-8			80	150													●
		HB56A48-10			100	180													●
		HB56A48-7L			70	130													●
		HB56A48-8L			80	150													●
		HB56A48-10L			100	180													●
		HB56B48-7			70	130													●
		HB56B48-8			80	150													●
		HB56B48-10			100	180													●
		HB56C48-7			70	130													●
		HB56C48-8			80	150													●
		HB56C48-10			100	180													●
	36 M-bit	HB56D136-7		1048576×36	70	130	72												●
		HB56D136-8			80	160													●
		HB56D136-10			100	190													●
		HB56D136-7L			70	130													●
		HB56D136-8L			80	160													●

(cont)

Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Dynamic RAM module	36 M-bit	HB56D136-10L	CMOS	1048576×36	100	190	72												●
		HB56A49-7		4194304×9	70	130	30												●
		HB56A49-8			80	150													●
		HB56A49-10			100	180													●
		HB56A49-7L			70	130													●
		HB56A49-8L			80	150													●
		HB56A49-10L			100	180													●
		HB56B49-7			70	130													●
		HB56B49-8			80	150													●
		HB56B49-10			100	180													●
		HB56C49-7			70	130													●
		HB56C49-8			80	150													●
		HB56C49-10			100	180													●
	40 M-bit	HB56A140-6		1048576×40	60	110	72												●
		HB56A140-7			70	130													●
		HB56A140-8			80	150													●
		HB56A140-10			100	180													●
		HB56A140-6L			60	110													●
		HB56A140-7L			70	130													●
		HB56A140-8L			80	150													●
		HB56A140-10L			100	180													●
	64 M-bit	HB56D232-7		2097152×32	70	130													●
		HB56D232-8			80	150													●
		HB56D232-10			100	180													●
		HB56D232-7L			70	130													●
		HB56D232-8L			80	150													●
		HB56D232-10L			100	180													●

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(cont)

Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Dynamic RAM module	72 M-bit	HB56D236-7	CMOS	2097152×36	70	130	72												●
		HB56D236-8			80	160													●
		HB56D236-10			100	190													●
		HB56D236-7L			70	130													●
		HB56D236-8L			80	160													●
		HB56D236-10L			100	190													●
	80 M-bit	HB56A240-6		2097152×40	60	110													●
		HB56A240-7			70	130													●
		HB56A240-8			80	150													●
		HB56A240-10			100	180													●
		HB56A240-6L			60	110													●
		HB56A240-7L			70	130													●
		HB56A240-8L			80	150													●
		HB56A240-10L			100	180													●
	134 M-bit	HB56A168-6		16777216×8	60	110													●
		HB56A168-7			70	130													●
		HB56A168-8			80	150													●
		HB56A168-10			100	180													●
	150 M-bit	HB56D436-6		4194304×36	60	110													●
		HB56D436-7			70	130													●
		HB56D436-8			80	150													●
		HB56D436-10			100	180													●
		HB56A169-6		16777216×9	60	110	30												●
		HB56A169-7			70	130													●
		HB56A169-8			80	150													●
		HB56A169-10			100	180													●

(cont)

Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	ZP	CG	CP	JP	M
Dynamic RAM module	167 M-bit	HB56A440-6	CMOS	4194304×40	60	110													●
		HB56A440-7			70	130													●
		HB56A440-8			80	150													●
		HB56A440-10			100	180													●
	301 M-bit	HB56D836-6		8388608×36	60	110													●
		HB56D836-7			70	130													●
		HB56D836-8			80	150													●
		HB56D836-10			100	180													●
	335 M-bit	HB56A840-6		8388608×40	60	110													●
		HB56A840-7			70	130													●
		HB56A840-8			80	150													●
		HB56A840-10			100	180													●

MOS ROM

Program	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Package: Pin No.	G	P	FP	T	R	TT	RR	CG	CC	CP	JP
Mask	256 k-bit	HN623257	CMOS	32768×8	120	28		●	●								
	1 M-bit	HN62331		131072×8	120			●	●								
		HN62321			150			●	●								
		HN62321B			200			●	●								
		HN62321E			200			●	●								
		HN62331A			120	32		●	●								
		HN62321A			150			●	●								
	2 M-bit	HN62422		131072×16 or 262144×8	150	40,44		●	●								
		HN62412			200			●	●								
		HN62302B-17		262144×8	170	32		●	●								
		HN62302B-20			200			●	●								
		HN62442B		131072×16	100	40,44		●								●	
	4 M-bit	HN62414-15		262144×16 or 524288×8	150	40,44 48,64		●	●								
		HN62414-17			170			●	●								
		HN62414-20			200			●	●								
		HN62434-15			150			●	●								
		HN62434-17			170			●	●								
		HN62434-20			200			●	●								
		HN62444		262144×16	100	40,44,48		●	●								
		HN62444B			100	40,44		●	●								●
		HN62314B-15		524288×8	150	32		●	●								
		HN62314B-17			170			●	●								
		HN62314B-20			200			●	●								
		HN62334B			150			●	●								
		HN62334B-17			170			●	●								
		HN62334B-20			200			●	●								
		HN62344B			100			●	●								

(cont)

Program	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Package Pin No.	G	P	FP	T	R	TT	RR	CG	CC	CP	JP
Mask	8 M-bit	HN62418	CMOS	524288×8 or 1048576×8	150	32,42 44,64		●	●								
		HN62428			200			●	●								
		HN62318B		1048576×8	150	32		●	●								
		HN62328B			200			●	●								
	16 M-bit	HN624116-15		1048576×16 or 2097152×8	150	42,44 48		●	●								
		HN624116-20			200			●	●								
Electrically erasable and programmable	64 k-bit	HN58C65-25		8192×8	250	28		●	●								
		HN58C66-25			250			●	●	●							
	256 k-bit	HN58C256-20		32768×8	200			●	●								
		HN58C257-20			200	32				●	●						
		HN58V257-35			350							●	●				
	1 M-bit	HN58C1001-12		131072×8	120			●		●	●						●
		HN58C1001-15			150			●		●	●						●
		HN58V1001-25			250			●		●	●						●
Flash memory		HN29C101-12			120			●		●	●						
		HN29C101-15			150			●		●	●						
		HN29C101-20			200			●		●	●						
		HN28F101-12			120			●	●	●	●					●	
		HN28F101-15			150			●	●	●	●					●	
		HN28F101-20			200			●	●	●	●					●	

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(cont)

Program	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Package Pin No.	G	P	FP	T	R	TT	RR	CG	CC	CP	JP
Flash memory	4 M-bit	HN28F4001-12	CMOS	524288×8	120	32		●		●	●						●
		HN28F4001-15			150			●		●	●						●
		HN28F4001-20			200			●		●	●						●
UV erasable and programmable	256 k-bit	HN27C256A-10		32768×8	100	28	●										
		HN27C256A-12			120		●										
		HN27C256A-15			150		●										
		HN27C256H-70			70		●										
		HN27C256H-85			85		●										
	512 k-bit	HN27512-25	NMOS	65536×8	250	28	●										
		HN27512-30			300		●										
		HN27C512-17	CMOS		170		●										
		HN27C512-20			200		●										
	1 M-bit	HN27C1024H-85		65536×16	85	40,44	●								●		
		HN27C1024H-10			100		●								●		
		HN27C1024H-12			120		●								●		
		HN27C1024H-15			150		●								●		
		HN27C101A-10		131072×8	100	32	●										
		HN27C101A-12			120		●										
		HN27C101A-15			150		●										
		HN27C101A-17			170		●										
		HN27C101A-20			200		●										
		HN27C101A-25			250		●										
		HN27C301A-10			100		●										
		HN27C301A-12			120		●										
		HN27C301A-15			150		●										
		HN27C301A-17			170		●										

(cont)

Program	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Package Pin No.	G	P	FP	T	R	TT	RR	CG	CC	CP	JP
UV erasable and programmable	1 M-bit	HN27C301A-20	CMOS	131072×8	200	32	●										
		HN27C301A-25			250		●										
	4 M-bit	HN27C4096-10		262144×16	100	40,44	●								●		
		HN27C4096-12			120		●								●		
		HN27C4096-15			150		●								●		
		HN27C4001-10		524288×8	100	32	●										
		HN27C4001-12			120		●										
		HN27C4001-15			150		●										
		HN27C4096-70		262144×16	70	40,44	●							●			
		HN27C4096-85			85		●							●			
One time electically programmable	256 k-bit	HN27C256A-12		32768×8	120	28		●	●								
		HN27C256A-15			150			●	●								
		HN27C256H-85			85			●	●								
		HN27C256H-10			100			●	●								
	512 k-bit	HN27512-25	NMOS	65536×8	250			●									
		HN27512-35			300			●									
	1 M-bit	HN27C1024H-10	CMOS	65536×16	100	44										●	
		HN27C1024H-12			120											●	
		HN27C1024H-15			150											●	
		HN27C101A-12		131072×8	120	32		●	●			●	●				
		HN27C101A-15			150			●	●			●	●				
		HN27C101A-20			200			●	●								
		HN27C101A-25			250			●	●								
		HN27C301A-12			120			●	●								
		HN27C301A-15			150			●	●								
		HN27C301A-20			200			●	●								
		HN27C301A-25			250			●	●								

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(cont)

Program	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Package Pin No.	G	P	FP	T	R	TT	RR	CG	CC	CP	JP
One time electically programmable	1 M-bit	HN27V101-20	CMOS	131072×8	200	32						●	●				
		HN27V101-25			250							●	●				
	4 M-bit	HN27C4096-12		262144×16	120	44										●	
		HN27C4096-15			150											●	
		HN27C4001-12*3		524288×8	120	32						●	●				
		HN27C4001-15*3			150							●	●				

ECL RAM

Mode	Total bit	Type No.	Organization (word×bit)	Output	Access time (ns) max	Supply voltage (V)	Power dissipation (W)	Package Pin No.	G	F	CG	JP
ECL 10 k	64 k-bit	HM10494-10	16384×4	Open emitter	10	–5.2	0.8	28	●			
		HM10494-12			12				●			●
		HM10490-10	65536×1		10		0.57	22	●			
		HM10490-12			12				●			
	256 k-bit	HM10500-15	262144×1		15		0.52	24	●			
ECL 100 k	64 k-bit	HM100494-10	16384×4		10	–4.5	0.65	28				●
		HM100494-12			12							●
		HM101494-8			8	–5.2	0.8			●		●
		HM101494-10			10		0.73		●			●
		HM101494-12			12				●			●
		HM101490-10	65536×1		10		0.57	22,24	●			●
		HM101490-12			12				●			●
	256 k-bit	HM100504-10	65536×4		10	–4.5	0.65	28,32		●		●
		HM100504-12			12					●		●
		HM101504-10			10	–5.2	0.75			●		●
		HM101504-12			12					●		●
		HM100500-18	262144×1		18	–4.5	0.5	28,24	●	●	●	
		HM101500F-15			15			24		●		
	1 M-bit	HM101514F-15*3	262144×4		15	–5.2	0.8	32		●		●
		HM101510F-15	1048576×1		15		0.7	28		●		
		HM101513F-15*4	262144×4		15	–4.2	0.8	32		●		
		HM101515F-15*4			15	–5.2				●		

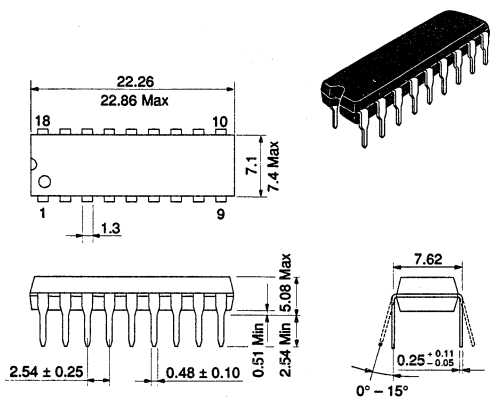
Notes: 1. The package codes in the table are applied to the package material as follows.
G: cerdip, P: plastic DIP, FP: Plastic flat package (SOP),
T: thin small outline package (TSOP) type I,
R: TSOP type I reverse type, TT: TSOP type II, RR: TSOP type II reverse type, TG: TSOP type II with window,
SP: skinny type plastic DIP, ZP: plastic ZIP, CG: ceramic leadless chip carrier,
CP: plastic leaded chip carrier, JP: plastic small outline J-bend package,
F: flat package, M: module
2. Maintenance only. This device is not available for new application.
3. Preliminary
4. Under development.

Package Information

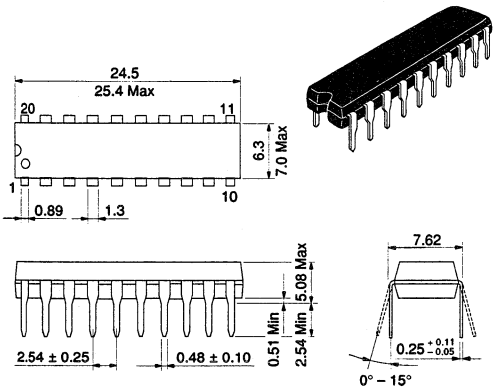
Dual-in-line Plastic

Unit: mm

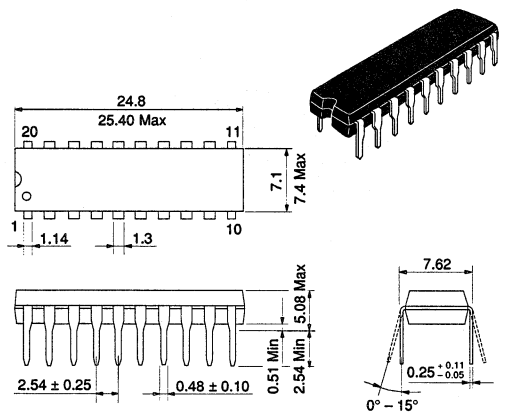
- DP-18C



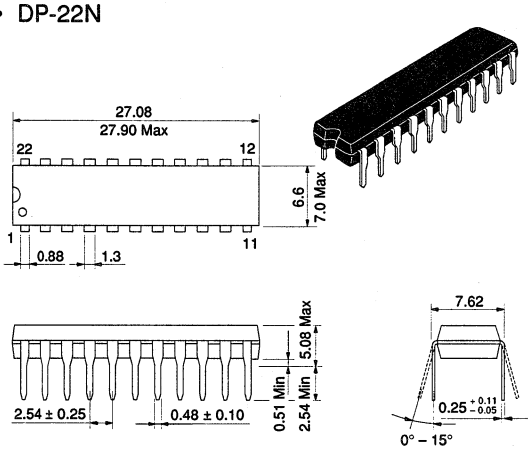
- DP-20N



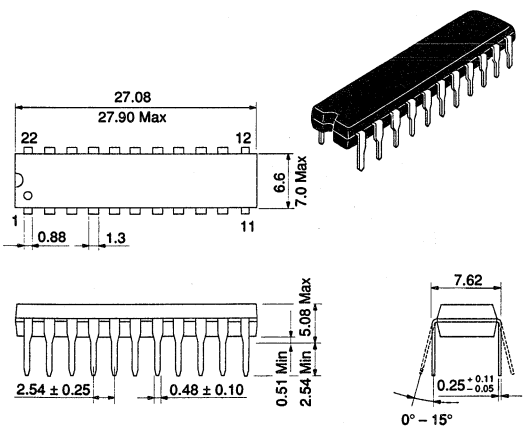
- DP-20NA



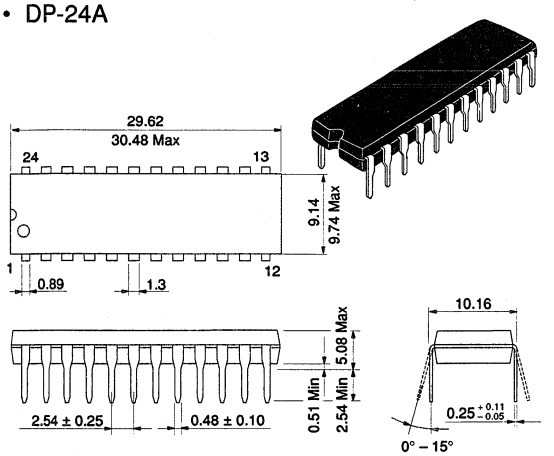
- DP-22N



- DP-22NB



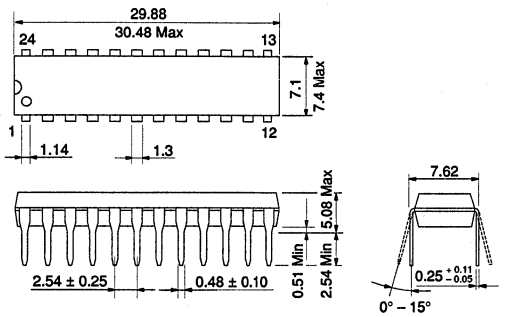
- DP-24A

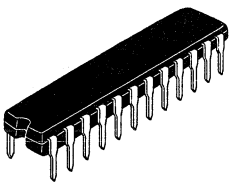


Package Information

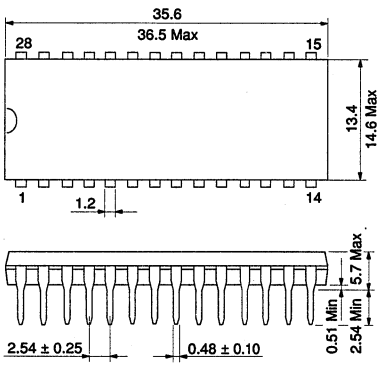
Unit: mm

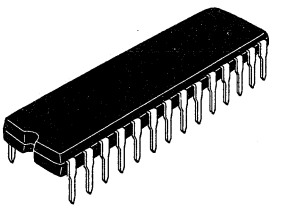
- DP-24NC



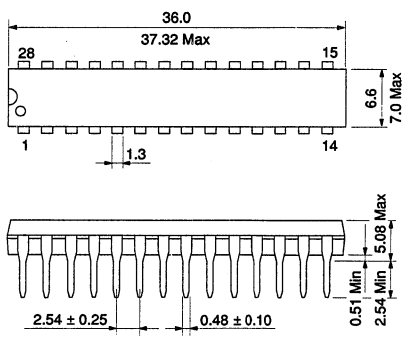


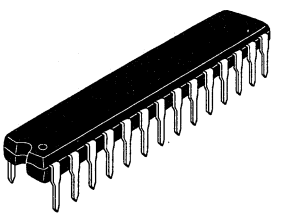
- DP-28





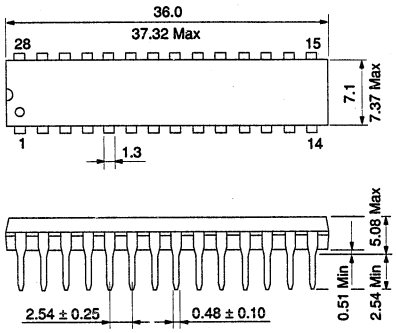
- DP-28N

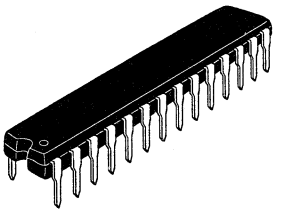


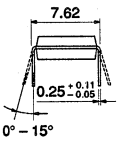


Unit: mm

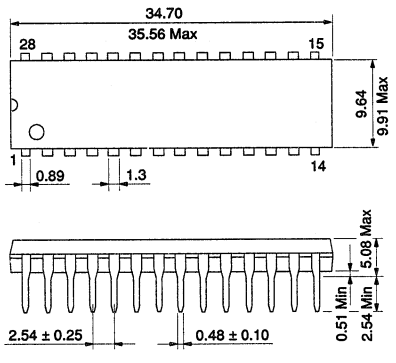
• DP-28NA

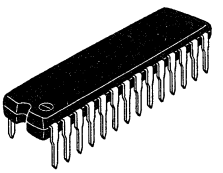


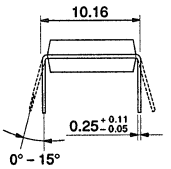




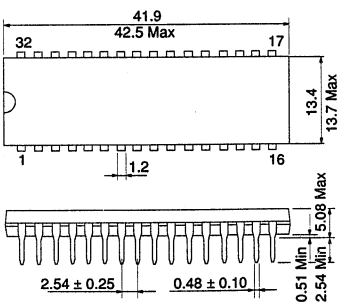
• DP-28C

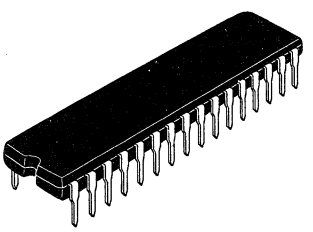


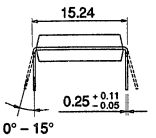




• DP-32



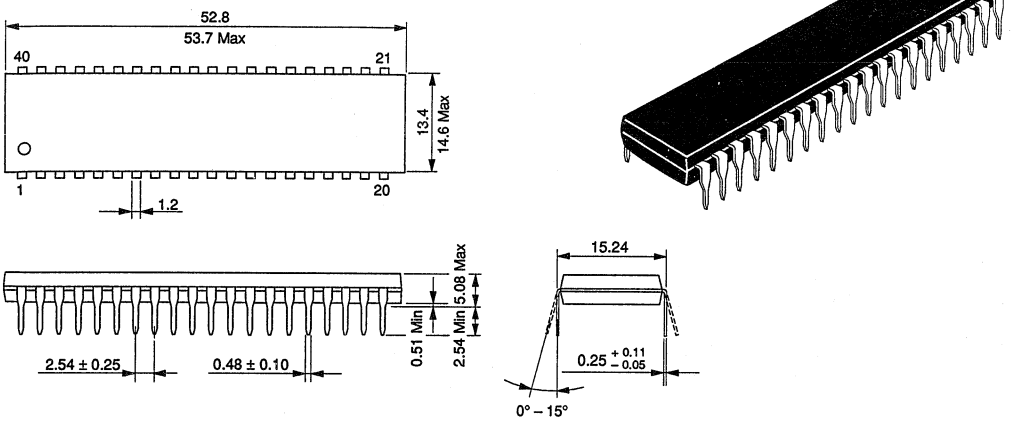




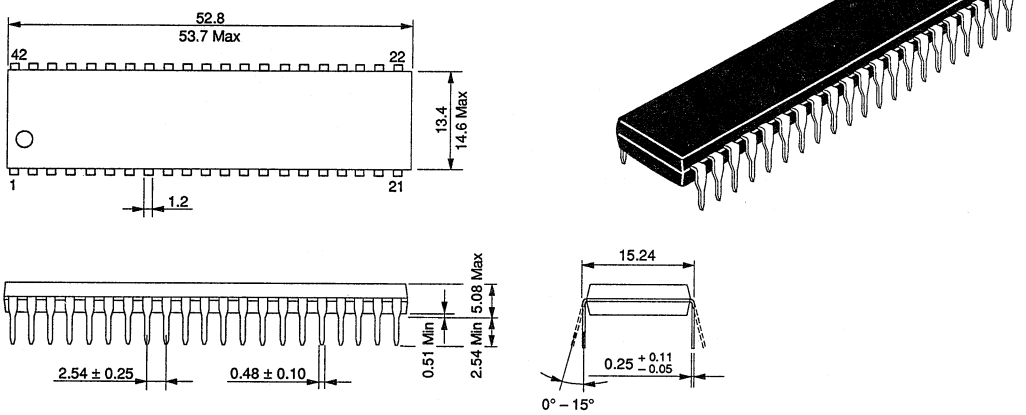
Package Information

Unit: mm

- DP-40



- DP-42



Applicable ICs

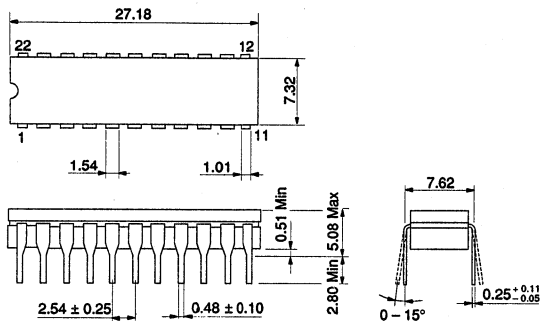
DP-18C	HM53051P Series, HM511000AP Series, HM511000ALP Series, HM511001AP Series, HM511002AP Series
DP-20N	HM6268P Series, HM6268LP Series, HM6267P Series, HM6267LP Series
DP-20NA	HM514256AP Series, HM514256ALP Series, HM514258AP Series, HM514266A Series
DP-22N	HM6287P Series, HM6287LP Series
DP-22NB	HM6288P Series, HM6288LP Series, HM6287HP Series, HM6287HLP Series
DP-24A	HM53461P Series, HM53462P Series
DP-24NC	HM6716P Series, HM6719P Series, HM6789HAP Series, HM6208HP Series, HM6208HLP Series, HM6708AP Series, HM6207HP Series, HM6207HLP Series, HM6707AP Series
DP-28	HM6264AP Series, HM6264ALP Series, HM6264ALP-L Series, HM62256P Series, HM62256LP Series, HM62256LP-SL Series, HM62256AP Series, HM62256ALP Series, HM62256ALP-SL Series, HM65256BP Series, HM65256BLP Series, HN623257PZ, HN62321P, HN62321BP, HN62331P, HN62321EP, HN62321AP, HN62331AP, HN58C65P Series, HN58C66P Series, HN58C256P Series, HN27C256AP Series, HN27C256HP Series, HN27512P Series
DP-28N	HM6264ASP Series, HM6264ALSP Series, HM6264ALSP-L Series, HM65256BSP Series, HM65256BLSP Series, HM63021P Series
DP-28NA	HM62256ASP Series, HM62256ALSP Series, HM62256ALSP-SL Series, HM62832HP Series, HM62832HLP Series, HM62832UHP Series, HM62832UHLP Series, HM63921 Series
DP-28C	HM624256P Series, HM624256LP Series, HM624256AP Series, HM624256ALP Series, HM621100AP Series, HM621100ALP Series
DP-32	HM628128P Series, HM628128LP Series, HM628128LP-SL Series, HM628512P Series, HM628512LP Series, HM628512LP-SL Series, HM658128ADP Series, HM658128ALP Series, HM658128ALP-L Series, HM658512DP Series, HM658512LP Series, HM658512LP-L Series, HN58C1000P Series, HN29C101P Series, HN29C101B Series, HN62314BP, HN62334BP, HN62344BP, HN62321AP, HN62331AP, HN62321GP, HN62318BP, HN62328BP, HN62302BP, HN27C101AP Series, HN27C301AP Series, HN28F4001P Series, HM628128AP Series, HM628128ALP Series, HM628128ALP-SL Series, HM629128P Series, HM629128LP Series, HM629128LP-SL Series, HM62V8128P Series, HM62V8128LP Series, HM62V8128LP-SL Series, HN58V1001P Series, HN58C1001P Series
DP-40	HN62412P, HN62422P, HN62444P, HN62444BP, HN62442BP, HN62414P, HN62434P
DP-42	HN62428P, HN62418P, HN62428P, HN624116P

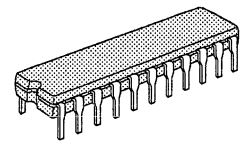
Package Information

CERDIP

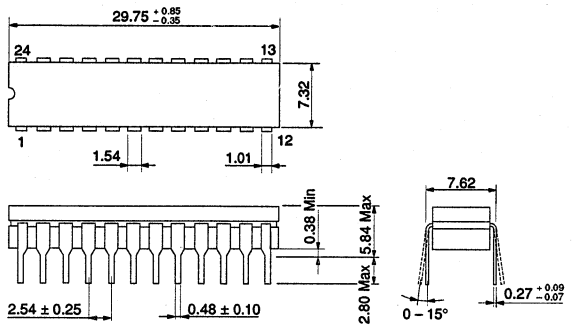
Unit: mm

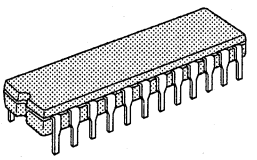
- DG-22N



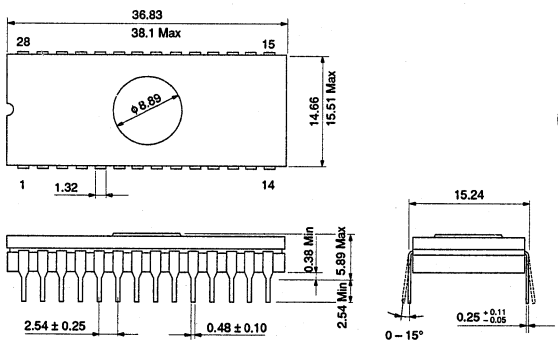


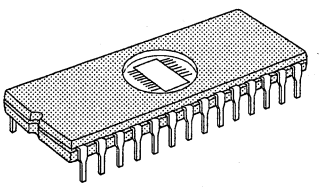
- DG-24V



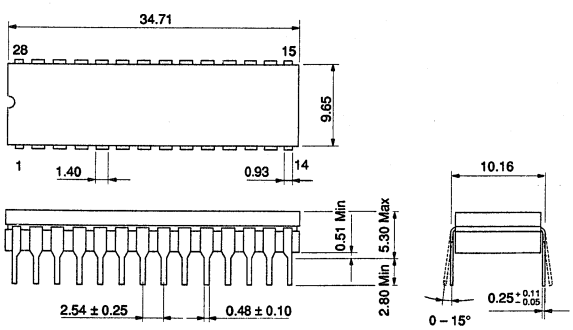


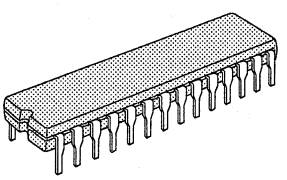
- DG-28





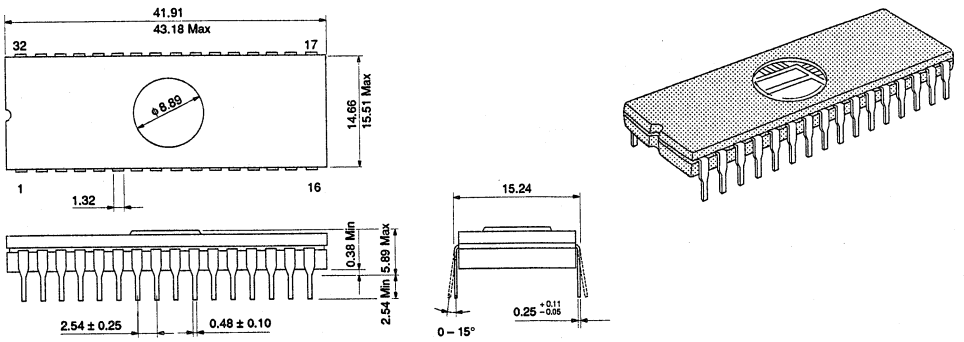
- DG-28N



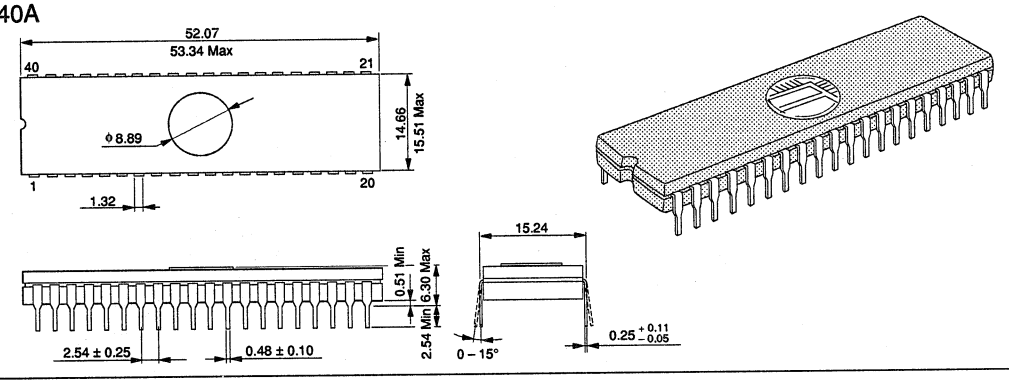


Unit: mm

• DG-32



• DG-40A



Applicable ICs

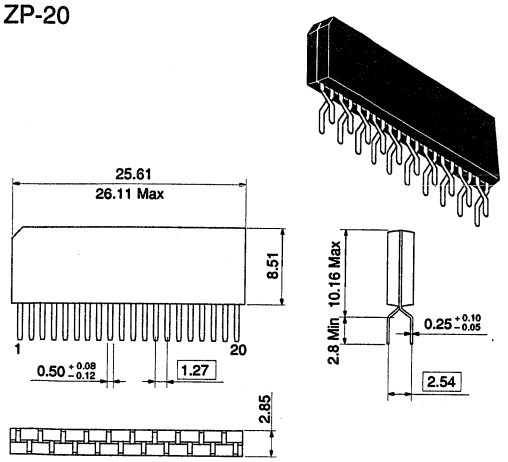
DG-22N	HM10490 Series, HM101490 Series
DG-24V	HM10500 Series, HM100500 Series
DG-28	HN27C256AG Series, HN27C256HG Series, HN27512G Series
DG-28N	HM10494 Series, HM101494 Series
DG-32	HN27C101AG Series, HN27C301AG Series, HN27C4001G Series
DG-40A	HN27C1024HG Series, HN27C4096G Series, HN27C4096HG Series

Package Information

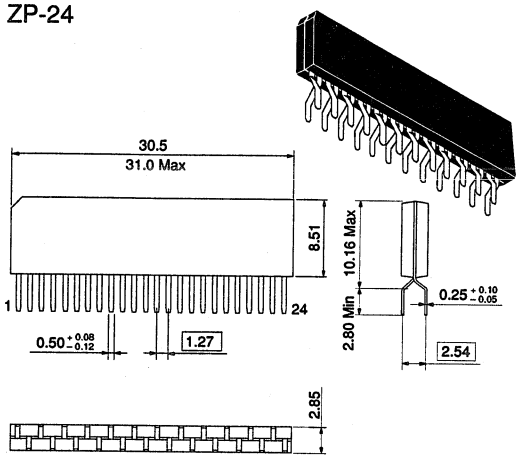
Zigzag-in-line Plastic

Unit: mm

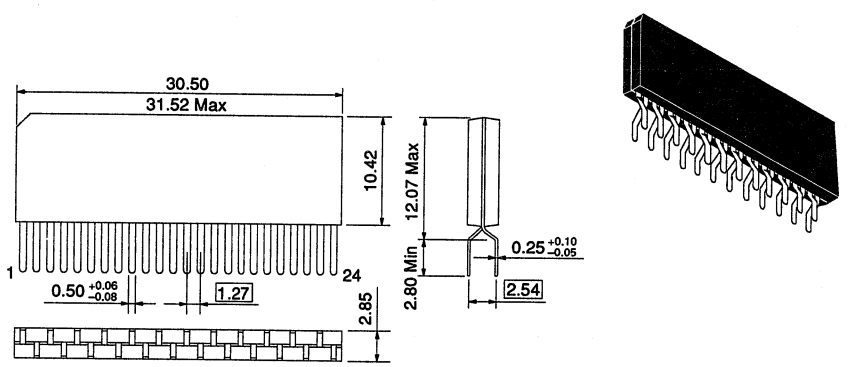
• ZP-20



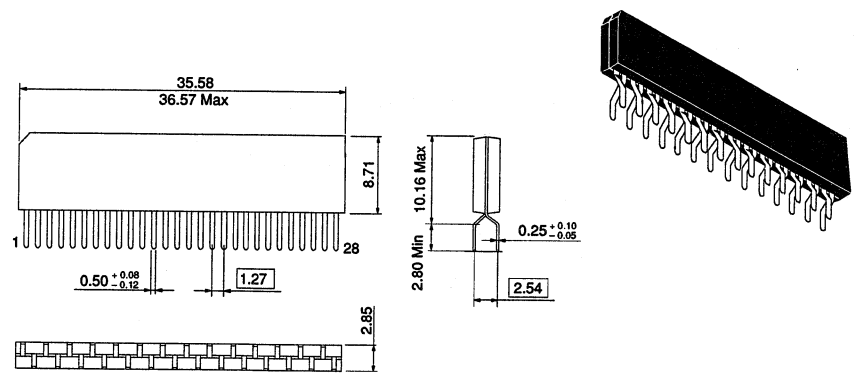
• ZP-24



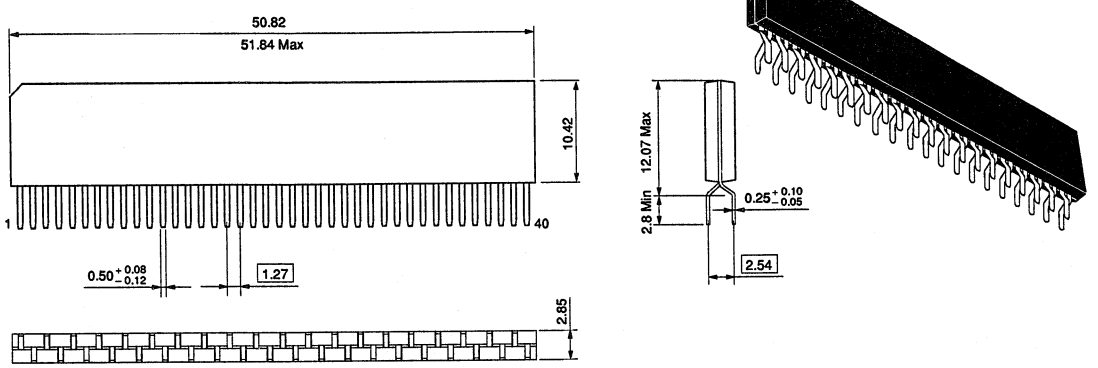
• ZP-24A



• ZP-28



• ZP-40



Applicable ICs

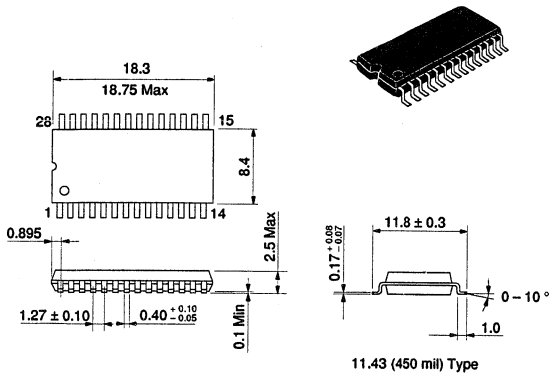
ZP-20	HM514256AZP Series, HM514256ALZP Series, HM514258AZP Series, HM514266A Series, HM511000AZP Seires, HM511000ALZP Series, HM511001AZP Series, HM511002AZP Series, HM514400ZP Series, HM514400LZP Series, HM514400SLZ Series, HM514402ZP Series, HM514410ZP Series, HM514100ZP Series, HM514100LZP Series, HM514100SLZ Series, HM514101ZP Series, HM514102ZP Series, HM514400AZ Series, HM514400ALZ Series, HM514400ASLZ Series, HM514402AZ Series, HM514402ALZ Series, HM514402ASLZ Series, HM514410AZ Series, HM514410ALZ Series, HM514410ASLZ Series, HM514412AZ Series, HM514412ALZ Series, HM514412ASLZ Series, HM514100AZ Series, HM514100ALZ Series, HM514100ASLZ Series, HM514101AZ Series, HM514101ALZ Series, HM514101ASLZ Series, HM514102AZ Series, HM514102ALZ Series, HM514102ASLZ Series
ZP-24	HM53461ZP Series, HM53462ZP Series
ZP-24A	HM5116100ZP Series, HM5116400ZP Series, HM5117400Z Series, HM5116402Z Series, HM5116102Z Series, HM5116101Z Series, HM5116412Z Series, HM5116410Z Series
ZP-28	HM534251ZP Series, HM534252ZP Series, HM534251AZ Series, HM534253AZ Series, HM574256ZP Series, HM571000ZP Series, HM514800ZP Series, HM514800LZP Series, HM514900ZP Series, HM514900LZP Series
ZP-40	HM538121AZ Series, HM538123AZ Series, HM511664ZP Series, HM511665ZP Series, HM514280ZP Series, HM514280LZP Series, HM514260ZP Series, HM514260LZP Series, HM514170ZP Series, HM514170LZP Series, HM514190ZP Series, HM514190LZP Series, HM511666Z Series, HM511666LZ Series

Package Information

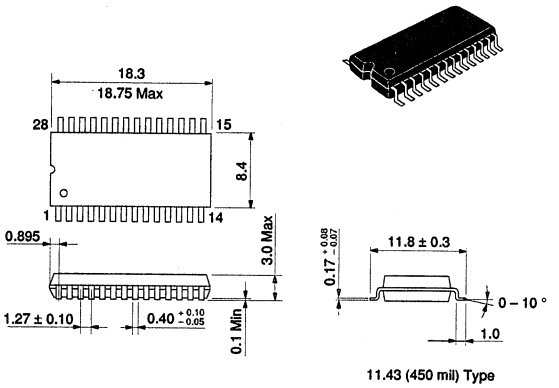
Flat Package

Unit: mm

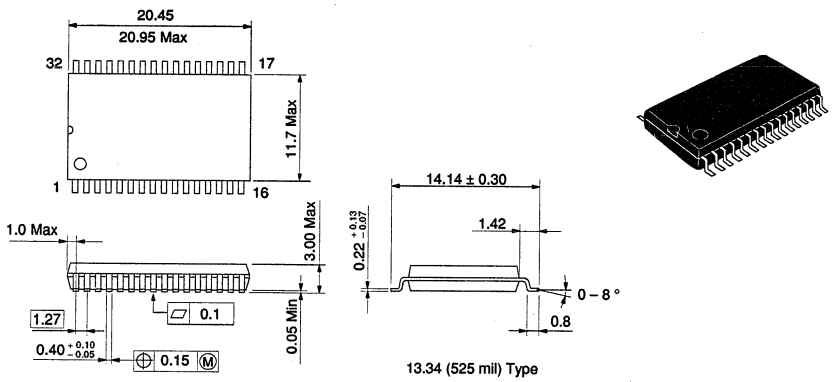
• FP-28D



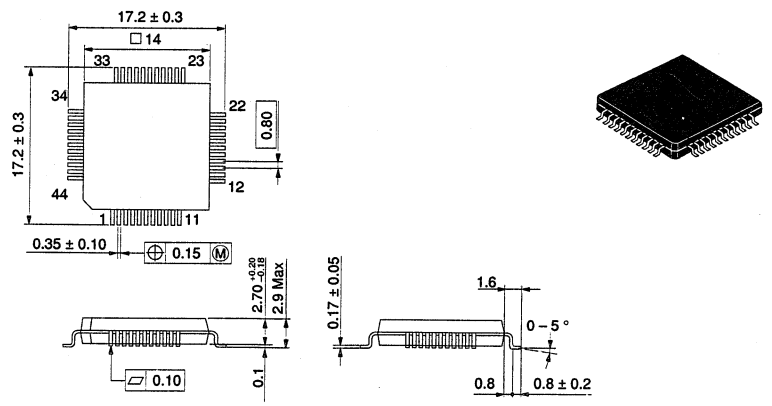
• FP-28DA



• FP-32D

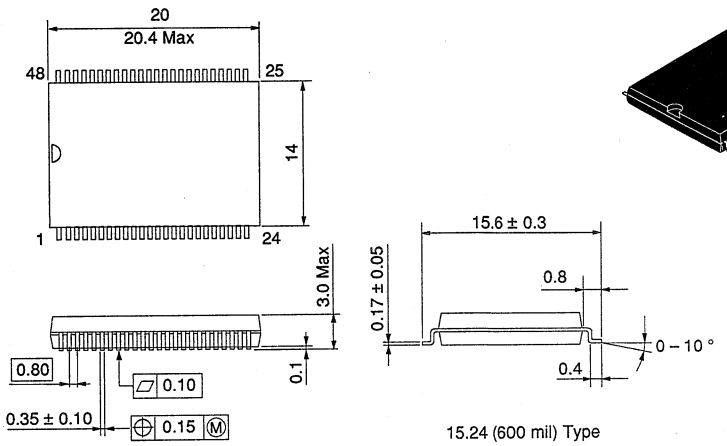


• FP-44A

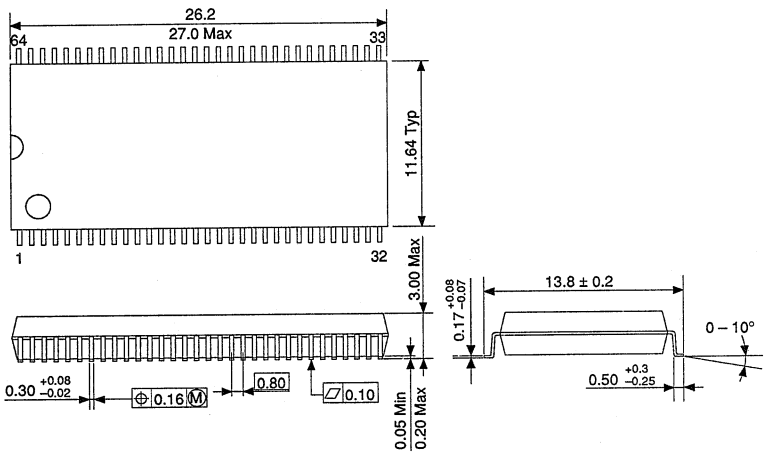


Unit: mm

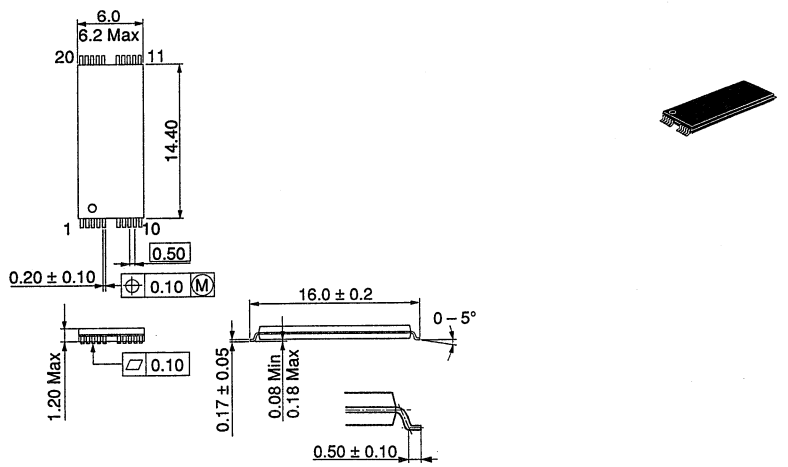
• FP-48DA



• FP-64DS



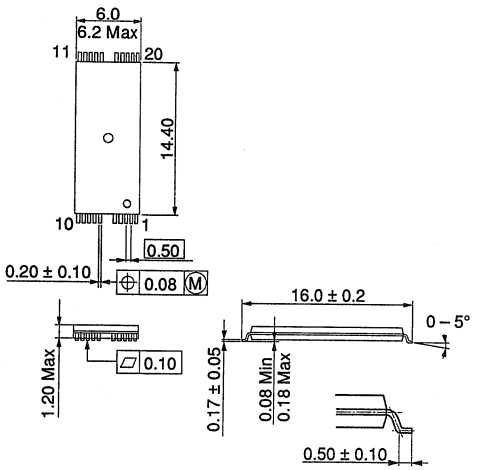
• TFP-20D



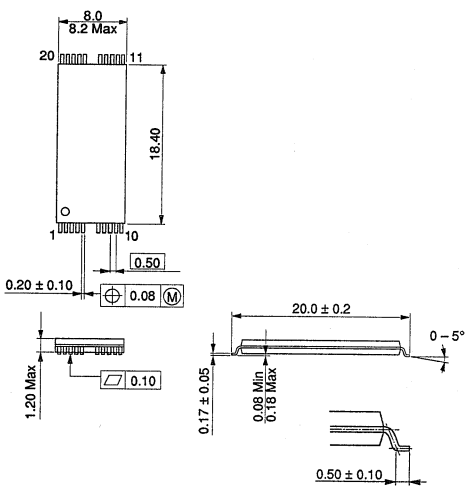
Package Information

Unit: mm

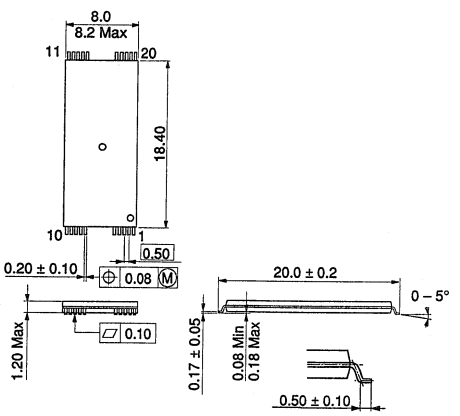
- TFP-20DR



- TFP-20DA

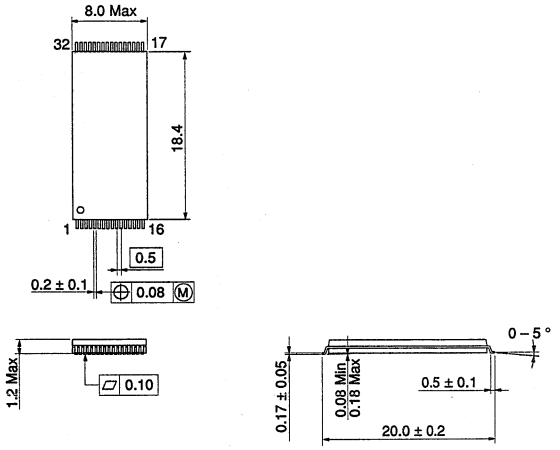


- TFP-20DAR

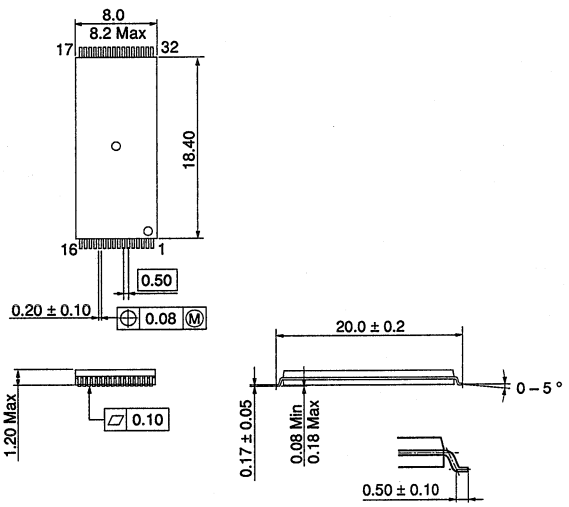


Unit: mm

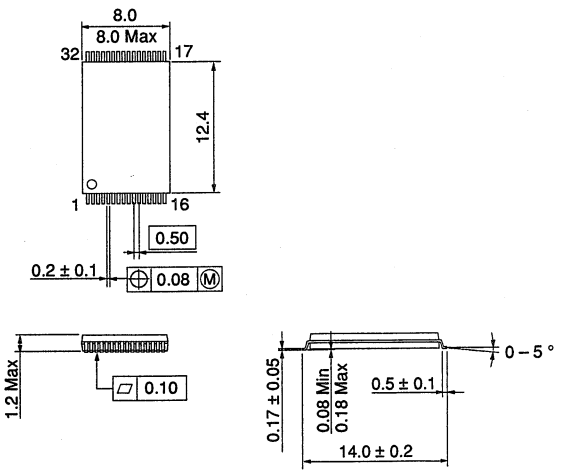
- TFP-32D



- TFP-32DR



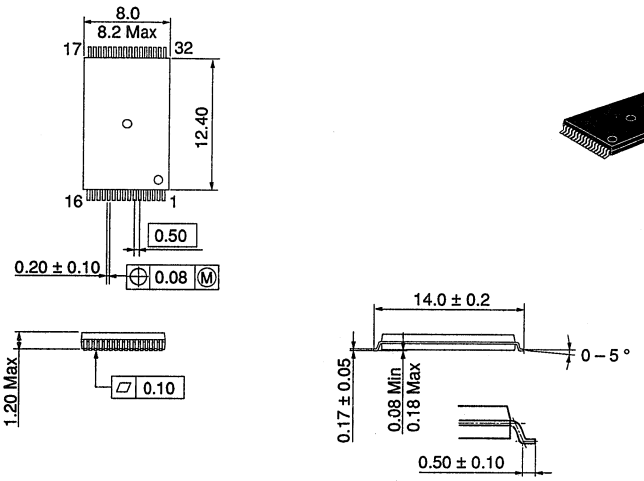
- TFP-32DA



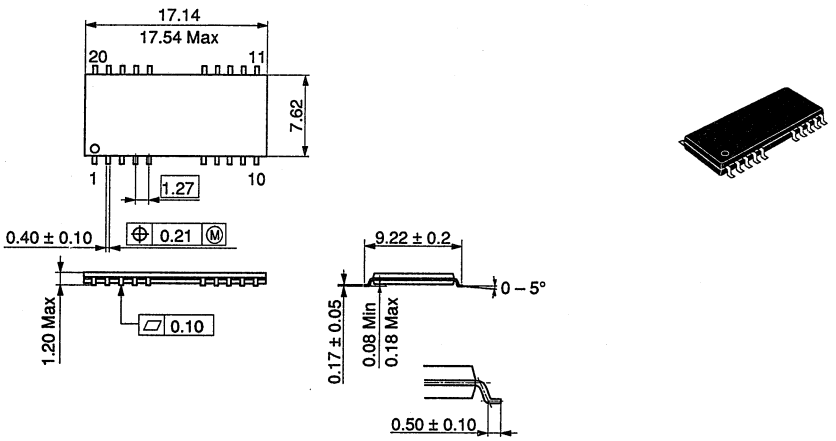
Package Information

Unit: mm

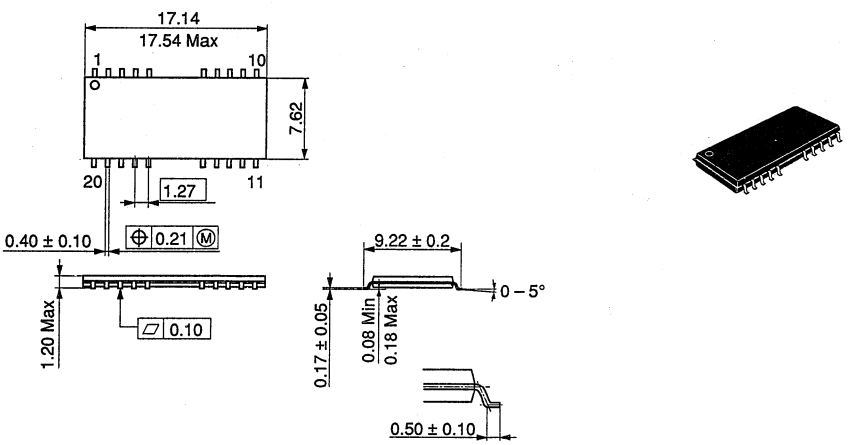
- TFP-32DAR



- TTP-20D

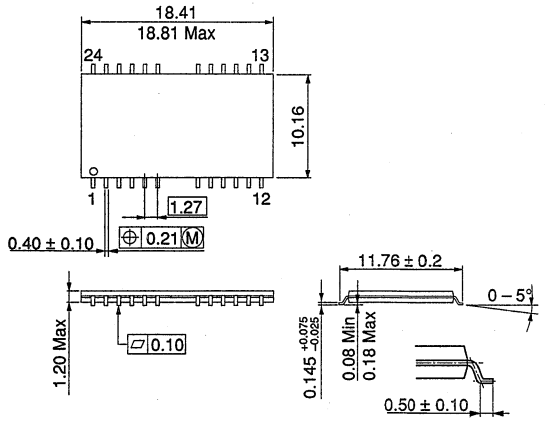


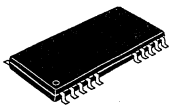
- TTP-20DR



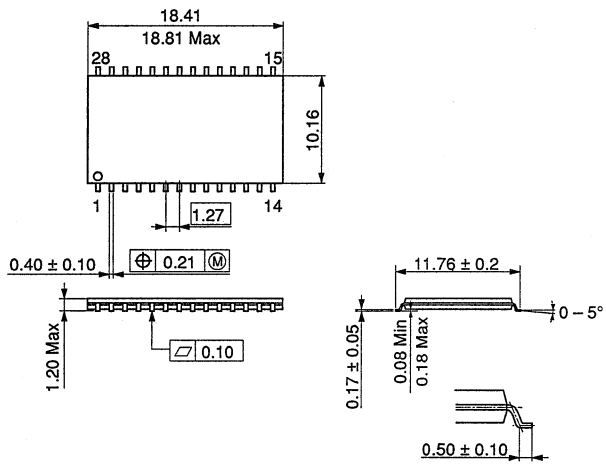
Unit: mm

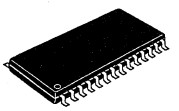
- TTP-24D



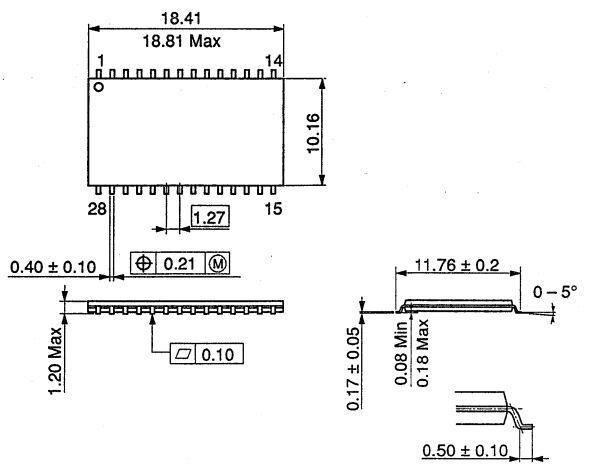


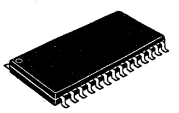
- TTP-28D





- TTP-28DR

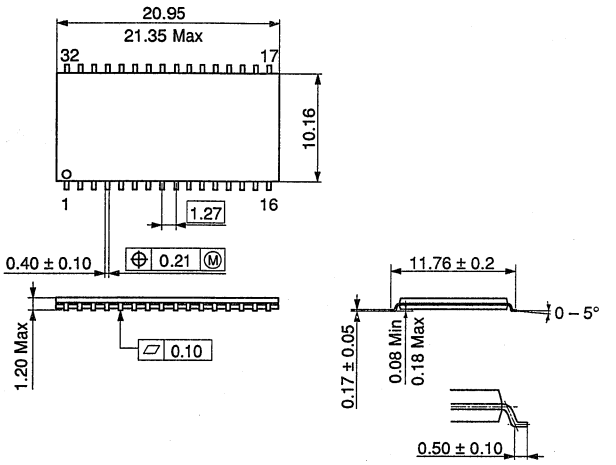


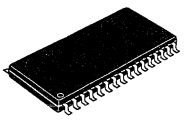


Package Information

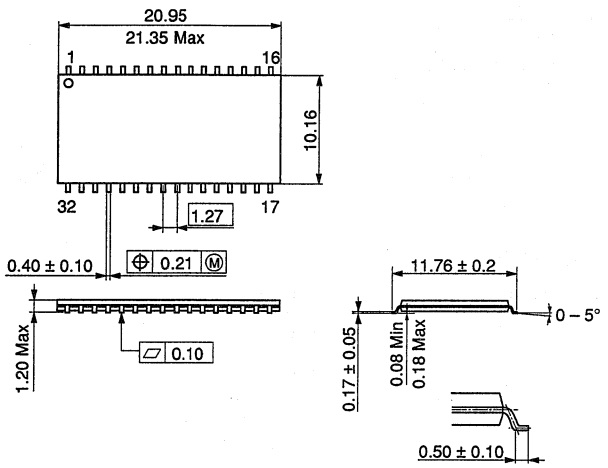
Unit: mm

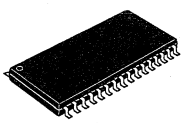
- TTP-32D



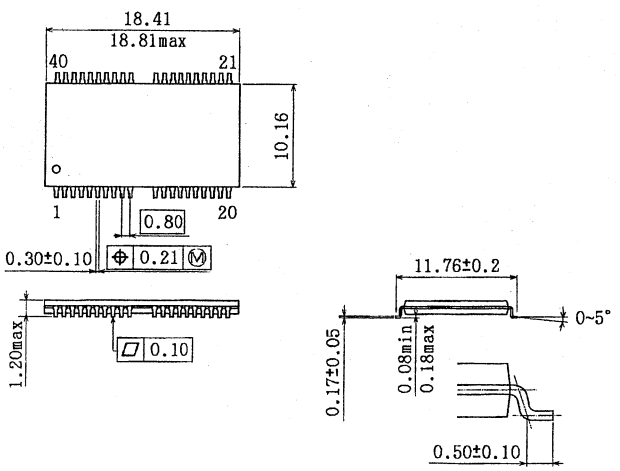


- TTP-32DR



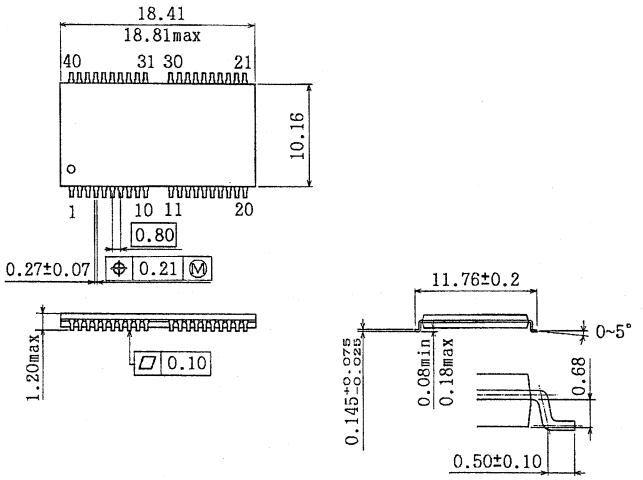


- TTP-40DA

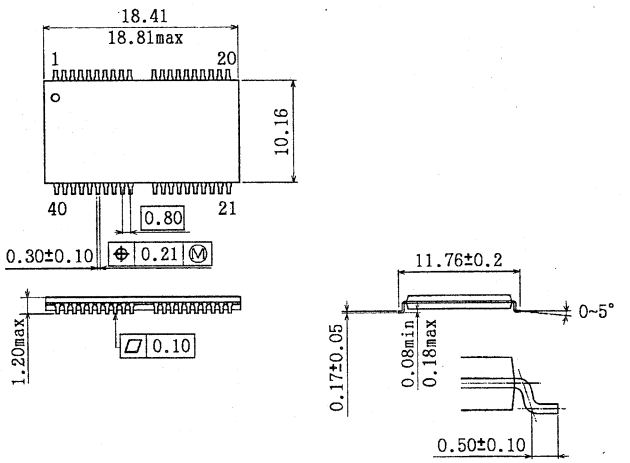


Unit: mm

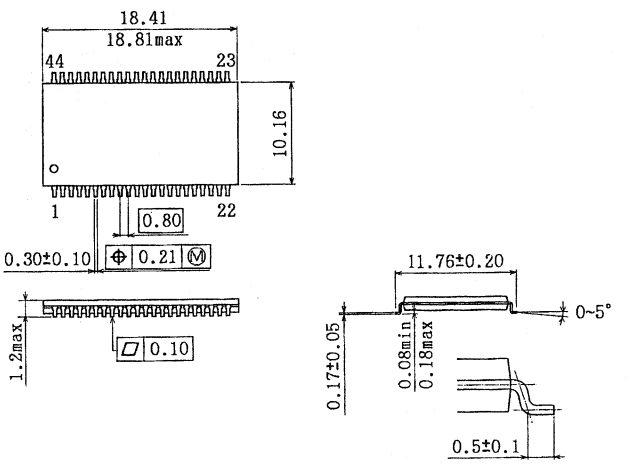
- TTP-40DB



- TTP-40DAR



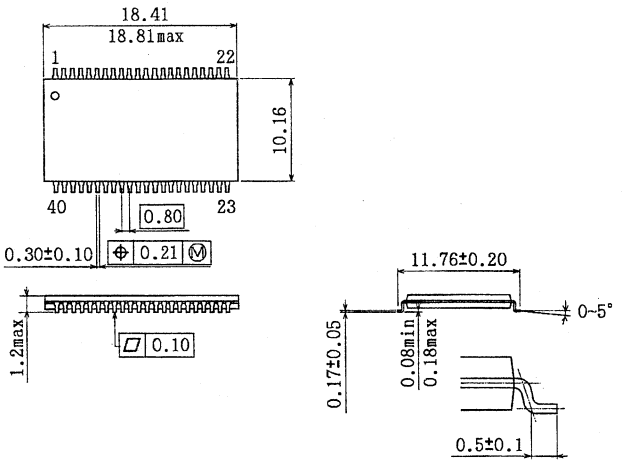
- TTP-44DB



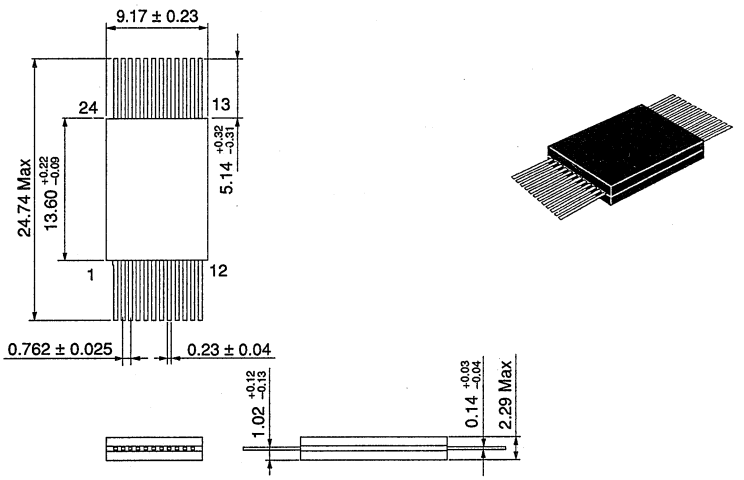
Package Information

Unit: mm

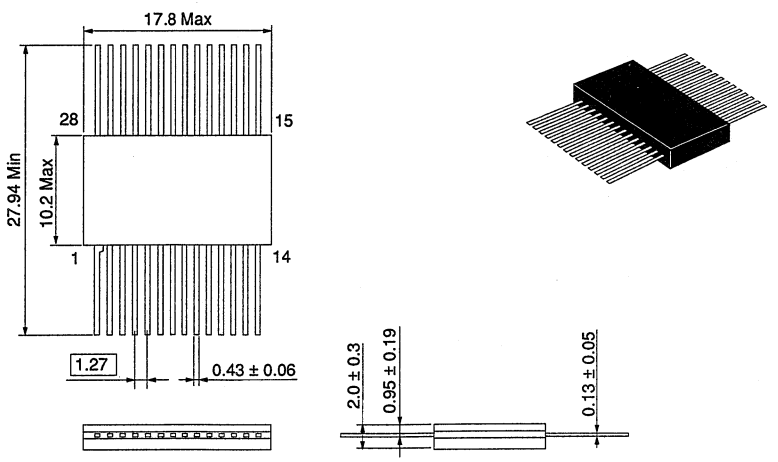
- TTP-44DBR



- FG-24D

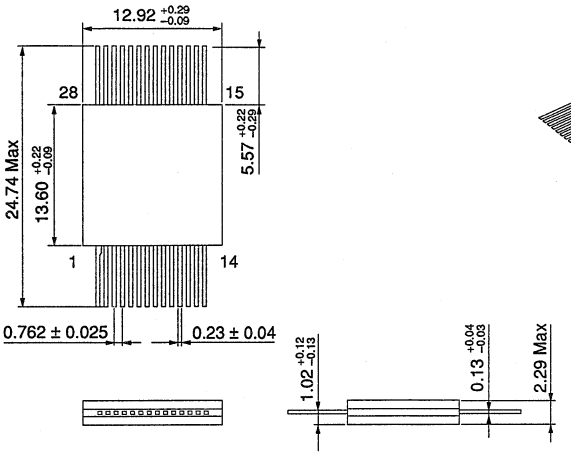


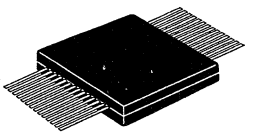
- FG-28D



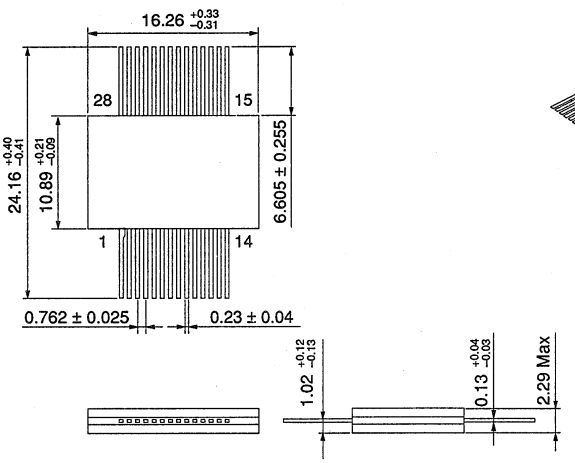
Unit: mm

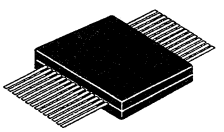
• FG-28DA



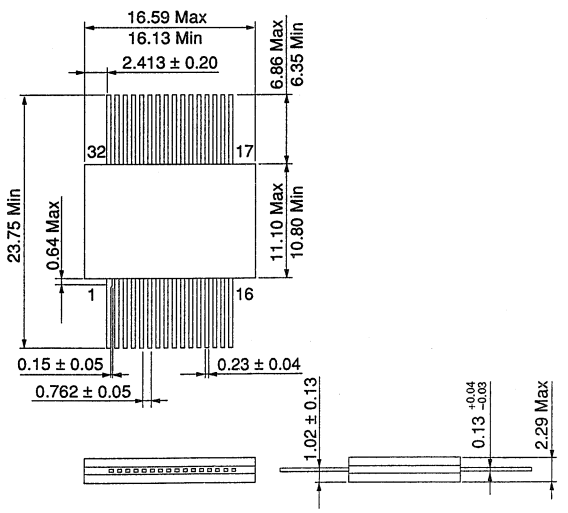


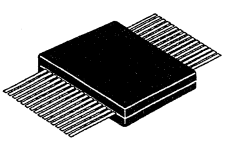
• FG-28DB





• FG-32D





Package Information

Applicable ICs

FP-28D	HM6264AFP Series, HM6264ALFP Series, HM6264ALFP-L Series, HN58C65FP Series, HN58C66FP Series, HN58C256FP Series
FP-28DA	HM6264AFP Series, HM6264ALFP Series, HM6264ALFP-L Series, HM62256FP Series, HM62256LFP Series, HM62256LFP-SL Series, HM62256AFP Series, HM62256ALFP Series, HM62256ALFP-SL Series, HM65256BFP Series, HM65256BLFP Series, HM63021FP Series, HM53051FP Series, HN623257FZ, HN62321F, HN62321BF, HN62331F, HN62321EF, HN58C65FP Series, HN58C66FP Series, HN27C256AFP Series, HN27C256HFP Series
FP-32D	HM628128FP Series, HM628128LFP Series, HM628128LFP-SL Series, HM628512FP Series, HM628512LFP Series, HM628512LFP-SL Series, HM658128ADFP Series, HM658128ALFP Series, HM658128ALFP-L Series, HM658512DFP Series, HM658512LFP Series, HM658512LFP-L Series, HN62321AF, HN62331AF, HN62314BF, HN62334BF, HN62344BF, HN62321GF, HN62302BF, HN62318BF, HN62328BF, HN58C100FP Series, HN29C101BFP Series, HN27C101AFP Series, HN27C301AFP Series, HN28F4001FP Series, HM628128AFP Series, HM628128ALFP Series, HM628128ALFP-SL Series, HM62V8128FP Series, HM62V8128LFP Series, HM62V8128LFP-SL Series, HM629128FP Series, HM629128LFP Series, HM629128LFP-SL Series, HM65V8512DFP Series, HM65V8512LFP Series, HM65V8512LFP-L Series, HN58V1001FP Series, HN58C1001FP Series
FP-44A	HN62412FP, HN62422FP, HN62428FP, HN62418FP, HN62444FP, HN624116FP HN62414FP, HN62434FP
FP-48DA	HN62428F, HN624116F, HN62418F, HN62414, HN62434F, HN62444F
FP-64DS	HM5316123 Series
TFP-20D	HM514256AT Series, HM514256ALT Series, HM514266AT Series, HM511000AT Series, HM511000ALT Series,
TFP-20DR	HM514256AR Series, HM514256ALR Series, HM514266AR Series, HM511000AR Series, HM511000ALR Series,
TFP-20DA	HM514400AT Series, HM514400ALT Series, HM514400ASLT Series, HM514402AT Series, HM514402ALT Series, HM514402ASLT Series, HM514410AT Series, HM514410ALT Series, HM514410ASLT Series, HM514412AT Series, HM514412ALT Series, HM514412ASLT Series, HM514100AT Series, HM514100ALT Series, HM514100ASLT Series, HM514101AT Series, HM514101ALT Series, HM514101ASLT Series, HM514102AT Series, HM514102ALT Series, HM514102ASLT Series
TFP-20DAR	HM514400AR Series, HM514400ALR Series, HM514400ASLR Series, HM514402AR Series, HM514402ALR Series, HM514402ASLR Series, HM514410AR Series, HM514410ALR Series, HM514410ASLR Series, HM514412AR Series, HM514412ALR Series, HM514412ASLR Series, HM514100AR Series, HM514100ALR Series, HM514100ASLR Series, HM514101AR Series, HM514101ALR Series, HM514101ASLR Series, HM514102AR Series, HM514102ALR Series, HM514102ASLR Series

Applicable ICs (cont)

TFP-32D	HM628128T Series, HM628128LT Series, HM628128LT-L Series, HM658128ADT Series, HM658128ALT Series, HM658128ALT-L Series, HN28F4001T Series, HM628128AT Series, HM628128ALT Series, HM628128ALT-L Series, HM629128T Series, HM629128LT Series, HM629128LT-L Series, HM62V8128T Series, HM62V8128LT Series, HM62V8128LT-L Series
TFP-32DR	HM628128R Series, HM628128LR Series, HM628128LR-L Series, HM658128ADR Series, HM658128ALR Series, HM658128ALR-L Series, HN28F4001R Series, HM628128AR Series, HM628128ALR Series, HM628128ALR-L Series, HM629128R Series, HM629128LR Series, HM629128LR-L Series, HM62V8128R Series, HM62V8128LR Series, HM62V8128LR-L Series
TFP-32DA	HM62256ALT Series, HM62256ALT-SL Series, HN58C257T Series, HN58C1000T Series, HN29C101T Series, HN29C101BT Series, HM534251AT Series, HM534253AT Series, HN58V1001T Series, HN58C1001T Series, HN58V257T Series
TFP-32DAR	HM62256ALR Series, HM62256ALR-SL Series, HN58C257R Series, HN58C1000R Series, HN29C101R Series, HN29C101BR Series, HM534251AR Series, HM534253AR Series, HN58V1001R Series, HN58C1001R Series, HN58V257R Series
TTP-20D	HM514400ATT Series, HM514400ALTT Series, HM514400ASLTT Series, HM514402ATT Series, HM514402ALTT Series, HM514402ASLTT Series, HM514410ATT Series, HM514410ALTT Series, HM514410ASLTT Series, HM514412ATT Series, HM514412ALTT Series, HM514412ASLTT Series, HM514100ATT Series, HM514100ALTT Series, HM514100ASLTT Series, HM514101ATT Series, HM514101ALTT Series, HM514101ASLTT Series, HM514102ATT Series, HM514102ALTT Series, HM514102ASLTT Series
TTP-20DR	HM514400ARR Series, HM514400ALRR Series, HM514400ASLRR Series, HM514402ARR Series, HM514402ALRR Series, HM514402ASLRR Series, HM514410ARR Series, HM514410ALRR Series, HM514410ASLRR Series, HM514412ARR Series, HM514412ALRR Series, HM514412ASLRR Series, HM514100ARR Series, HM514100ALRR Series, HM514100ASLRR Series, HM514101ARR Series, HM514101ALRR Series, HM514101ASLRR Series, HM514102ARR Series, HM514102ALRR Series, HM514102ASLRR Series
TTP-24D	HM5116100TT Series, HM5116400TT Series, HM5117400TT Series, HM5116402TT Series, HM5116102TT Series, HM5116101TT Series, HM5116412TT Series, HM5116410TT Series HM5116100RR Series, HM5116400RR Series, HM5117400RR Series, HM5116402RR Series, HM5116102RR Series, HM5116140RR Series, HM5116410RR Series
TTP-28D	HM514800TT Series, HM514800LTT Series, HM514900TT Series, HM514900LTT Series
TTP-28DR	HM514800RR Series, HM514800LRR Series
TTP-32D	HM658512DTT Series, HM658512LTT Series, HM658512LTT-L Series, HN27C101ATT Series, HN27C4001TT Series, HM628512LTT Series, HM628512LTT-SL Series, HM5116800TT Series, HN27V101ATT Series, HM621400P Series, HM621400LP Series, HM624100P Series, HM624100LP Series, HM65V8512DTT Series, HM65V8512LTT Series, HM65V8512LTT-L Series HN62302BTT, HN62314BTT, HN62334BTT, HN62318BTT, HN62328BTT

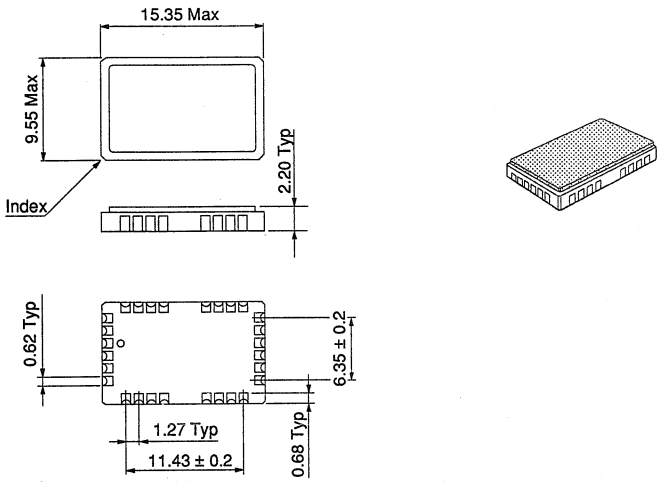
Applicable ICs (cont)

TTP-32DR	HM658512DRR Series, HM658512LRR Series, HM658512LRR-L Series, HN27C101ARR Series, HN27C4001RR Series, HM5116800RR Series, HN27V101ARR Series, HM65V8512DRR Series, HM65V8512LRR Series, HM65V8512LRR-L Series
TTP-40DA	HM538253TT Series
TTP-40DB	HM514260TT Series, HM514260LTT Series, HM514280TT Series, HM514280LTT Series
TTP-40DAR	HM538253RR Series
TTP-44DB	HM5116170TT Series, HM5116190TT Series, HM5116180TT Series, HM5116160TT Series
TTP-44DBR	HM5116170RR Series, HM5116190RR Series, HM5116180RR Series, HM5116160RR Series
FG-24D	HM100500F Series, HM101500F Series
FG-28D	HM101494F Series
FG-28DA	HM100504F Series, HM101504F Series
FG-28DB	HM101510F Series
FG-32D	HM101514F Series, HM101513F Series, HM101515F Series

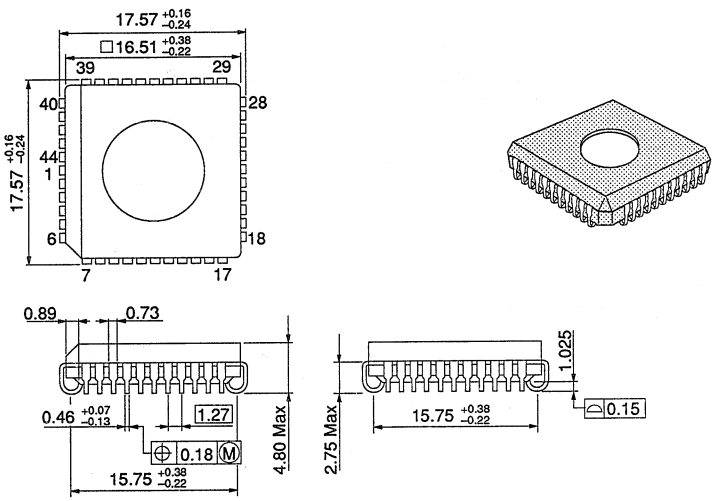
Chip Carrier

Unit: mm

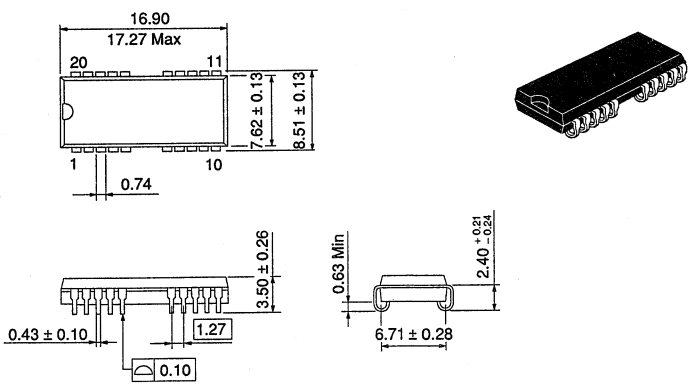
• CG-28B



• CC-44



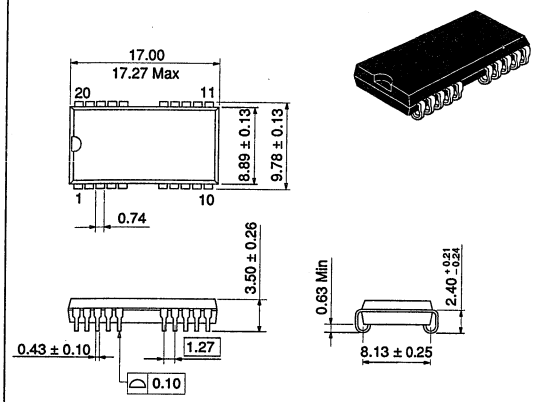
• CP-20D



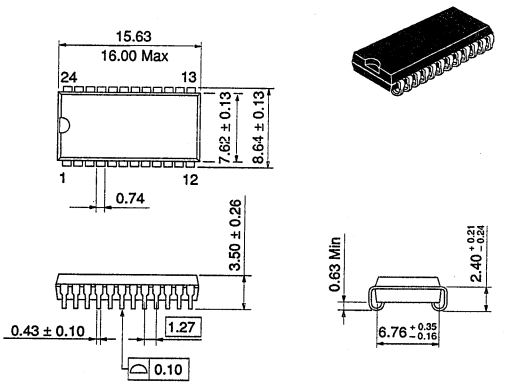
Package Information

Unit: mm

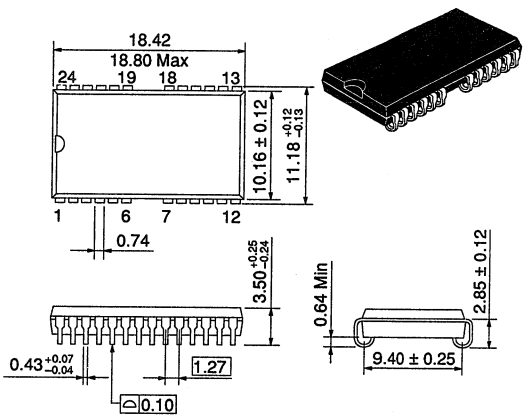
• CP-20DA



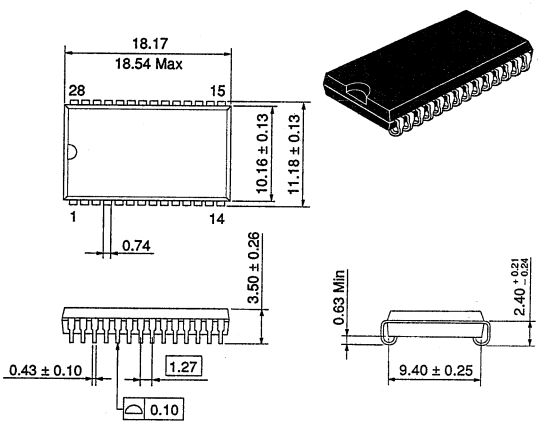
• CP-24D



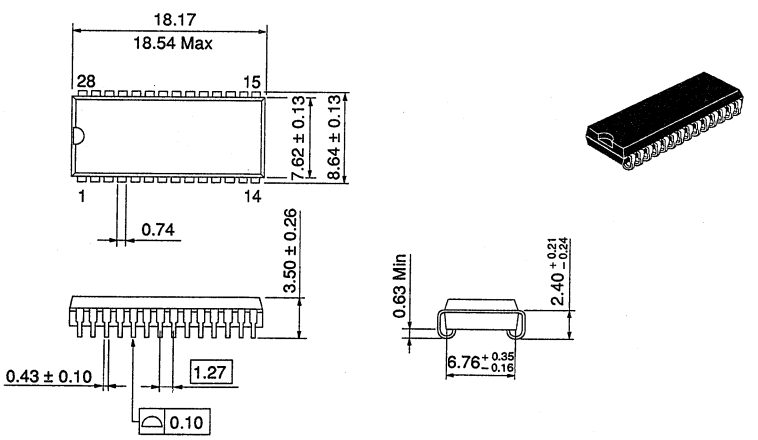
• CP-24DA



• CP-28D

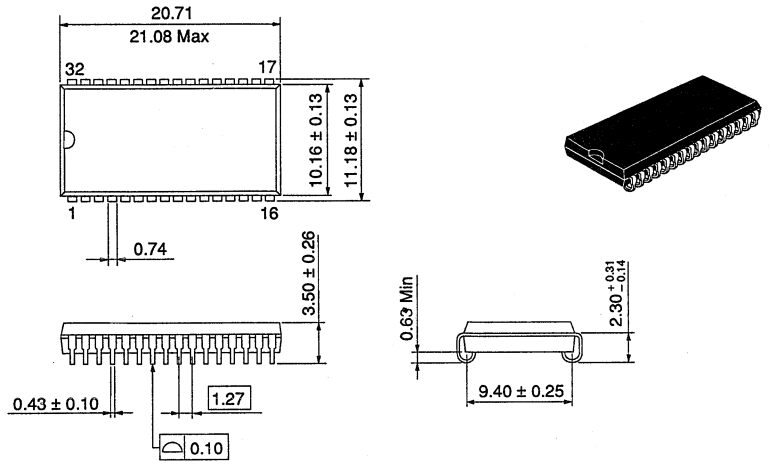


• CP-28DN

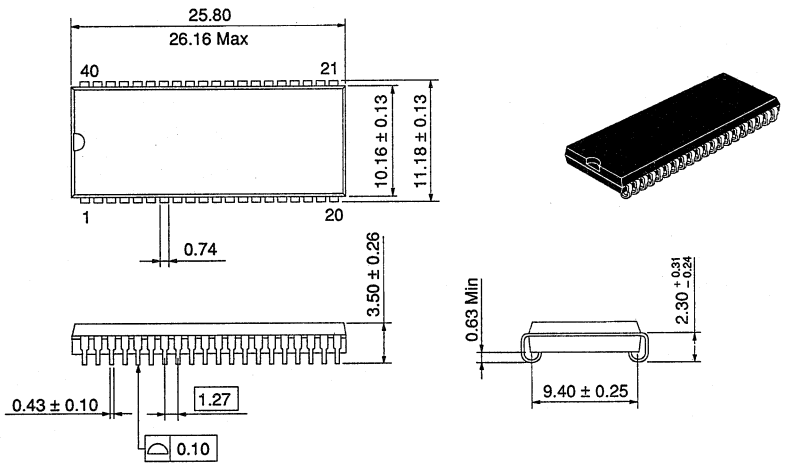


Unit: mm

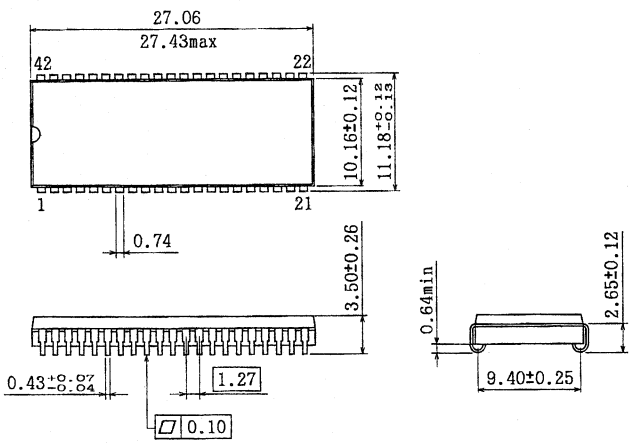
- CP-32D



- CP-40D



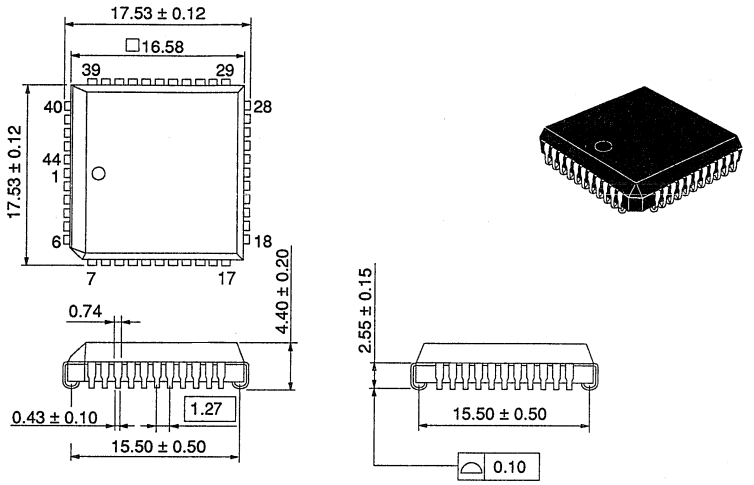
- CP-42D



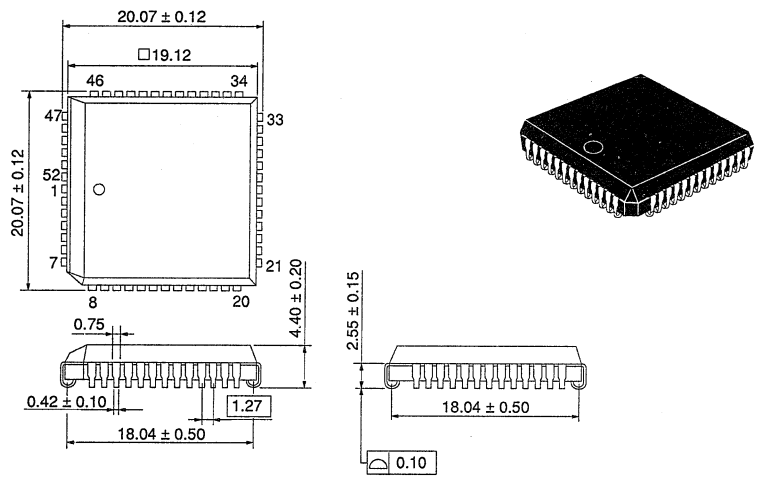
Package Information

Unit: mm

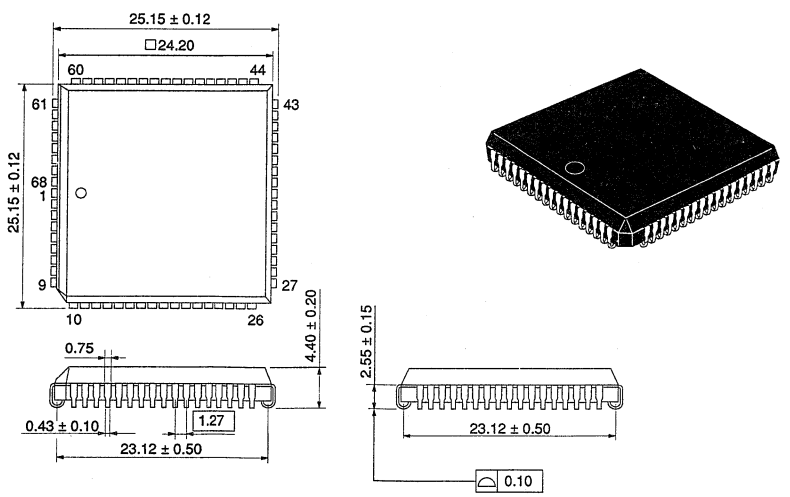
• CP-44



• CP-52



• CP-68



Applicable ICs

CG-28B	HM100500CG Series
CC-44	HM27C1024HCC Series, HN27C4096CC Series, HN27C4096HCC Series
CP-20D	HM514256AJP Series, HM514256ALJP Series, HM514258AJP Series, HM514266AJP Series, HM511000AJP Series, HM511000ALJP Series, HM511001AJP Series, HM511002AJP Series, HM514400AS Series, HM514400ALS Series, HM514400ASLS Series, HM514402AS Series, HM514402ALS Series, HM514402ASLS Series, HM514410AS Series, HM514410ALS Series, HM514410ASLS Series, HM514412AS Series, HM514412ALS Series, HM514412ASLS Series, HM514100AS Series, HM514100ALS Series, HM514100ASLS Series, HM514101AS Series, HM514101ALS Series, HM514101ASLS Series, HM514102AS Series, HM514102ALS Series, HM514102ASLS Series
CP-20DA	HM514400JP Series, HM514400JP Series, HM514400SLJ Series, HM514402JP Series, HM514410JP Series, HM514100JP Series, HM514100LJP Series, HM514100SLJ Series, HM514101JP Series, HM514102JP Series, HM514400AJ Series, HM514400ALJ Series, HM514400ASLJ Series, HM514402AJ Series, HM514402ALJ Series, HM514402ASLJ Series, HM514410AJ Series, HM514410ALJ Series, HM514410ASLJ Series, HM514412AJ Series, HM514412ALJ Series, HM514412ASLJ Series, HM514100AJ Series, HM514100ALJ Series, HM514100ASLJ Series, HM514101AJ Series, HM514101ALJ Series, HM514101ASLJ Series, HM514102AJ Series, HM514102ALJ Series, HM514102ASLJ Series
CP-24D	HM6289JP Series, HM6289LJP Series, HM6789HAJP Series, HM6288JP Series, HM6288LJP Series, HM6287HJP Series, HM6287HLJP Series, HM6208HJP Series, HM6208HLJP Series, HM6708SHJP Series, HM6708AJP Series, HM6207HJP Series, HM6207HLJP Series, HM6707AJP Series, HM53461 Series, HM53462 Series, HM101490JP Series
CP-24DA	HM5116100JP Series, HM5116400JP Series, HM5117400J Series, HM5116402J Series, HM5116102J Series, HM5116101J Series, HM5116412J Series, HM5116410J Series
CP-28D	HM624256JP Series, HM624256LJP Series, HM624256AJP Series, HM624256ALJP Series, HM621100AJP Series, HM621100ALJP Series, HM534251JP Series, HM534252JP Series, HM534251AJ Series, HM534253AJ Series, HM514800JP Series, HM514800LJP Series, HM514900JP Series, HM514900LJP Series
CP-28DN	HM62832HJP Series, HM62832HLJP Series, HM62832UHJP Series, HM62832UHLJP Series, HM67832SHJP Series, HM6709AJP Series, HM6209SHJP Series, HM63921JP Series, HM100494JP Series, HM101494JP Series, HM574256JP Series, HM571000JP Series
CP-32D	HM624257JP Series, HM624257LJP Series, HM624257AJP Series, HM5116800J Series, HM624257ALJP Series, HM100504JP Series, HM101504JP Series, HM621400JP Series, HM621400JLP Series, HM624100JP Series, HM624100LJP Series, HM62A9128JP Series, HM62A8128JP Series

Applicable ICs (cont)

CP-40D	HM538253J Series, HM538121JP Series, HM538122JP Series, HM538121AJ Series, HM538123AJ Series, HM511664JP Series, HM511665JP Series, HM514280JP Series, HM514280LJP Series, HM514260JP Series, HM514260LJP Series, HM514170JP Series, HM514170LJP Series, HM514190JP Series, HM514190LJP Series, HM511666J Series, HM511666LJ Series
CP-42D	HM5116170J Series, HM5116190J Series, HM5116180J Series, HM5116160J Series
CP-44	HM67B932CP Series, HN27C1024HCP Series, HN27C4096CP Series HN62444BCP, HN62442BCP
CP-52	HM62A168CP Series, HM62A188CP Series, HM62B168CP Series, HM62B188CP Series, HM62A2016CP Series
CP-68	HM62A2017CP Series

Reliability of Hitachi IC Memories

1. Structure

IC memory devices are classified as NMOS type, CMOS type, and Bi-CMOS type. There are advantages to it's circuit design, layout pattern, degree of integration, and manufacturing process.

All Hitachi memories are produced using standardized design, manufacturing, and inspection techniques. Reliability, a key factor in Hitachi IC design and usage, is enhanced by Test Element Group (TEG) evaluation. This approach ensures the best possible application of our experience and knowledge at every step of IC development.

IC memories consist of memory cells which are circuit patterns arranged within a device at very high density. Examples of memory cell circuitry of MOS memories are shown in Table 1.

The dies of IC memories are encapsulated in various packages. The most common packages are plastic and cerdip. Plastic packages are widely used in many different types of equipment. Cerdip packaging is especially suitable in equipment requiring high reliability. Surface mount packages, such as the plastic leaded chip carrier (PLCC) and small outline package (SOP) have been developed for high density applications.

Hitachi has developed new techniques of IC packaging, thus achieving high levels of reliability. Hitachi plastic IC packages have been improved to match the performance of other hermetically sealed packages.

Table 2 illustrates the appearance and relative sizes of various Hitachi IC packages.

Table 1 Basic Memory Cell Circuit of IC Memories

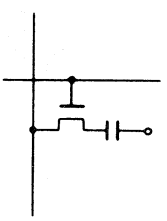
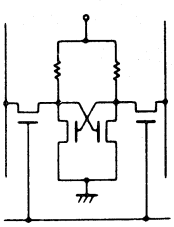
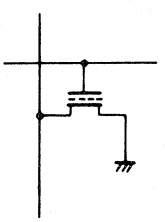
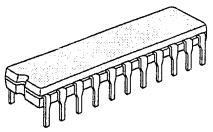
Classification	Dynamic RAM	Static RAM	EPROM
Example of basic cell circuit			

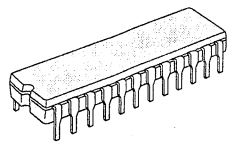
Table 2 IC Memory Package Outline

■ Cerdip

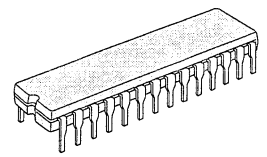
● 22 pin



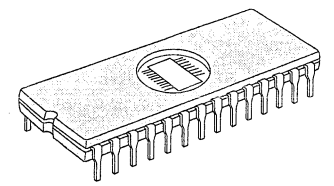
● 24 pin



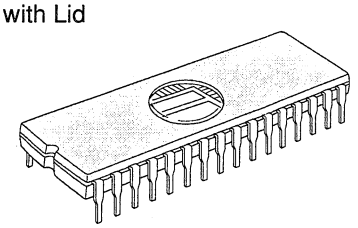
● 28 pin



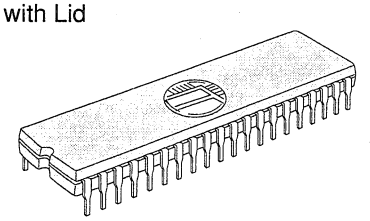
● 28 pin with Lid



● 32 pin with Lid

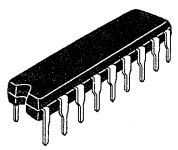


● 40 pin with Lid

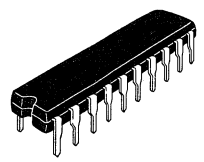


■ Plastic DIP

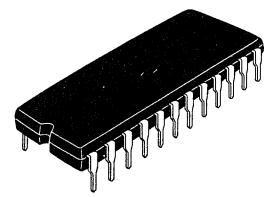
● 18 pin



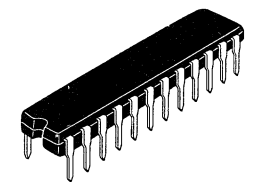
● 20 pin



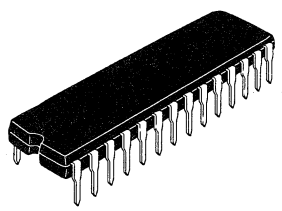
● 24 pin



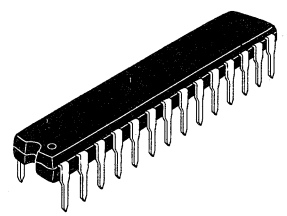
● 24 pin



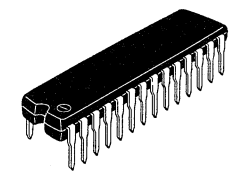
● 28 pin



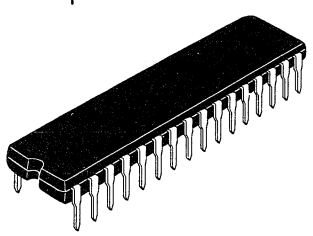
● 28 pin



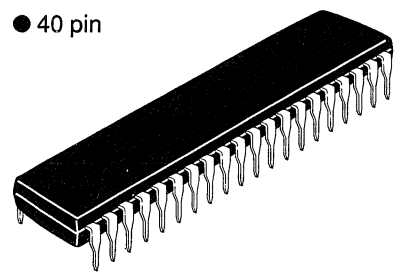
● 28 pin



● 32 pin



● 40 pin



● 42 pin

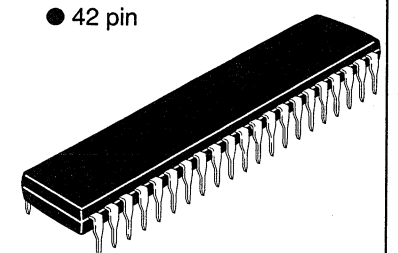
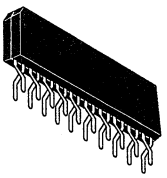


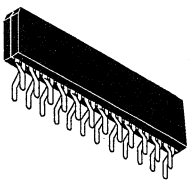
Table 2 IC Memory Package Outline (cont)

■ Zigzag-in-line Plastic

● 20 pin



● 24 pin



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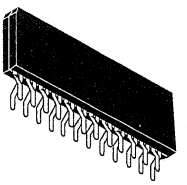
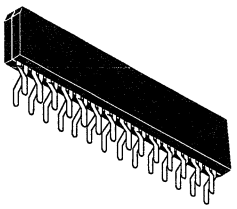
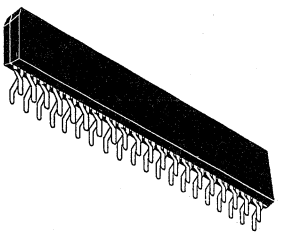


● 28 pin

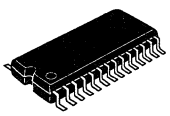


● 40 pin

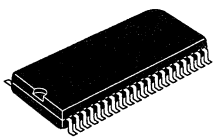


■ SOP

● 28/32 pin



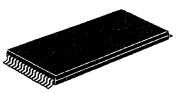
● 44 pin



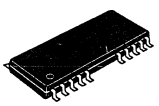
● 48 pin

● 20 pin

● 32 pin



● 20 pin



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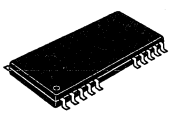
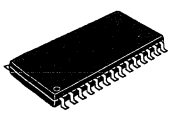
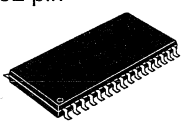


● 28 pin

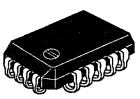


● 32 pin

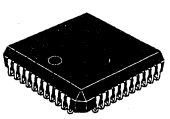


■ PLCC

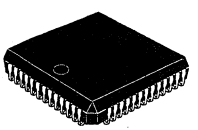
● 18 pin



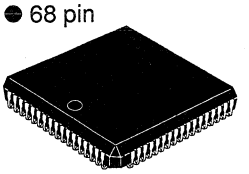
● 44 pin



● 52 pin

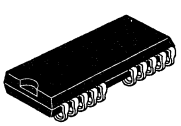


● 68 pin

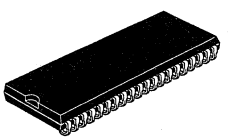


■ SOJ

● 20/26/28/32 pin



● 40 pin



2. Reliability

Hitachi IC memory reliability test results are listed below.

2.1 Reliability Test Data of Hi-BiCMOS Memory

Hi-BiCMOS memory is a recently developed design, based on the latest fine process technologies. Hi-BiCMOS memory offers a combination of the best features of other, earlier devices—the low power consumption and high integrity of CMOS devices, plus the high speed and high drive capability of bipolar (ECL) circuits. Hi-BiCMOS memory also supports the input and output levels of both ECL and TTL devices, which allows interfacing with other devices.
The reliability test data for HM101510F-15 (1M × 1 bit) and HM6708AJP-20 (64k × 4 bits) is listed in Tables 3 and 4.

In normal use, Hi-BiCMOS memory reliability is affected by some limitations based on the circuit composition. Besides the normal constraints of CMOS and bipolar device design, Hi-BiCMOS memory should not be used in applications involving deformed or slow signal waveforms that may cause latch-up or other malfunctions. For further information, refer to the detailed specifications on the data sheet for each Hi-BiCMOS device.

Table 3 Results of Hi-BiCMOS Memory Reliability Tests (1)

	HM101510F-15 (FPG)					HM6708AJP-20 (SOJ)					
Test Item	Test Condition	Samples	Total Test Time	Failures	Failure Rate	Test Item	Test Condition	Samples	Total Test Time	Failures	Failure Rate	Remarks
High-temperature pulse operation	Ta = 125°C V_{EE} = –5.2V	328	C.H. 3.28×10^5	0	1/h 3.3×10^{-6}	High-temperature pulse operation	Ta = 125°C V_{CC} = 7.0V	380	C.H. 3.8×10^5	1*	1/h 5.3×10^{-6}	* foreign matter
	Ta = 100°C V_{EE} = –7.0V	32	C.H. 3.2×10^4	0	1/h 2.9×10^{-5}	Moisture endurance	85°C 85% RH 5V	210	2.1×10^5	0	4.4×10^{-6}	
High-temperature storage	Ta = 200°C	235	2.35×10^5	0	3.9×10^{-6}	Pressure cooker	121°C 100% RH	80	0.16×10^5	0	5.8×10^{-5}	

Table 4 Results of Hi-BiCMOS Memory Reliability Tests (2)

		HM101510F-15 (FPG)		HM6708AJP-20 (SOJ)	
Test Item	Test Condition	Samples	Failures	Samples	Failures
Temperature cycling	–55° to +150°C, 100 cycles	180	0	180	0
Soldering heat	260°C, 10 seconds	22	0	22	0
Thermal shock	0° to +100°C, 10 cycles	50	0	50	0
Mechanical shock	1500 G, 0.5 ms, three times each for X, Y, and Z axes	22	0	—	—
Variable frequency vibration	100 to 200 Hz, 20 G, three times each for X, Y, and Z axes	22	0	—	—
Constant acceleration	20000 G, 1 minute, each for X, Y, and Z axes	22	0	—	—

2.2 Reliability Test Data of MOS Memory

2.2.1 MOS DRAM and SRAM Tests

Tables 5, 6, and 7 show the reliability test data on 1-Mbit DRAMs (HM511000, HM514256), 4-Mbit DRAMs (HM514100/HM514400), 256-kbit SRAM (HM62256), and 1-Mbit SRAM (HM628128FP). The life test is performed at high temperature and high voltage to evaluate product reliability using many samples. For all failures identified in the manufacturing process, the data is analyzed in great detail to improve the quality and reliability of both the process and the finished product.

Table 5 Reliability Data on 1M MOS DRAM

		HM511000P/HM514256P Series (DIP)				HM511000JP/HM514256JP Series (SOJ)				
Test Item	Test Condition	Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	Remarks
High-temperature operation	125°C/5.5 V	300	6.00×10^{5}	0	1.53×10^{-6}	200	4.00×10^{5}	0	2.30×10^{-6}	* Oxide film failure ×1
	125°C/7 V	1252	4.50×10^{5}	1*	4.49×10^{-6}	3186	9.34×10^{5}	0	9.85×10^{-7}	
	150°C/7 V	200	4.00×10^{5}	0	2.30×10^{-6}	200	4.00×10^{5}	0	2.30×10^{-6}	
Moisture endurance	85°C 85% RH 5.5 V	420	8.40×10^{5}	0	1.10×10^{-6}	682	1.36×10^{6}	0	6.74×10^{-7}	
Pressure cooker	121°C/100% RH	150	4.50×10^{4}	0	2.04×10^{-5}	200	6.00×10^{4}	0	1.53×10^{-5}	

Note: Confidence level 60%

		HM511000ZP/HM514256ZP Series (ZIP)				HM511000ATS/HM514256ATS Series (TSOP)				
Test Item	Test Condition	Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	Remarks
High-temperature operation	125°C/5.5 V	300	6.0×10^{5}	0	1.53×10^{-6}	—	—	—	—	
	125°C/7 V	4368	6.0×10^{5}	0	1.53×10^{-6}	1100	1.5×10^{5}	0	6.22×10^{-6}	
	150°C/7 V	180	3.6×10^{5}	0	2.56×10^{-6}	—	—	—	—	
Moisture endurance	85°C 85% RH 5.5 V	426	8.5×10^{5}	0	1.08×10^{-6}	200	2.0×10^{5}	0	4.60×10^{-6}	
Pressure cooker	121°C/100% RH	125	3.7×10^{4}	0	2.70×10^{-5}	100	3.0×10^{4}	0	3.07×10^{-5}	

Note: Confidence level 60%

Table 6 Reliability Data on 4M DRAM

Test Item	Test Condition	HM514100AS/HM514400AS Series (SOJ) Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	HM514100AZ/HM514400AZ Series (ZIP) Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	Remarks
High-temperature operation	125°C/5.5 V	823	8.2×10^5	0	1.12×10^{-6}	—	—	—	—	*
	125°C/7 V	2514	8.3×10^5	1*	2.43×10^{-6}	1100	1.5×10^5	0	6.22×10^{-6}	Oxide film failure ×1
	150°C/7 V	151	1.5×10^5	0	6.09×10^{-6}	—	—	—	—	
Moisture endurance	85°C 85% RH 5.5 V	317	3.2×10^5	0	2.90×10^{-6}	300	3×10^5	0	3.07×10^{-6}	
Pressure cooker	121°C/100% RH	100	3×10^4	0	3.07×10^{-5}	100	3×10^4	0	3.07×10^{-5}	

Note: Confidence level 60%

Test Item	Test Condition	HM514100AT/HM514400AT Series (TSOP) Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	HM5116100/HM5116400 Series (SOJ) Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	Remarks
High-temperature operation	125°C/5.5 V	—	—	—	—	—	—	—	—	
	125°C/7 V	1100	1.5×10^5	0	6.22×10^{-6}	4146	2.0×10^5	0	5.02×10^{-6}	
	150°C/7 V	—	—	—	—	—	—	—	—	
Moisture endurance	85°C 85% RH 5.5 V	300	3.0×10^5	0	3.07×10^{-6}	156	1.56×10^5	0	6.41×10^{-6}	
Pressure cooker	121°C/100% RH	100	3.0×10^4	0	3.07×10^{-5}	130	3.9×10^4	0	2.56×10^{-5}	

Note: Confidence level 60%

Table 7 Reliability Data on 256k and 1M MOS SRAM

Test Item	Test Condition	HM62256FP (SOP) Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	HM628128FP (SOP) Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	Remarks
High-temperature operation	125°C/5.5 V	3088	3.11×10^6	0	2.96×10^{-7}	1946	1.08×10^6	0	8.52×10^{-7}	*1
	125°C/7 V	455	4.55×10^5	0	2.02×10^{-6}	1096	6.78×10^5	1*1	2.98×10^{-6}	Foreign ×2
	150°C/7 V	103	1.00×10^5	1*1	2.02×10^{-5}	125	2.05×10^5	0	4.49×10^{-6}	
Moisture endurance	85°C/85% RH 7 V	680	6.80×10^5	0	1.35×10^{-6}	287	4.14×10^5	0	2.22×10^{-6}	*2 Leak ×1
Pressure cooker	121°C/100% RH	320	6.40×10^4	1*2	3.16×10^{-5}	150	3.90×10^4	0	2.36×10^{-5}	

Note: Confidence level 60%

2.2.2 Reliability Test Data on EPROM

There are two types of EPROM: the conventional EPROM with a transparent window over the active device area; and the one-time-programmable ROM (OTPROM) packaged in plastic. Table 8 shows the reliability test data on the 512-kbit EPROM (HN27512, HN27512P) and 1-Mbit EPROM (HN27C101, HN27C301).

The high temperature failures shown in Table 8 are due to data dissipation in the memory cells. By absorbing thermal energy, the electrons in the floating gates are activated and dissipated. In actual usage, however, this is not a significant problem since this phenomenon is highly dependent on temperature (about 1.0 eV of activated energy) that should not appear during normal operation.

The moisture resistance of the OTPROM is satisfactory.

Table 9 shows an example of PROM derating. The primary derating parameter is generally temperature since other operating parameters are specified. The maintaining of low junction temperature during device mounting is especially important for a stable application operation (relative to access time, refresh time, and other characteristics).

Table 8 Reliability Data on 512-kbit and 1-Mbit MOS EPROMs

		HN27512 (Cerdip/Plastic)				HN27C101/HN27C301 (Cerdip)				
Test Item	Test Condition	Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	Remarks
High-temperature operation	125°C/5.5 V	240	4.52×10^5	0	2.03×10^{-6}	220	4.18×10^5	0	2.20×10^{-6}	* Data dissipation×49
	125°C/7 V	570	9.55×10^5	0	0.96×10^{-6}	445	8.45×10^5	0	1.09×10^{-6}	
High-temperature bake	175°C	290	5.51×10^5	0	1.67×10^{-6}	180	9.0×10^5	0	1.02×10^{-6}	
	200°C	260	4.02×10^5	1*	5.02×10^{-6}	130	6.49×10^5	1*	3.11×10^{-6}	
	250°C	200	2.09×10^5	8*	4.51×10^{-5}	110	3.07×10^5	40*	1.30×10^{-4}	
Moisture endurance	85°C/85% RH 5.5 V	300	5.42×10^5	0	1.70×10^{-6}	—	—	—	—	Data of 512k OTPROM
Pressure cooker	121°C/100% RH	50	0.10×10^5	0	9.20×10^{-5}	—	—	—	—	

Note: Confidence level 60%

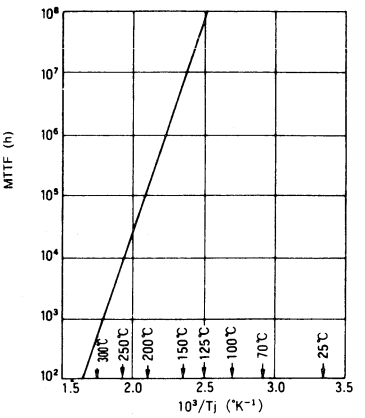
2.2.3 Reliability Test Data on MASK ROM

Table 10 shows the reliability test data for the 16-Mbit and 8-Mbit MASK ROMs. The MASK ROM is patterned in the manufacturing process, so data dissipation is not generated during high temperature operations, unlike EPROM and EEPROM devices.

Table 9 Example of HN27C101/HN27C301 Derating

Factor	Temperature
Failure criteria	Electrical characteristics, function test
Failure mechanism	Increase of leakage current, and others

Results:
The result of high temperature baking of the PROM is shown in the figure at right.



Note: As shown in the figure, decreasing junction temperature will improve reliability. The junction temperature can be calculated by the formula: Tj = Ta + θja · Pd where θja is about 100°C/W with no air flow and about 60° to 70°C/W with 2.5 m/s air flow.

Table 10 Reliability Data on 16-Mbit and 8-Mbit MASK ROMs

		HN624016P (Plastic)				HN62408P (Plastic)				
Test Item	Test Condition	Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	Remarks
High-temperature operation	125°C/5.5 V	140	1.4×10^5	0	6.6×10^{-6}	200	4.0×10^5	0	2.3×10^{-6}	
	125°C/7 V	100	1.0×10^5	0	9.2×10^{-6}	130	1.3×10^5	0	7.1×10^{-6}	
Moisture endurance	85°C/85% RH 5.5 V	100	1.0×10^5	0	9.2×10^{-6}	150	1.5×10^5	0	6.1×10^{-6}	
Pressure cooker	121°C/100% RH	60	3.0×10^4	0	3.1×10^{-5}	90	4.5×10^4	0	2.0×10^{-5}	

Note: Confidence level 60%

2.2.4 Reliability Test Data on MOS Memory (environmental testing)

Tables 11 and 12 list MOS memory environmental test data, showing excellent results without any failures, even in severe environments.

In MOS transistor operations, V_{TH} is a basic process parameter. While in use, MOS memory exhibits almost no change in V_{TH}, largely due to designed-in surface stabilization technology and extremely clean production processes.

Figure 3 shows examples of time dependent degradation for minimum V_{CC} and access time t_{RAC} for 4-Mbit DRAM under high temperature operation test conditions.

2.3 Change of Electrical Characteristics on IC Memories

The degradation of I_{CBO} and h_{FE} are the main factors of performance degradation for inner cell transistors in bipolar memory. The actual element design, however, specifies the operation in a range at which no degradation occurs. In this normal situation, no changes in the operating characteristics, including access time, will arise. Time dependencies in the access time for the HM100500 and HM6708P are shown in Figures 1 and 2.

Table 11 Reliability Data on MOS Memory (1)

		HM511000P (DIP)		HM511000JP (SOJ)		HM511000ZP (ZIP)		HM511000ATS (TSOP)		HM62256FP (SOP)		HM628128FP (SOP)		EPROM (Cerdip)	
Test Item	Test Condition	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures
Temperature cycling	–55° to 150°C 10 cycles	3755	0	2786	0	1500	0	900	0	3328	0	1215	0	2850	0
Temperature cycling	–55° to 150°C 500 cycles	150	0	200	0	175	0	250	0	482	0	210	0	520	0
Thermal shock	–65° to 150°C 15 cycles	77	0	100	0	50	0	22	0	76	0	77	0	100	0
Soldering heat	260°C, 10 sec	22	0	22	0	22	0	22	0	22	0	35	0	22	0
Mechanical shock	1500 G, 0.5 ms	—	—	—	—	—	—	—	—	—	—	—	—	38	0
Variable frequency vibration	100 to 2000 Hz 20 G	—	—	—	—	—	—	—	—	—	—	—	—	38	0
Constant acceleration	6000 G	—	—	—	—	—	—	—	—	—	—	—	—	38	0

Table 12 Reliability Data on MOS Memory (2)

		HM514400AS (SOJ)		HM514400AZ (ZIP)		HM5116400J (SOJ)		HM514400AT (TSOP)		HN624016P (DIP)		HN62408P (DIP)		
Test Item	Test Condition	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	Remarks
Temperature cycling	–55° to 150°C 10 cycles	949	0	1000	0	1280	0	900	0	330	0	370	0	
Temperature cycling	–55° to 150°C 500 cycles	200	0	200	0	141	0	100	0	70	0	12	0	
Thermal shock	–65° to 150°C 15 cycles	22	0	22	0	32	0	22	0	22	0	22	0	
Soldering heat	260°C, 10 sec	22	0	600	0	22	0	22	0	22	0	22	0	

Example	
Device name	HM101510F-15
Test condition	Ta = 125°C, V_{EE} = –5.2 V all bit scanning
Failure criteria	t_{AA} = 15 ns
Failure mechanism	Surface degradation

Results:
Access time is stabilized.

Example of Time Dependent Degradation in Access Time for Hi-BiCMOS Memory

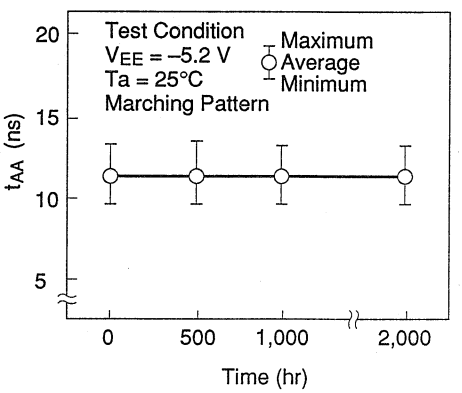


Figure 1 Time Dependent Degradation in Access Time for Hi-BiCMOS Memory

Example	
Device name	HM6708AJP-20
Test condition	Ta = 125°C, V_{CC} = 7.0 V all bit scanning
Failure criteria	V_{CC} = 4.5 V, t_{AA} = 25 ns
Failure mechanism	Surface degradation

Results:
Both V_{CC} (min) and t_{AA} are stabilized.

Examples of Time Dependent Degradation in V_{CC} min and t_{AA} for Hi-BiCMOS Memory

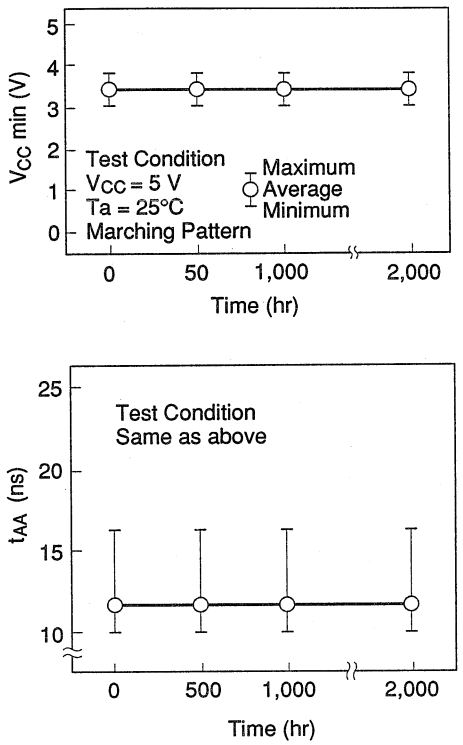


Figure 2 Time Dependent Degradation in Minimum V_{CC} and t_{AA} for Hi-BiCMOS Memory

Example	
Device name	HM514400AS
Test condition	Ta = 125°C, V_{CC} = 7 V all bit scanning
Failure criteria	ΔV_{CC} = 1.0 V, Δt_{RAC} = 6 ns
Failure mechanism	Surface degradation

Results:
V_{CC} margin and access time (t_{AA}) are stabilized and are within the failure criteria.

Note: Test accuracy is 0.2 V, 2 ns.

Example of Time Dependent Degradation in V_{CC} min and t_{RAC} for MOS Memory

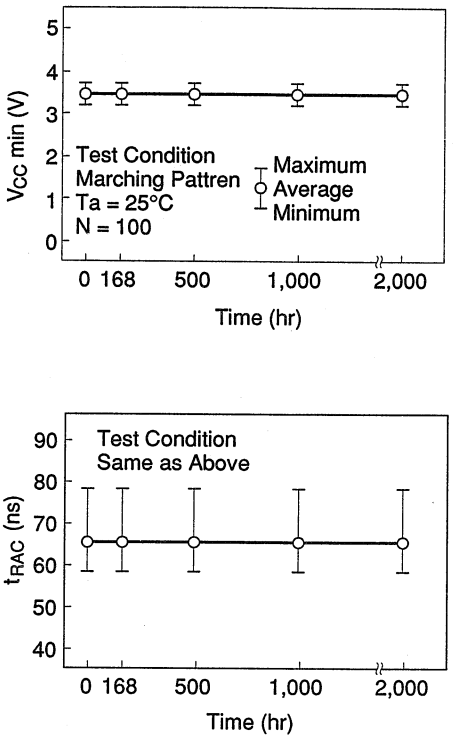


Figure 3 Time Dependent Degradation in Minimum V_{CC} and t_{RAC} for MOS Memory

2.4 Failure Mode Rate

Figures 4 and 5 show examples of failure modes identified in user applications. Since IC memories require the finest pattern process technology, the percentage of failures due to factors such as pinholes, photoresist defects, and foreign materials tends to increase along with product complexity. Hitachi has continued to improve its fabrication process technology, and performs 100% high temperature "burn-in" screening as a standard part of manufacturing.

Hitachi collects and analyzes customer usage data as part of a program designed to achieve higher product reliability. This analysis is a very useful feature of the program.

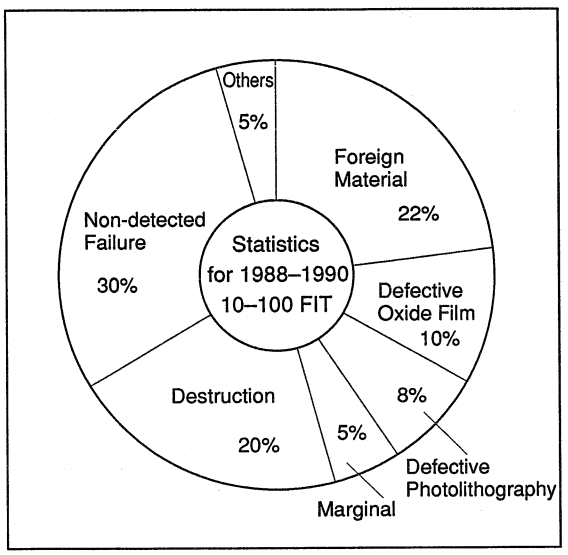


Figure 4 Failure Mode Rates for Hi-BiCMOSMemory

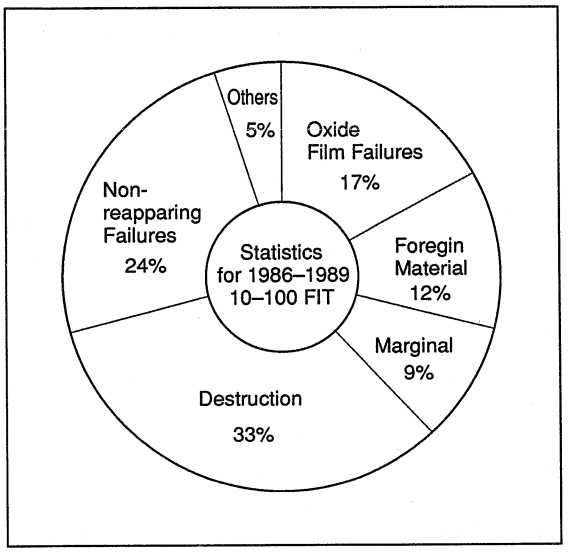


Figure 5 Failure Mode Rates for MOS Memory

3. Reliability of Semiconductor Devices

3.1 Reliability Characteristics for Semiconductor Devices

Hitachi semiconductor devices are designed, manufactured, and inspected to achieve a high level of reliability. System reliability is improved by combining highly reliable components with the proper environmental conditions. This section describes the reliability characteristics, failure types, and their mechanisms in terms of devices. First, the semiconductor device characteristics are examined in light of their reliability.

1. Semiconductor devices are essentially structure sensitive as seen in surface phenomena. Fabricating devices requires precise control of a large number of process steps.

2. Device reliability is partly governed by electrode materials and package materials, as well as by the coordination of these materials with the device materials.

3. Devices employ thin-film and fine-processing techniques for metallization and bonding. Fine materials and thin-film surfaces sometimes exhibit different physical characteristics from the bulk quantities of identical materials.

4. Semiconductor device technology advances very quickly, and therefore many new devices have been developed using new processes over a short period of time. Hence, conventional device reliability data cannot always be used for comparisons.

5. Semiconductor devices are characterized by volume production. Therefore, manufacturing variation is an important consideration.

6. Initial and accidental failures are only considered to be semiconductor device failures based on the fact that semiconductor devices are essentially semipermanently operable. However, failures caused by worn or aged materials and migration should also be reviewed when electrode and package materials are not suited for particular environmental conditions.

7. Component reliability may depend on the device mounting, conditions used, and environment. Device reliability is affected by such factors as voltage, electric field strength, current density, temperature, humidity, gas, dust, mechanical stress, vibration, mechanical shock, and radiation magnetic field strength. Device reliability is generally represented by a failure rate. "Failure" implies that a device has lost its function, and includes intermittent degradation or complete destruction.

   Generally, the failure rate of electrical components and equipment is represented by the "bathtub" curve as shown in Figure 6. For semiconductor devices, the configuration parameter of the Weibull distribution is smaller than 1, which indicates an initial failure type. Such devices ensure a long lifetime unless extreme environmental stress is applied. Therefore, initial and accidental failures can become a problem for semiconductor devices. Semiconductor device reliability can be represented physically as well as statistically. Both failure aspects have been thoroughly analyzed to establish a high level of reliability.

3.2 Failure Types and Their Mechanisms

3.2.1 Failure Physics

Failure physics is, in a broad sense, a basic technology of "physics + engineering." It is used to examine the physical mechanism of failures, in terms of atoms and molecules, to improve device reliability. This physical approach was introduced to the reliability field to answer the demand for minimized developmental cost and time. These conditions were derived from the development of solid-state physics (semiconductor physics) since the 1940's and from other associated device development. Failure physics has been employed to do the following:

1. Detect failed devices as soon as possible.
2. Establish models and equations used for failure prediction.
3. Evaluate the reliability in short time periods by accelerated life testing.

The purpose of the failure physics approach is to contribute to reliability related fields such as product design, prediction, test, storage, and usage, by including physics as a basic technology to conventional experimental and statistical approaches.

3.2.2 Failure Types and Their Mechanisms

The physical aspects of device failures are covered in this section. Semiconductor device failures are basically categorized as open, short circuit, deterioration, and miscellaneous failures. These failures and their causes are summarized in Table 13. Typical failure mechanisms are as follows:

1. Surface deterioration

The pn junction has a charge density of 10^{14} to 10^{20} cm^{-3}. If charges exceeding the above density are accumulated on the pn junction surface, the electrical characteristics of the junction will tend to vary. Although the surface of such devices as planar transistors is generally covered with a SiO_2 film and is in an inactive state, the possibility of deterioration caused by the surface channels still exists. Surface deterioration depends heavily on the applied temperature and voltage and is often handled by the reaction model.

An example of a recent failure is the surface deterioration caused by hot carriers. Hot carriers are generated when such devices as MOS dynamic RAMs are operated at a voltage near the minimum breakdown voltage BV_{DS}, thus raising the internal voltage and establishing a strong electric field near the drain of the MOS device. This may be a result from reduced device geometry (from 2 μm to 0.8 μm) as technological advances have occurred in production methods. Generated hot carriers may affect the surface boundary characteristics on a section of the gate oxide film, resulting in the degradation of the threshold voltage (V_{TH}) and counter conductance (gm). Hitachi devices have consistently employed improved designs and process techniques to prevent these problems. However, as processes become even finer, surface deterioration may become a serious problem.

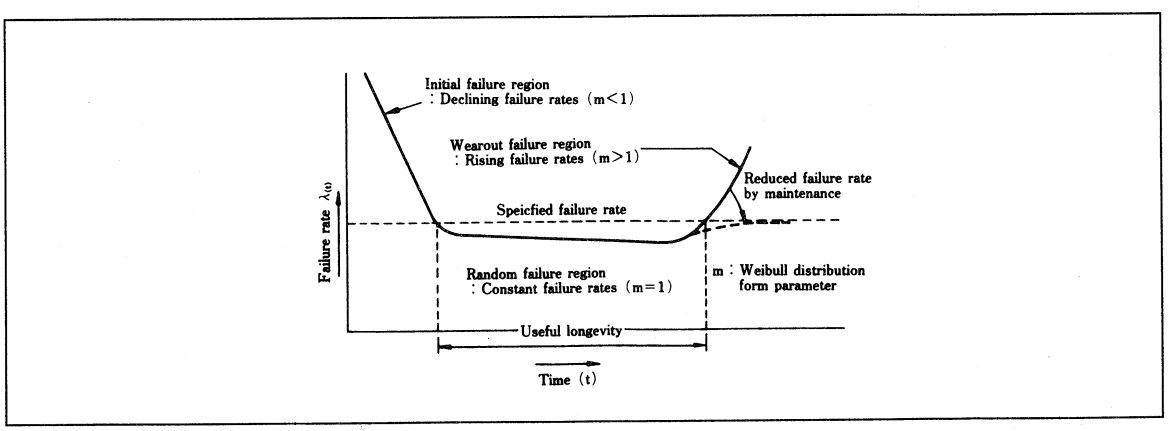


Figure 6 Typical Failure Rate Curve

2. Electrode-related failures

The concern for electrode-related failures has increased as multilayer metallization has become more complex. Noticeable failures include electromigration and Al metallization corrosion in plastic sealed packages.

a. Electromigration

This phenomenon takes place when metal atoms are moved by a large current of about 10^6 A/cm^2 that is supplied to the metal. When ionized atoms collide with the current of electrons, an "electron wind" is produced. This wind moves the metal atoms in the opposite direction from the current flow, which generates voids at a negative electrode, and hillock and whiskers at the opposite side. The generated voids increase wiring resistance and cause excessive currents to flow in some areas, leading to disconnection. The generated whiskers may cause short circuits in multimetal lines.

b. Multimetal line related failures

Major failures associated with multimetal lines include increased leakage currents, short circuits caused by a failed dielectric interlayer, and increased contact metal resistance and disconnection between metal wirings.

c. Al line corrosion and disconnection

When plastic encapsulated devices are subjected to high temperatures, high humidity, or a bias-applied condition, the Al electrodes in the devices can cause corrosion or disconnection (Figure 7). Under high temperature and high humidity, corrosion is randomly generated over the element surface.

However, after an extended period of time, such corrosion does not significantly increase. This type of failure is possibly due to initial failures associated with manufacturing variances. It is also known that such failures can be generated when the adhesion surface between an element and resin is separated or when foreign materials are attached to the element with human saliva. Under a bias-applied, high temperature, high humidity condition, on the other hand, pit corrosion is generated in higher potential areas while in lower potential areas, intergranular corrosion occurs. Once this failure occurs in part of a device, the device can become worn out in a relatively short time. This failure proves to depend on the hydroscopic volume resistivity of sealed resin. The Al line corrosion mechanism described above is summarized in Figure 8.

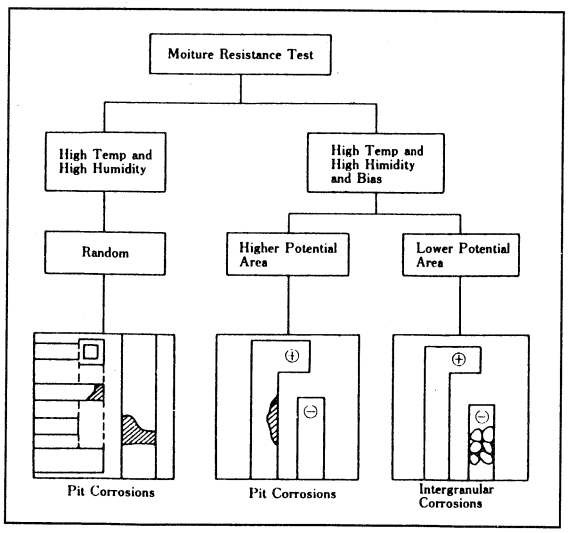


Figure 7 Categorized Al Corrosions

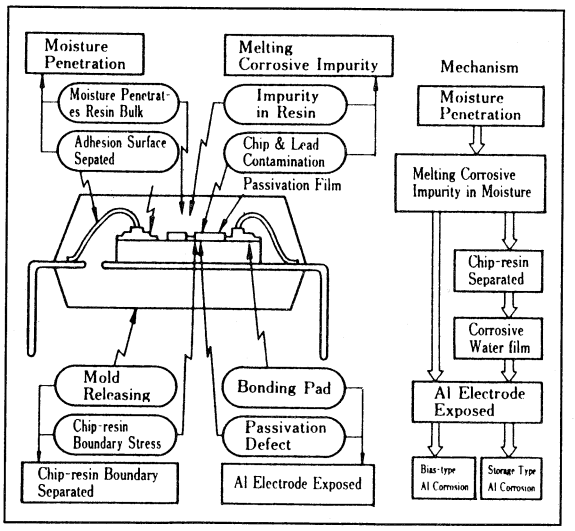


Figure 8 Plastic Package Cross Section and Al Corrosion Mechanism

3. Bonding related failures

   a. Degradation caused by intermetallic formation
   Bonding strength degradation and contact resistance increase are caused by compounds formed in the connections between Au wire and Al film or between Au film and Al wire. These are the most serious problems in terms of reliability. The compounds are formed rapidly during bonding and are increased through thermal treatment. Consequently, Hitachi products are subjected to a lower-temperature, shorter-period bonding whenever possible.

   b. Wire creep
   Wire creep is wire neck destruction in an Au ball along an intergranular system occurring when a plastic sealed device is subjected to a long-term thermal cycling test. This failure results from increased crystal grains due to heat application when forming a ball at the top of an Au wire, or from an impurity introduced to the intergranular system. Bonding under usual conditions with no abnormal loop configuration failures does not cause this failure, unless a severe long-term thermal cycling test is applied. Accordingly, wire creep is not a problem in actual usage.

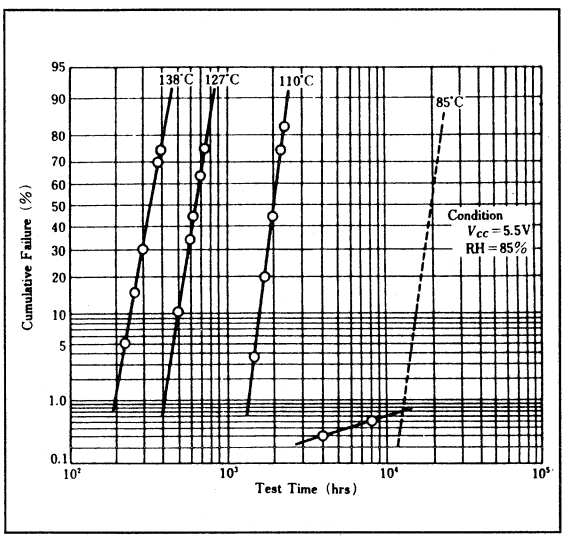


Figure 9 An Example of Moisture Resistance by High Temperature, High Humidity, and High Bias

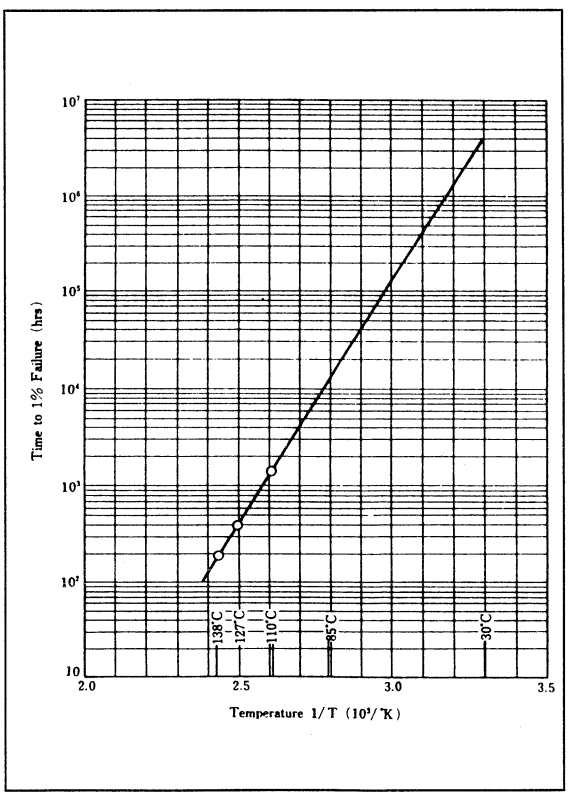


Figure 10 Relationship Between Temperature and Time to 1% Failure (RH = 85%)

c. Chip crack
With the increase in chip size associated with the increased number of incorporated functions, more problems have been occurring during assembly, such as chip cracks during bonding. Bonding methods include Au-silicon eutectic, soldering and Ag-paste. Soldering and Ag-paste exhibit few chip crack problems. For Au-silicon eutectic, in contrast, large stress is applied to a pellet due to its strength and high temperature resistance for attachment, which may result in critical chip defects. Today, the chip destruction limit can be determined by finite-element method and by distortion measurement using a fine accuracy gauge. Ideally, Au-silicon eutectic should be evenly applied over the entire surface. Therefore, specifications for Au-silicon eutectic have been established based on stress analysis and thermal cycling test results.

d. Reduced maximum power dissipation
For power devices, heat fatigue due to thermal expansion coefficient mismatches among different materials deteriorates thermal resistance. This results in decreased maximum power dissipation.

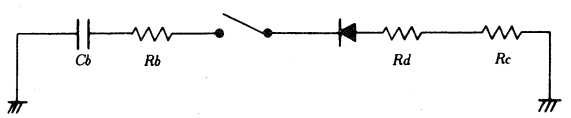
4. Sealing related failures
Hermetic sealing packages, including metal, glass, ceramic, and all other types, have the possibility of the following failures.

— Al line corrosion on the chip surface due to slight moisture and reactions between different ionized materials.
— Intermittent moving foreign metals causing short circuiting.
— Al line corrosion due to extraneous H_2O caused by hermetic failure.

Moving foreign matter, even if it is a non-active solid, can be charged up within a cavity during movement, thereby inducing parasitic effects and metal shorts. The foreign matter detection method is specified by the MIL-STD-883C, PIND (particle impact noise detection) test. The PIND test consists of filtering a particle impact waveform (ultrasonic waveform), detecting it with a microphone, and then amplifying it.

5. Disturbance

a. Electrostatic discharge destruction
Destruction caused by electrostatic discharge is a problem common to semiconductor devices. A recent report introduced three modes of this failure: the human body model, a charged device model, and a field induced model.
The human body is easily charged. A person just walking across a carpet can be charged up to 15,000 V. This voltage is high enough to destroy a device. An equivalent circuit of the human body model is shown in Figure 11. The human body's capacitance C_b and resistance R_b are 100 to



Cb — Human Body Capacity
Rb — Human Body Resistance
Rd — Device Resistance
Rc — Resistance Between Device and Ground

$$E = \frac{1}{2} CbV^2 = 0.2 \times 10^{-3} J$$

Figure 11 Equivalent Circuit of the Human Body Model

200 pF and 1000 to 2000 Ω, respectively. Assuming a body is charged with 2000 V, the dissipated energy is obtained as follows: With a time constant of 10^{-7}s, the dissipated energy is 2 kW, which is enough to destroy a small area of a chip.

In the charged device model, charges are accumulated in a device, not a human body, and discharged through contact resistance during a short time. The equivalent circuit of this model is shown in Figure 12. Device size and device position relative to ground are important parameters in this model since the model depends on device capacity.

In the field induced model a device is left under a strong electric field or is affected by nearby high voltage. Since the capacitors or leads of a device act like antennas, the following cases will possibly cause its destruction.

— A device is incorporated into a high electric field such as a CRT.
— A device is left under a high-frequency electric field.
— A device is moved within a container charged at high voltage, such as a tube.

b. Latch-up

Latch-up is a problem unique to CMOS devices. This problem is a thyristor phenomenon caused by a parasitic PNP or NPN transistor formed in the CMOS configuration. Latch up occurs when an accidental surge voltage exceeding a maximum rating, a power supply ripple, an unregulated power supply, or noise is applied, or when a device is operated from two sources having different setup voltages. These cases can cause input or output current to flow in the opposite direction from the usual flow, which triggers parasitic thyristors. This results in an excessive current flowing between a power supply and ground. This phenomenon continues until the power is removed or the current flow is reduced to a certain level. Once latch-up occurs in an operating device, the device will be destroyed.

Much effort should be made in designing circuits to prevent latch-up. Input or output currents that trigger latch-up start to flow under the following conditions.

$V_{in} > V_{CC}$ or $V_{in} < GND$ for input level
$V_{out} > V_{CC}$ or $V_{out} < GND$ for input level

Circuits should be designed so that no forward current flows through the input protection diodes or output parasitic diodes.

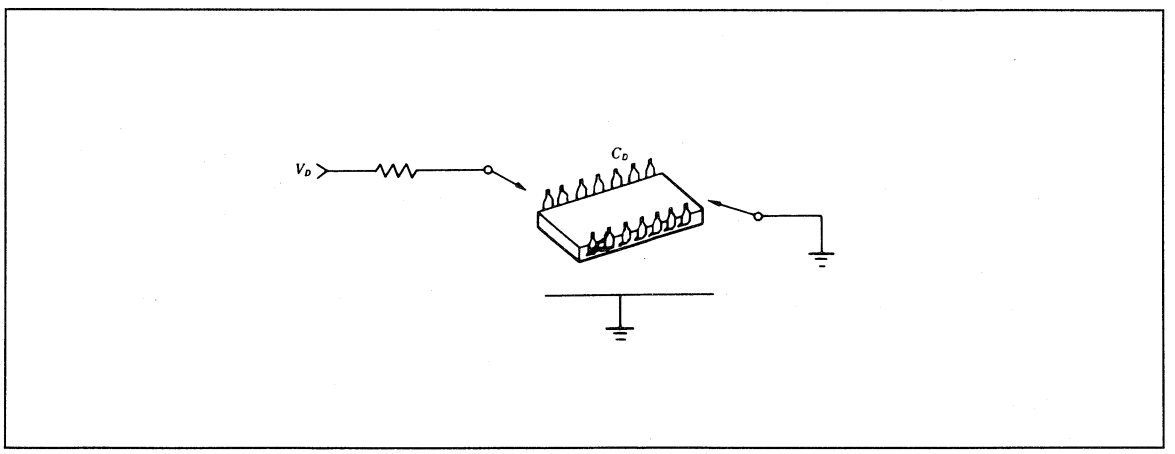


Figure 12 Equivalent Circuit of a Charged Model

c. Soft errors
When α-particles are generated from uranium or thorium on or near the silicon surface of an LSI chip and bombard the Si substrate, electron-hole pairs are formed. They act as noise to memory cell nodes and data lines, which results in data errors. This type of error occurs temporarily and is called a soft error. This phenomenon is shown in Figure 13. Only electrons from among the electron-hole pairs are collected into a memory cell. As a result, the cell changes from a state of 1 to 0, which is a soft error.
Hitachi devices have been subjected to simulation and irradiation tests to prevent soft errors. In some cases, an organic material, PIQ, is applied to the surface of the device.

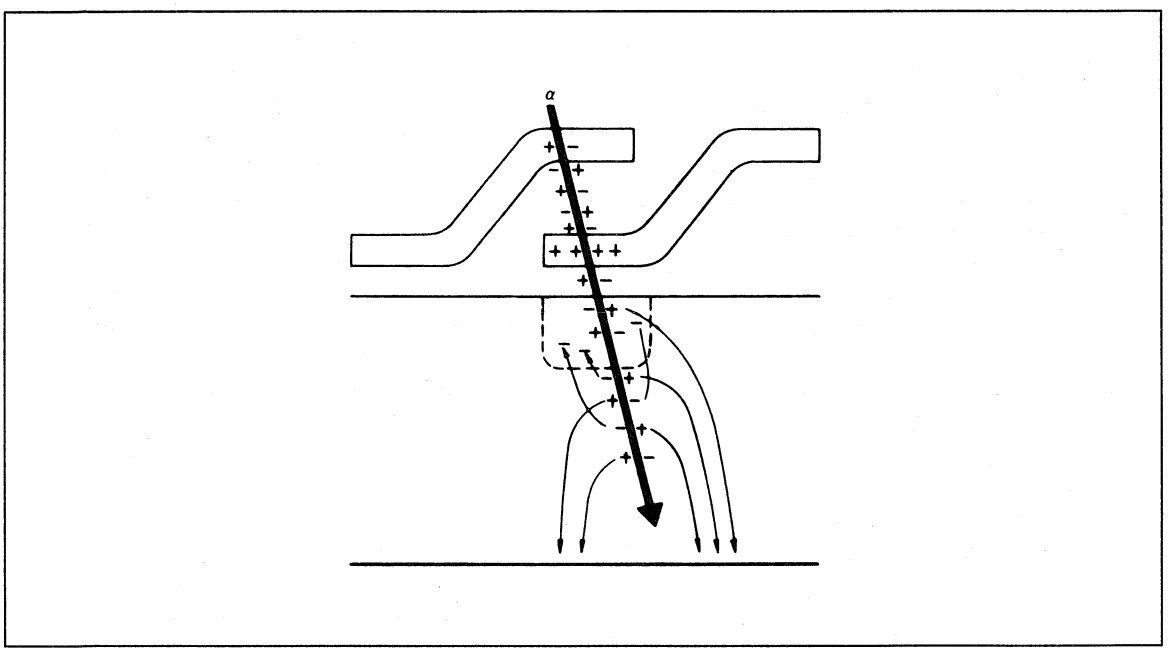


Figure 13 Soft Errors Caused by α-Particles in Dynamic Memory

Table 13 Failure Causes and Mechanisms

Failure Related Causes		Failure Mechanisms	Failure Modes
Passivation	Surface oxide film, insulating film between metallizations	Pin hole, crack, uneven thickness, contamination, surface inversion, hot carrier injected	Degradation of breakdown voltage, short, leak current increased, h_{FE} degraded, threshold voltage variation, noise
Metallization	Interconnection, contact, through hole	Flaw, void, mechanical damage, break due to uneven surface, non-ohmic contact, insufficient adhesion strength, improper thickness, electromigration, corrosion	Open, short, resistance increased
Connection	Wire bonding, ball bonding	Bonding runout, compounds between metals, bonding position mismatch, bonding damaged	Open, short resistance increased
Wire lead	Internal connection	Disconnection, sagging, short	Open, short
Diffusion, junction	Junction diffusion, isolation	Crystal defect, crystallized impurity, photo resist mismatching	Degradation of breakdown voltage, short
Die bonding	Connection between die and package	Peeling chip, crack	Open, short, unstable operation, thermal resistance increased
Package sealing	Package, hermetic seal, lead plating, hermetic package and plastic package, filler gas	Integrity, moisture ingress, impurity gas, high temperature, surface contamination, lead rust, lead bend, break	Short, leakage current increased, open, corrosion soldering failure
Foreign matter	Foreign matter in package	Dirt, conducting foreign matter, organic carbide	Short, leakage current increased
Input/output pin	Electrostatistics, excessive voltage, surge	Human body charged device	Short, open, fusing
Disturbance	α particle	Electron hole generated	Soft error
	High electric field	Surface inversion	Leakage current increased

6. Fine Geometry Related Problems
   LSI circuit geometry has been reduced down to 0.8 μm, and further reductions are expected. However, while transmission line dimensions have undergone this substantial reduction in size, power supplies have not been correspondingly adjusted for 5 V use. Problems associated with finer geometries are shown in Table 14.

Table 14 Finer Geometry Related Problems

Item	Problems	Countermeasure
5 V single supply voltage	• Breakdown voltage of gate oxide films • SiO_2 defects	Oxide film formation process improved • Cleaning • Gettering • Screening
Horizontal dimension reduction	• Soft errors by α particles • Al reliability • CMOS latch up • Mask alignment margin • Hot carriers	Surface passivation film improved • Metallization improved • Design/layout improved • Process improved
Vertical and horizontal dimension reduction	• Higher breakdown voltage not permitted • Electrostatic discharge resistance reduced	Use of low voltage examined • Configuration improved • Protection circuits enhanced

Quality Assurance of IC Memories

1. Views on Quality and Reliability

Hitachi products should always meet individual users' purposes and required quality levels, maintaining satisfactory performance for general applications. Hitachi works continuously to assure high reliability standards for our IC memories in actual usage. To meet user needs and to cover expanding applications, Hitachi has defined these goals:

1. Establish reliability by design during new product development.
2. Establish quality at all steps in the manufacturing process.
3. Strengthen the inspection process at all points.
4. Improve product quality based on user data.

Furthermore, to reach the highest quality and performance levels, development and production teams cooperate very closely with Hitachi research laboratories. All these methods together make it possible for Hitachi to meet and exceed user requirements.

2. Reliability Design of Semiconductor Devices

2.1 Reliability Targets

The establishment of reliability targets is important in manufacturing and marketing, as well as in determining function and price. Practically, the reliability targets cannot be determined from failure rates produced by any single common test condition; they are based on many factors such as equipment characteristics, target system purposes, derating applied during design, operating conditions, and maintenance requirements.

2.2 Reliability Design Factors

Timely analysis and execution are essential to achieve performance based on reliability targets. The primary design items of interest are design standardization, device process and structural design, design review, and reliability testing.

1. Design standardization
   Design standardization requires the establishment of design rules and the specification of parts, materials, and processes. When design rules are being established for the circuit, cell, and layout designs, critical quality and reliability features should also be examined. By doing this effectively, the use of standardized processes or materials, even in newly developed products, should generate much higher reliability (with the possible exception of special requirements or functions).

2. Device process and structural design
   It is important during device design to consider the total balance of process design, structural design, and circuit and layout design. Especially in the case of applying new processes or new materials, at Hitachi we study the technology in depth prior to any detailed device development.

3. Reliability testing by test site
   The test site is also called the test pattern. It is a useful method for evaluating the reliability of complex ICs and complicated functions.

   a. The purposes for the test site are:
   — To make clear definitions about fundamental failure modes
   — To analyze relationships between failure modes and manufacturing processes and/or conditions
   — To analyze failure mechanisms
   — To establish QC points in manufacturing

   b. The effects of the test site are:
   — Evaluation of common fundamental failure modes and failure mechanisms
   — Determination of predominant failure modes, and comparisons with field experiences
   — Analysis of relationships between failure causes and manufacturing factors
   — Simplification of testing

2.3 Design Review

Design review is a method to systematically confirm whether or not a design satisfies the performance required by users, whether it meets all specifications, and whether the technical items accumulated in test data and application data are effectively utilized.

In addition, from the standpoint of comparisons to competitive products, a major focus of the design review is to insure the quality and reliability of the product. At Hitachi, the design review is performed as a part of new product development, and when changing existing products.

The following items are considered in design review.

1. Describing the product based on specified design documents.

2. Planning and executing each product function and program (such as calculations) by considering the product and its documentation from the standpoint of each participant. Experiments and further investigations are indicated if any results are not exactly as expected.

3. Determining the contents and methods of reliability testing based on design documents and drawings.

4. Checking manufacturing process ability to achieve design goals.

5. Arranging preparations for production.

6. Planning and executing each product function and program of all design changes proposed by individual specialists. Generating tests, experiments, and calculations as needed to confirm the results of each design change.

7. Refering to past performance and failure experiences with similar devices. Confirming the prevention of any repetition of such experience, and planning and executing a test program to prove this level of performance.

At Hitachi, design reviews including these steps of analysis and decision are made using individual check lists according to each objective.

3. Quality Assurance System of Semiconductor Devices

3.1 Activity of Quality Assurance

At Hitachi, these are the general purposes of quality assurance:

1. Problems are resolved within each step, so that by the final stage of production even very small potential failure factors will be removed.
2. Information developed at every step is used in other steps, as indicated, to improve quality in the entire production sequence, and therefore achieve satisfactory levels of reliability and performance.

3.2 Qualification

For maximum product quality and reliability, qualification tests are done at each stage of trial production and mass production, based on design reliability as described in Section 2 "Reliability Design of Semiconductor Devices."

These are the purposes of qualification at Hitachi.

1. Qualify the product objectively from a customer standpoint (as by a third party).
2. Consider the failure experiences and data provided by customers.
3. Qualify every change in design and process.
4. Qualify, with special emphasis, all final choices of parts, materials, and processes.
5. Establish control points within the production procedure by considering the process ability and factors of manufacturing variance.

Figure 1 shows the general outline of design qualification at Hitachi.

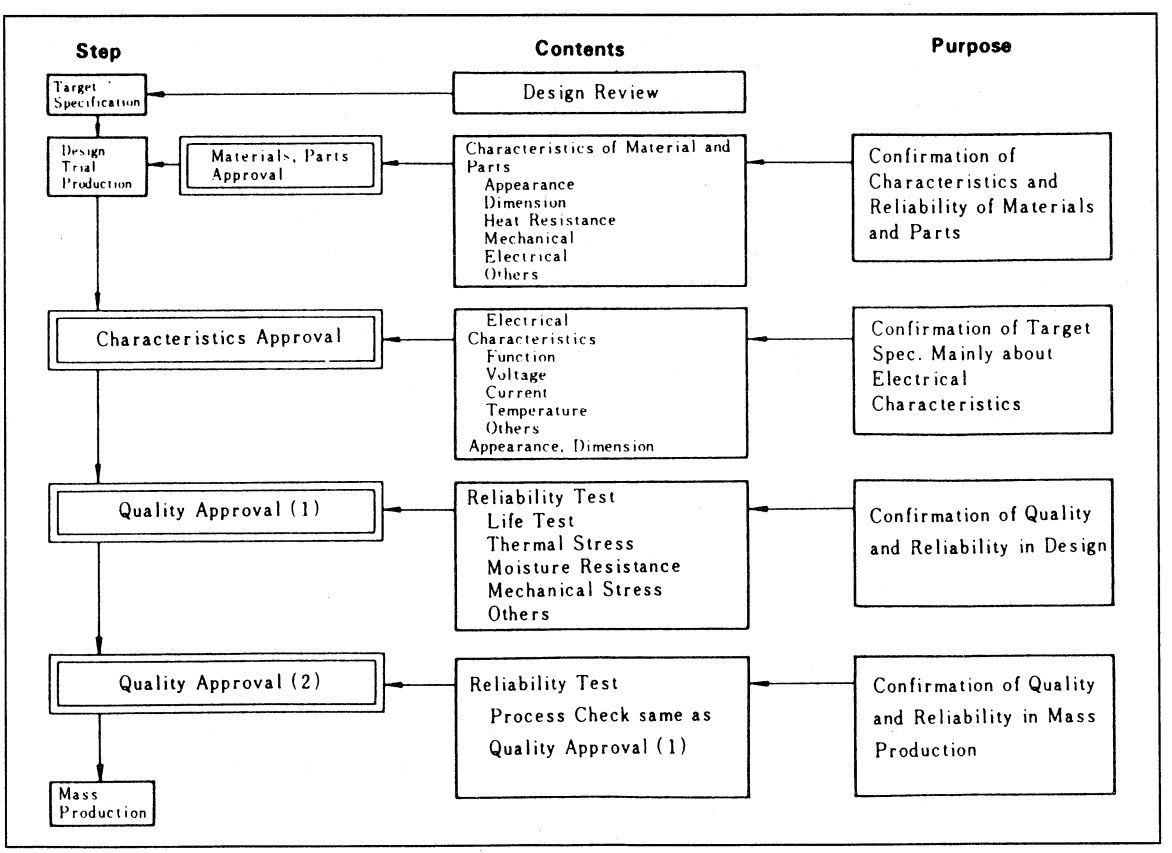


Figure 1 Flowchart of Device Design Qualification

3.3 Quality and Reliability Control in Mass Production

In mass production, quality is the functional responsibility of each department, primarily as defined by the manufacturing department and the quality assurance department. The total function flow is shown in Figure 2.

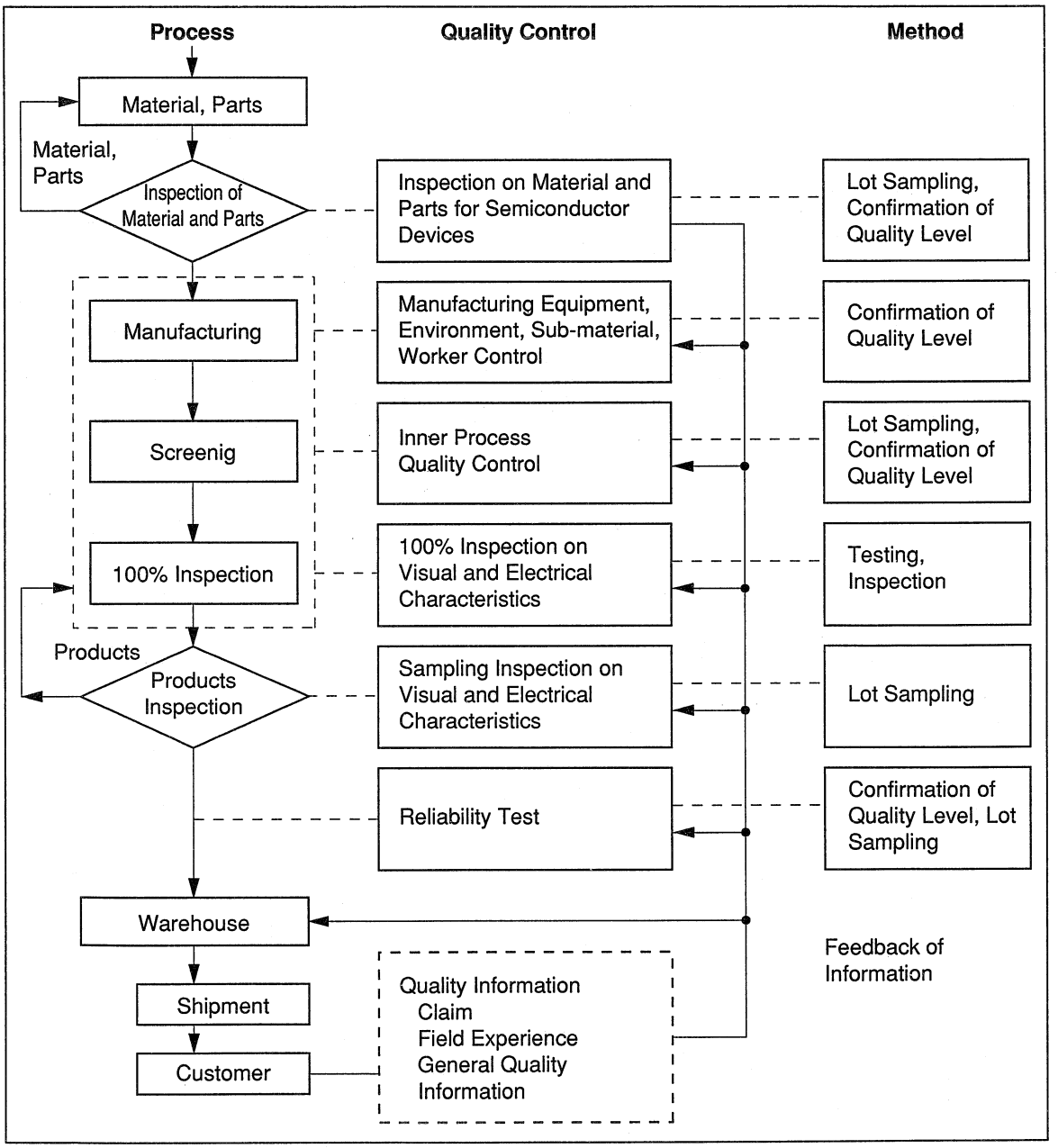


Figure 2 Flowchart of Quality Control in the Manufacturing Process

3.3.1 Quality Control on Parts and Materials

With the tendency toward higher performance and higher reliability of devices, the quality control of parts and materials becomes more important. Items such as crystals, lead frames, fine wire for wire bonding, and packages and materials required in manufacturing processes like mask patterns and chemicals are all subject to inspection and control. Besides the qualification of parts and materials as stated in Section 3.2, the quality control of parts and materials begins at incoming inspection, which is performed based on purchase specifications, drawings and (mainly) sampling tests based on MIL-STD-105D. Other activities related to quality assurance are as follows.

1. Technology meetings with vendors.
2. Approval and guidance of vendors.
3. Analysis and test of physical chemistry.

The typical check points of parts and materials are shown in Table 1.

Table 1 Quality Control Check Points of Parts and Materials (example)

Material parts	Important control items	Check points
Water	Appearance	Damage and contamination on surface
	Dimension	Flatness
	Sheet resistance	Resistance
	Defect density	Defect numbers
	Crystal axis	
Mask	Appearance	Defect numbers, scratches
	Dimension	Dimension level
	Resistoration	
	Gradation	Uniformity of gradation
Fine wire for wire bonding	Appearance	Contamination, scratches, bend, twist
	Dimension	
	Purity	Purity level
	Elongation ratio	Mechanical strength
Frame	Appearance	Contamination, scratches
	Dimension	Dimension level
	Processing accuracy	
	Plating	Bondability, solderability
	Mounting characteristics	Heat resistance
Ceramic package	Appearance	Contamination, scratches
	Dimension	Dimension level
	Leakage resistance	Airtightness
	Plating	Bondability, solderability
	Mounting characteristics	Heat resistance
	Electrical characteristics	
	Mechanical strength	Mechnical strength
Plastic	Composition	Characteristics of plastic material
	Electrical charactristics	
	Thermal characteristics	
	Molding performance	Molding performance
	Mounting characteristics	Mounting characteristics

3.3.2 Process Quality Control

Control of process quality is extremely significant in the overall process of device quality assurance. Quality control functions at every stage of production are described below. Figure 3 lists specific process quality control factors.

1. Quality control of products in every stage of production
   Potential device failure factors should be removed as soon as possible in the manufacturing process. To do this, check points are set up within each process to prevent products exhibiting failure factors to move onto any following process. Especially for devices designed for high reliability, manufacturing lines are rigidly monitored to control process quality. Additionally, we perform very stringent checks on some processes and/or lots, and even 100% inspections in certain critical processes to remove potentially failing items related to unavoidable manufacturing variances. Screening based on high temperature aging or temperature cycling are also part of quality assurance procedures. Controlling quality during processing includes these items:

   a. Control of conditions of equipment and workers
   b. Sampling test of uncompleted products
   c. Proposal and implementation of improvements in working conditions
   d. Continuous worker education
   e. Maintenance and improvement of yields
   f. Identification of quality problems, and implementation of countermeasures to eliminate them
   g. Communication of quality-related information

2. Quality control of manufacturing facilities and measuring equipment
   Manufacturing facilities have been developed to answer the need for higher device performance and automated production. It is also important to define and accurately measure quality and reliability.

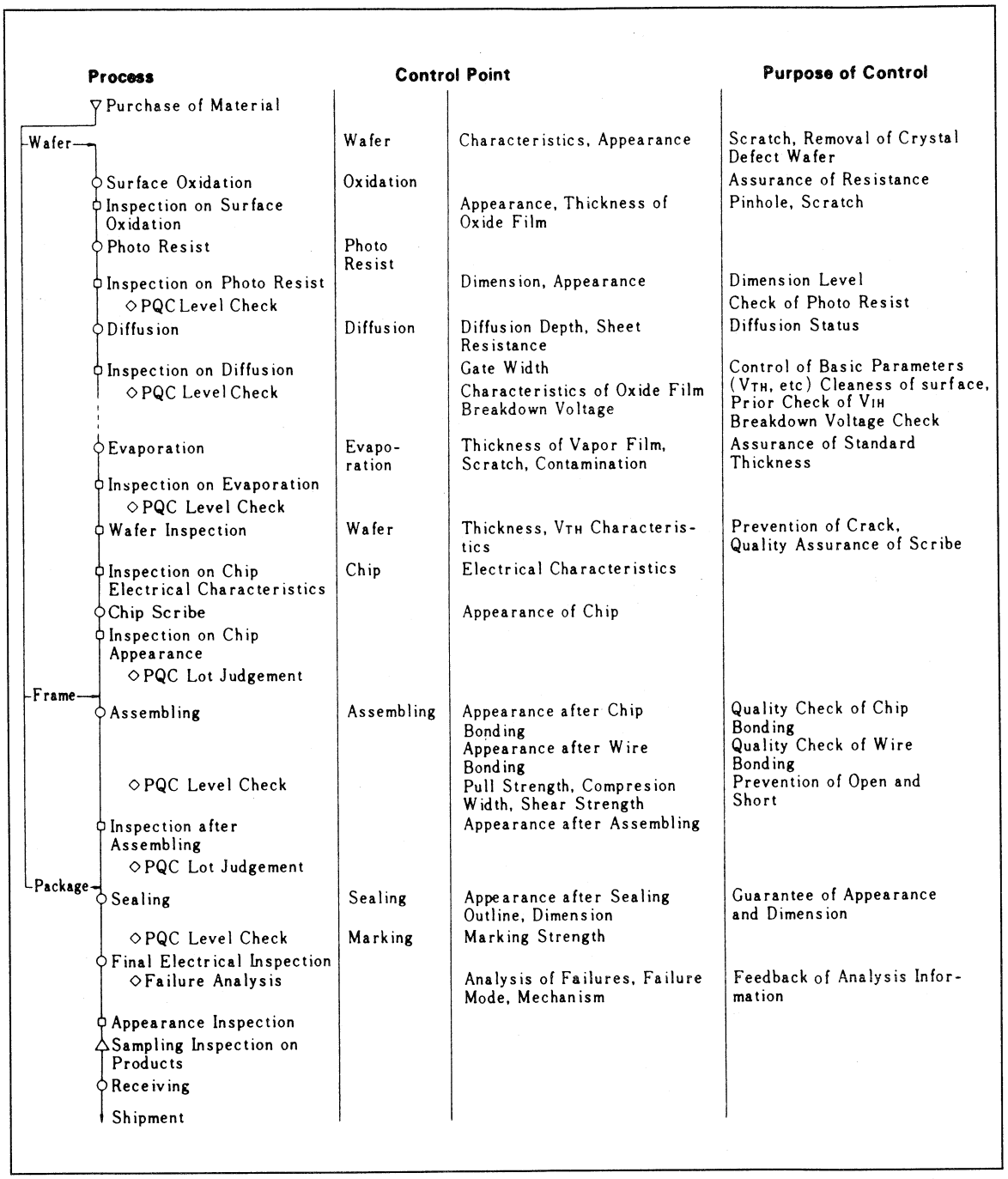
   At Hitachi, automated manufacturing is used to reduce manufacturing variances. The operation of high performance equipment requires automated control to function properly.

   Maintenance inspections are carried out daily to ensure proper quality control, and in some instances at other more frequent intervals according to specifications, at every check point.

   The adjustment and maintenance of measuring equipment is done according to specifications and past experience, and is vigorously monitored to maintain and improve the quality of our products.

3. Quality control of the manufacturing environment and submaterial
   Final quality and reliability of devices are especially affected by manufacturing processes. We therefore thoroughly control factors of the manufacturing environment, such as gases or pure water.

   Dust control is critical to achieve higher integration and higher device reliability. To maintain and improve the cleanliness of the manufacturing site, we take great care to keep buildings, facilities, air-conditioning systems, materials, clothes, and all possible elements associated with production as clean and dust-free as we can. We extend this effort to periodically check the ambient air in the manufacturing facility for floating dust, and we check for any minute amounts which might have accumulated on the floor, other surfaces, or on any equipment.



Process	Control Point		Purpose of Control
▽ Purchase of Material			
Wafer —			
	Wafer	Characteristics, Appearance	Scratch, Removal of Crystal Defect Wafer
○ Surface Oxidation	Oxidation		Assurance of Resistance
○ Inspection on Surface Oxidation		Appearance, Thickness of Oxide Film	Pinhole, Scratch
○ Photo Resist	Photo Resist		
○ Inspection on Photo Resist		Dimension, Appearance	Dimension Level
◇ PQC Level Check			Check of Photo Resist
○ Diffusion	Diffusion	Diffusion Depth, Sheet Resistance	Diffusion Status
○ Inspection on Diffusion		Gate Width	Control of Basic Parameters (V_{TH}, etc) Cleaness of surface, Prior Check of V_{IH} Breakdown Voltage Check
◇ PQC Level Check		Characteristics of Oxide Film Breakdown Voltage	
○ Evaporation	Evaporation	Thickness of Vapor Film, Scratch, Contamination	Assurance of Standard Thickness
○ Inspection on Evaporation			
◇ PQC Level Check			
○ Wafer Inspection	Wafer	Thickness, V_{TH} Characteristics	Prevention of Crack, Quality Assurance of Scribe
○ Inspection on Chip Electrical Characteristics	Chip	Electrical Characteristics	
○ Chip Scribe		Appearance of Chip	
○ Inspection on Chip Appearance			
◇ PQC Lot Judgement			
Frame —			
○ Assembling	Assembling	Appearance after Chip Bonding	Quality Check of Chip Bonding
		Appearance after Wire Bonding	Quality Check of Wire Bonding
◇ PQC Level Check		Pull Strength, Compresion Width, Shear Strength	Prevention of Open and Short
○ Inspection after Assembling		Appearance after Assembling	
◇ PQC Lot Judgement			
Package —			
○ Sealing	Sealing	Appearance after Sealing Outline, Dimension	Guarantee of Appearance and Dimension
◇ PQC Level Check	Marking	Marking Strength	
○ Final Electrical Inspection			
◇ Failure Analysis		Analysis of Failures, Failure Mode, Mechanism	Feedback of Analysis Information
○ Appearance Inspection			
△ Sampling Inspection on Products			
○ Receiving			
Shipment			

Figure 3 Example of Process Quality Control Factors

3.3.3 Final Tests and Reliability Assurance Tests

1. Final tests
   Lot inspection is done by the quality assurance department for products already passed in 100% testing during the manufacturing process. Although 100% performance is expected, sample lot inspection is also carried out to prevent any possible accidental mixture of failed products with regular, satisfactory devices.
   The extra lot inspection not only confirms that all products meet all user requirements, but considers any other potential factors. Our lot inspection is based on MIL-STD-105D.

2. Reliability assurance tests
   To assure reliability, appropriate tests are performed periodically on each manufacturing lot if the user requires such a high level of examination.

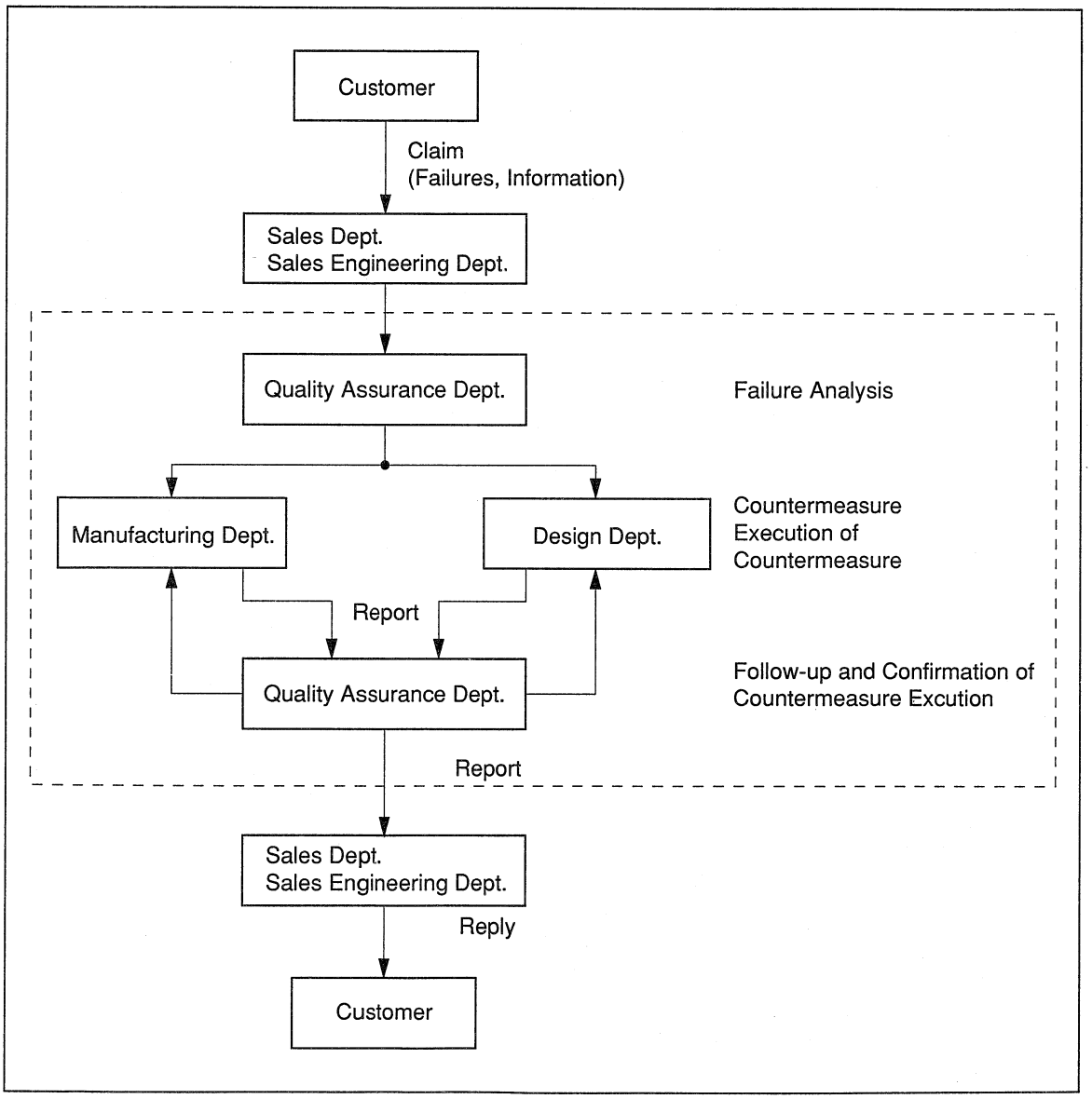


Figure 4 Process Flowchart for Customer-Reported Failure

Outline of Testing Method

1. Inspection Method

In memory IC inspection, the quality cannot be judged solely by a DC test on the external pins. The number of elements such as transistors which can be judged in a DC test is a very small part of all elements. The proposed address patterns listed below inspect whether internal circuits are functioning correctly.

1. All low, all high
2. Checker flag
3. Stripe pattern
4. Marching pattern
5. Galloping
6. Walking
7. Ping-pong

These are only a few representative samples of the testing options. There are also patterns to check the mutual interference of bits and the maximum power dissipation. Among the listing, 1 through 4 are called N patterns, which can check one sequence of N-bit IC memory with several consecutive cycles of N patterns. 5 through 7 are called N^2 patterns, which need several cycles of N^2 patterns to check one sequence of N-bit IC memory. Serious problems arise using N^2 patterns in large-capacity memory. For example, the inspection of 1-Mbit memory with the galloping pattern takes considerable time—about 120 hours. 1, 2, and 3 are rather simple and effective methods, but these patterns will not find all the failures in decoder circuits. Marching is the most simple and powerful pattern to check the functions of IC memories.

2. Marching Pattern

The marching pattern, as its name indicates, is a pattern in which 1s sequentially replace 0s throughout the device. The 1s "march" into all bits of 0. For example, a simple addressing of 16-bit memory is described below.

1. Clear all bits (see Figure 1 a).
2. Read 0 from the 0th address and check that read data is 0. Hereafter, to read means "checking and judging data."
3. Write 1 on the 0th address (see Figure 1 b).
4. Read 0 from the 1st address.
5. Write 1 on the 1st address.

   .
   .
   .
6. Read 0 from the nth address.
7. Write 1 on the nth address (see Figure 1 c).
8. Repeat 6 and 7 to the last address. Finally all data will be 1.
9. After all data has become 1, repeat from 2 through 8 replacing 0 with 1.

In this method, 5N address patterns are necessary for the N-bit memory.

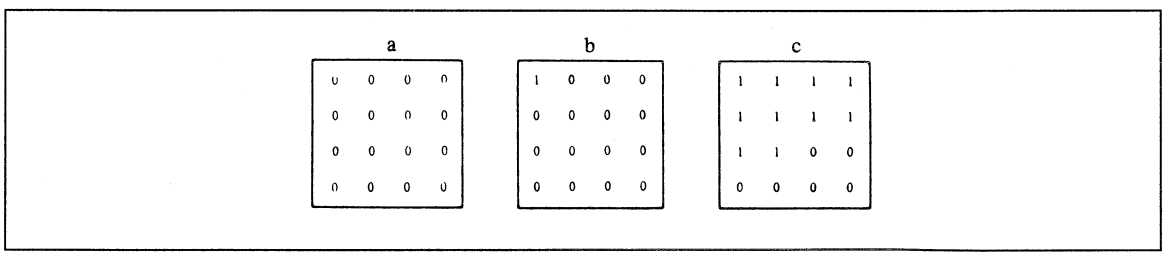


Figure 1 Addressing Method of 16-Bit Memory in the Marching Pattern

1. Static RAM

1.1 Static RAM Memory Cell

A memory cell used in Hitachi static RAM consists of 4 NMOS transistors and 2 load resistors as shown in Figure 1-1. The data in the cell can be retained as long as power is supplied, and read out without being destroyed.

1.2 Data Retention Mode and Battery Backup System

The data in RAM is destroyed at power off. However, CMOS static RAM has a data retention mode. In this mode, power consumption at standby is extremely low and supply voltage can be reduced to 2 V. This enables a battery backup system to retain the data during power failure.

Data Retention Mode: The important point in designing a battery backup system is the timing relationship between the memory power supply and the chip select signal during a change from the ordinal power source and battery power. If proper timing for the change is missed, memory data might be destroyed.

Figure 1-2 shows the timing for switching the power supply. The definitions for the technical terms related to the data retention mode are as follows.

Data retention mode: The period during which the supply voltage is lower than the specified operation voltage. During this period, memory must be kept in non-select condition (e.g. $\overline{CS}$ = V_{DR} – 0.2 V).

t_{CDR} (time from chip select to data retention): The minimum time needed to change from operating mode to data retention mode. Normally 0 ns.

t_R (operation recovery time): The minimum time needed to change from data retention mode to operating mode.

V_{DR} (data retention voltage): The voltage applied in data retention mode. Normally the minimum supply voltage needed to retain memory data is 2 V.

I_{CCDR} (data retention current): The current consumption in the data retention mode depends on the memory power supply voltage and ambient temperature. It is specified as supply voltage, V_{DR} = 3.0 V.

Battery Backup System: The sequence of activities required to switch to battery backup is as follows.

1. External circuit detects a failure in the system power supply.

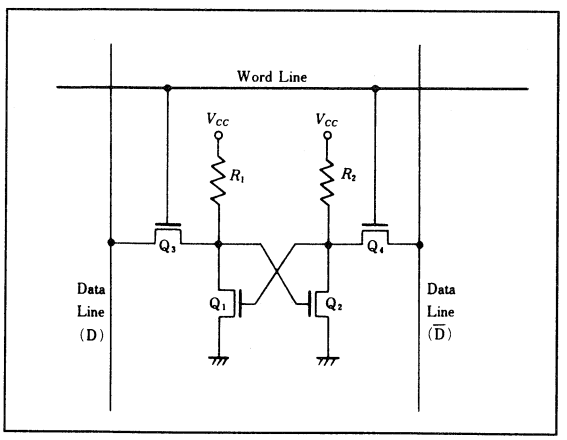


Figure 1-1 Static RAM Memory Cell

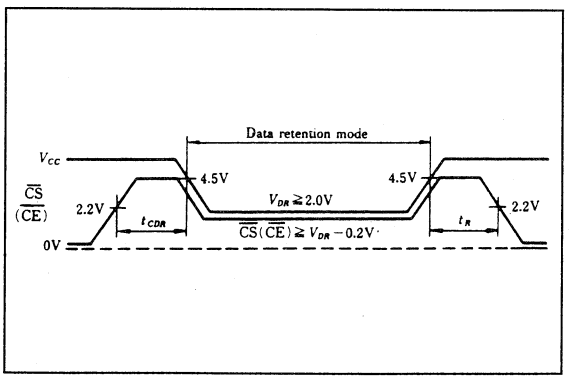


Figure 1-2 Timing for Battery Backup Application

2. External circuit switches the RAM to standby mode.
3. External circuit separates the RAM from the system power supply.
4. External circuit switches to the backup power supply.

The control circuit detects the power failure and disconnects the power source after switching memory to the standby mode. On recovery, it confirms the power supply availability and, after some delay, returns memory to the operating mode. Memory control signals depend on the types of memory used in the system.

1. Using memory with only one $\overline{CS}$:
   The NAND signal between the control signal and chip select signal should be connected to $\overline{CS}$. Since the level of $\overline{CS}$ in the data retention mode must be higher than V_{DR} – 0.2 V, the power supply for this NAND gate must either be shared with the memory power supply or be pulled up to the memory power supply.
2. Using memory with two $\overline{CS}$:
   Basically, the signals are the same as above. In general use, two pins should be used for the control signal and the chip select signal, respectively. When the $\overline{CS}$ intercepts the current path of other pins in the input buffers, it is used as control signal input for the data retention mode.
3. Using memory with $\overline{CS}$ and CS:
   Since CS selects the chips at high level, it is preferable to use CS rather than $\overline{CS}$ as a control signal input for the data retention mode. As soon as power down is detected, the signals should be brought low. Therefore, a pull-up to the memory power supply level is not needed, thus simplifying the circuit organization.

Figure 1-4 shows an example of a battery backup system circuit. Hitachi recommends using CMOS logic for gate G1 in a control circuit and memory V_{CC}. The low V_{CE} transistor Q_1 is required to switch the regulating circuit from system power supply to backup power supply.

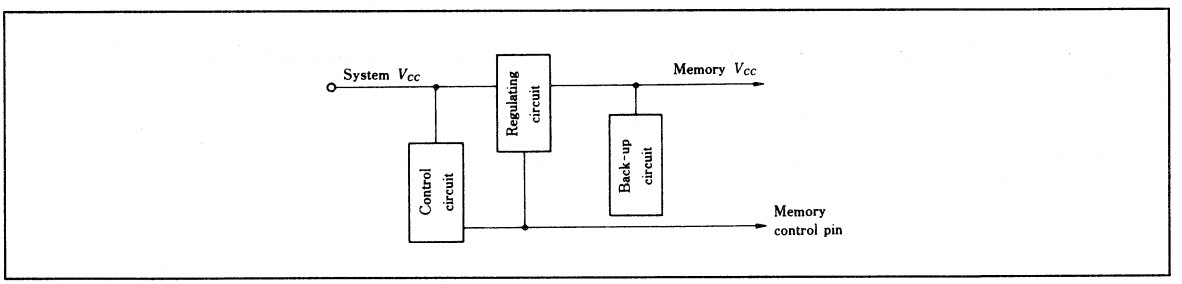


Figure 1-3 Example of Battery Backup System

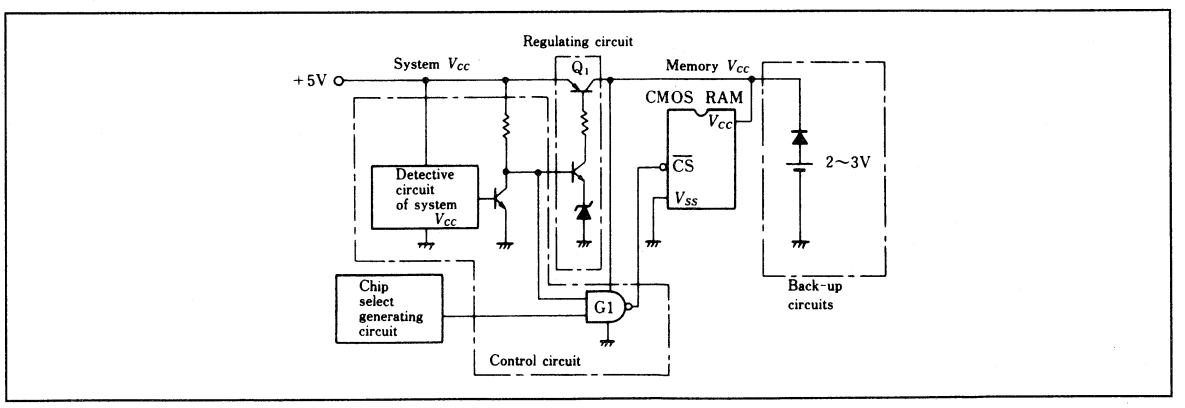


Figure 1-4 Example of a Battery Backup System Circuit

2. Pseudo-Static RAM

2.1 Pseudo-Static RAM Features

A new type of memory, pseudo-static RAM (PSRAM), provides the advantages of dynamic RAM (low cost, high density), and static RAM (easy usage). An IC memory consists of memory cells for data storage, and input/output circuits for interfacing to the external circuits. PSRAM provides memory cells and peripheral circuits of DRAM, external control circuits (including a part of refresh control circuits not provided by dynamic RAM) and interface circuits similar to those of static RAM on a single chip as shown in Table 2-1. The address input is not multiplexed, and the data input/output is byte-wide like the standard static RAM. With PSRAM, a medium density memory system can be easily designed. PSRAM provides address refresh, automatic refresh, and self-refresh.

Using PSRAM, the circuits interfacing to the CPU can be drastically reduced, compared with DRAM. Figure 2-1 shows examples of system design using PSRAM and DRAM. Figure 2-2 shows a block diagram of the PSRAM.

2.2 1-Mbit Pseudo-Static RAM Function

Read/Write Cycle: Figures 2-3 and 2-4 show the timing chart for the read/write cycle of the 1-Mbit pseudo-static RAM HM658128A. The HM658128A can perform two types of access in a read cycle, $\overline{CE}$ access (Figure 2-3 a) and $\overline{OE}$ access (Figure 2-3 b). It writes the data at the rising edge of $\overline{WE}$ (Figure 2-4 a) or at the rising edge of $\overline{CE}$ (Figure 2-4 b). The $\overline{CS}$ pin should be brought high when the address is latched at the falling edge of $\overline{CE}$ in the read/write cycle. The HM658128A has no $\overline{OE}$ specification at the falling edge of $\overline{CE}$ as it provides both the $\overline{OE}$ pin and the $\overline{RFSH}$ pin.

Table 2-1 PSRAM Features

	SRAM	PSRAM	DRAM
Memory cell	4 Tr + 2 R	1 Tr + 1 C	1 Tr + 1 C
Address	Single address	Single address	Multiplexed address
Refresh	Not necessary	Necessary	Necessary
External circuits	Simple ◄——————►		Complex

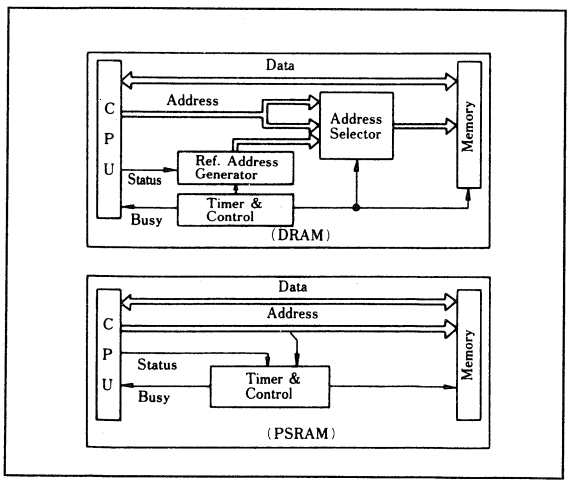


Figure 2-1 System Organization

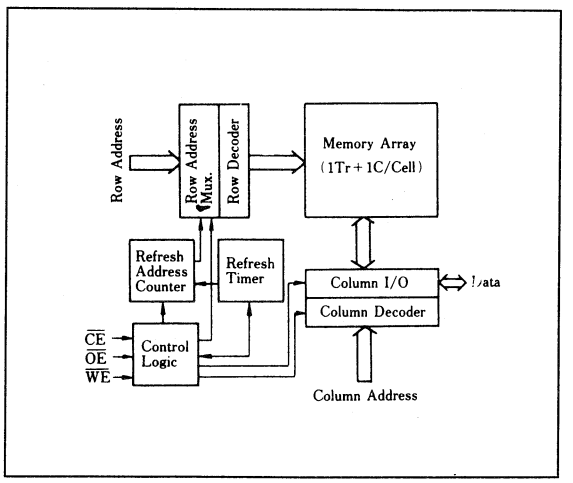


Figure 2-2 Block Diagram (PSRAM)

CS Standby Mode: The HM658128A enters the CS standby mode for one cycle if CS goes low at the falling edge of $\overline{CE}$ (Figure 2-5).

Address Refresh: Address refresh mode performs refresh by accessing to row addresses (A0–A8) 0–511 sequentially within 8 ms as shown in Figure 2-6 (in the distributed mode). In this mode, CS should be high at the falling edge of $\overline{CE}$.

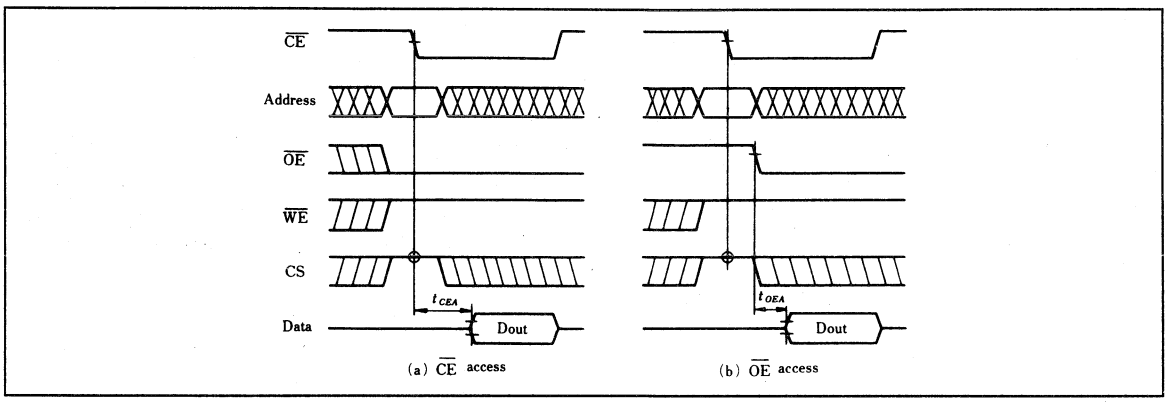


Figure 2-3 Read Cycle

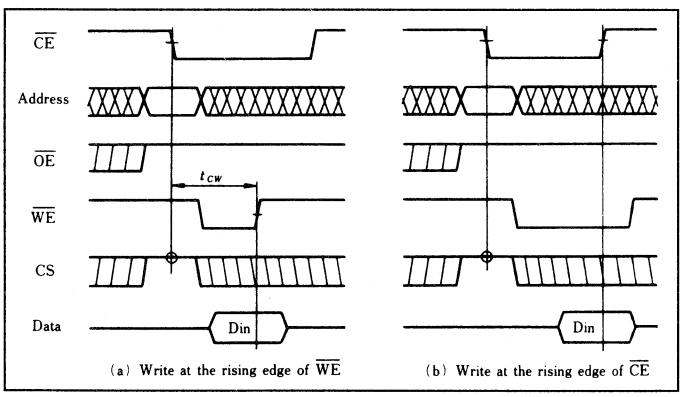


Figure 2-4 Write Cycle

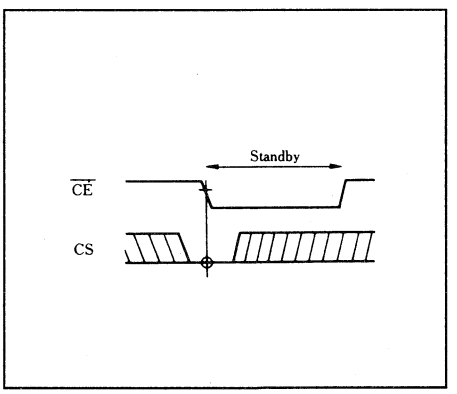


Figure 2-5 CS Standby Mode

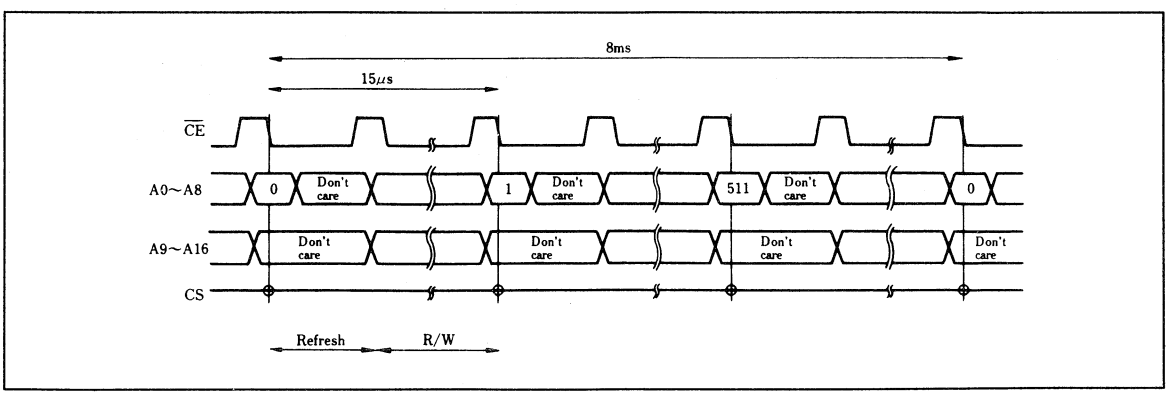


Figure 2-6 Address Refresh

Automatic Refresh: The HM658128A goes to automatic refresh mode, while $\overline{CE}$ is high, if $\overline{RFSH}$ falls and is kept low for more than t_{FAP}.

It is not required to input the refresh address from address pins A0–A8, as it is generated internally. Figure 2-7 shows the timing chart for distributed refresh. In the automatic refresh mode, the timing for only $\overline{CE}$ and $\overline{RFSH}$ are specified.

Self-Refresh: Self-refresh mode performs refresh at an internally determined interval. The HM658128A enters this mode when the internal refresh timer is enabled by keeping $\overline{CE}$ high and $\overline{RFSH}$ low for more than 8 µs (Figure 2-8).

Considerations for Using the HM658128A: The following should be considered when using the HM658128A.

- Data retention:
  The HM658128A can retain data on battery power. The HM658128AL, a low power version, offers a typical self-refresh or standby current of 100 µA.
  A 1-Mbyte system (using eight HM658128Ls) can retain the data for about 1.5 months with a battery supplying 1000 mAh current. V_{CC} = 5 V ±10% must be maintained for data retention.
- Power on:
  Start HM658128A operation by executing more than eight initial cycles (dummy cycles) for more than 100 µs after the power voltage reaches 4.5 to 5.5 V following power on.
- Bypass capacitor:
  Hitachi recommends inserting one bypass capacitor per RAM device.

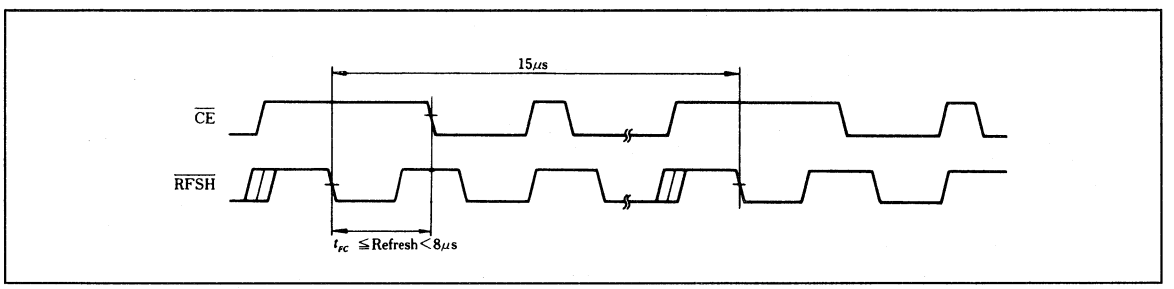


Figure 2-7 Automatic Refresh

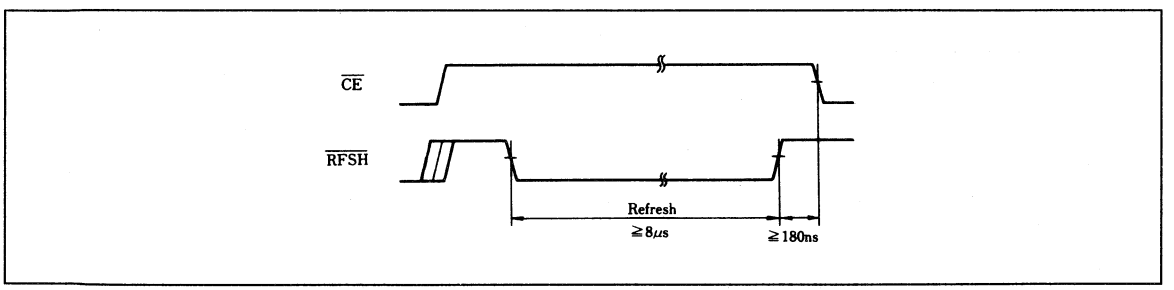


Figure 2-8 Self-Refresh

2.3 Pseudo-Static RAM Data Retention

PSRAM with self-refresh retains data when $\overline{CE}$ and $\overline{OE}$ are fixed to the specific level for more than a defined period.

Low voltage data retention of PSRAM is not same as that of full SRAM.

PSRAM uses one MOS-type memory cell as shown in Figure 2-9. The charge is stored on the capacitor C.
In self refresh mode the charge is periodically refreshed by internal clocks and the data is retained. There are special characteristics of PSRAM self refresh.

Power supply voltage in self refresh mode: Power supply voltage in self refresh mode is 4.5 V to 5.5 V for standard parts. Although, Hitachi provide 3.0 V or 4.0 V V_{CC} min for special parts.

Since the internal refresh circuits operate in self refresh mode, low V_{CC} limit is higher than full SRAM. Figure 2-10 indicates the image of the operation voltage for self refresh and subsequent read. If there is big voltage difference between these two modes, PSRAM does not work.

Slope of power supply rising or falling: The rising slope or the falling slope of supply voltage below 4.5 V, must be smaller than 0.05 V/ms.

V_{CC} dependency or temperature dependancy of self refresh current: V_{CC} dependency is shown in Figure 2-11 and temperature dependency in Figure 2-12.

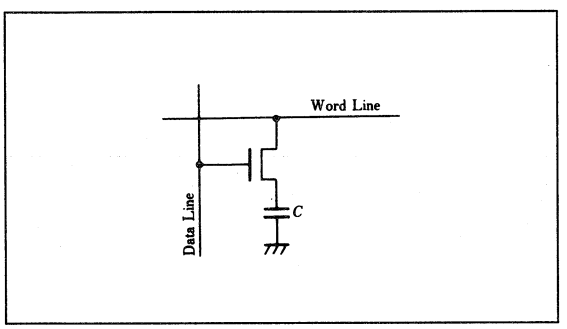


Figure 2-9 A Memory Cell of PSRAM

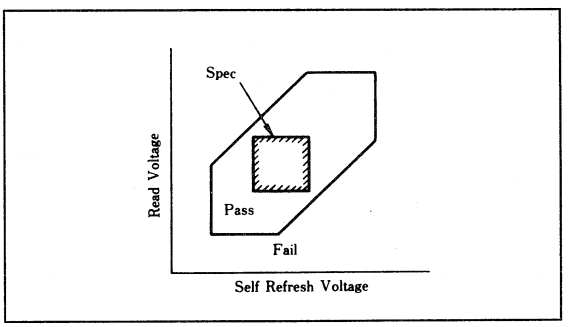


Figure 2-10 PSRAM Operating Voltage

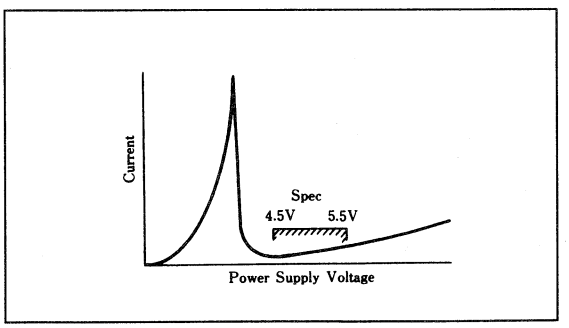


Figure 2-11 Self-Refresh Current vs. Voltage

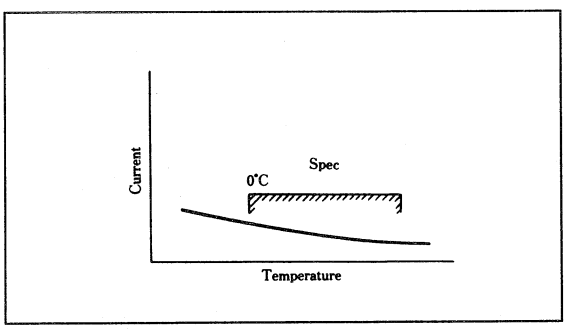


Figure 2-12 Self-Refresh Current vs. Temperature

3. Specific Memories for Graphic/ Video Applications

3.1 Multiport Video RAM

Figure 3-1 shows the general concept of video RAM. A multiport video RAM provides an internal data register (SAM) with memory (RAM). Both can be accessed asynchronously. Effective graphic display memory can be developed by using the random port of the RAM component for graphic processor drawing, and the serial port of the SAM component for CRT display.

Figure 3-2 shows the block diagram of the 256-k/1-Mbit multiport video RAM HM53461/HM534251, and Table 3-1 shows the operation modes of the HM53461/HM534251.

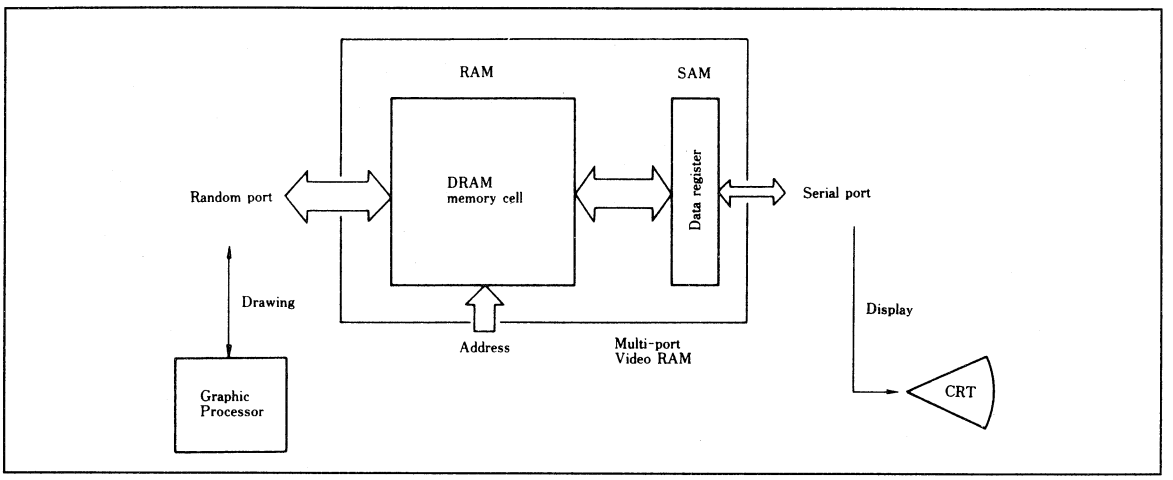


Figure 3-1 A General Concept of Multiport Video RAM

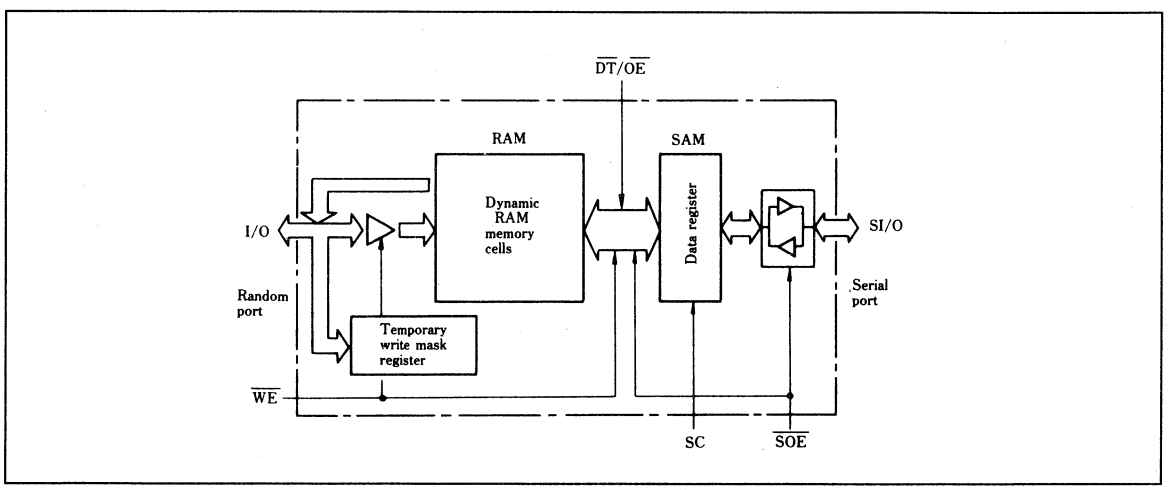


Figure 3-2 Block Diagram of HM53461/HM534251

The operation modes shown in Table 3-1 are described as follows.

Read/Write Operation: Read/write is performed on the random port in the same sequence as a dynamic RAM (Figure 3-3). The HM53461/HM534251 starts the read operation with $\overline{WE}$ high and the write operation at the falling edge of $\overline{WE}$.

Temporary Write Mask Set and Temporary Masked Write Operation: The HM53461/HM534251provides a temporary masked write operation which inhibits writing data bit-by-bit (write mask) during one $\overline{RAS}$ cycle. The temporary write mask set function defines the bits to be inhibited (Figure 3-4). This operation puts the data on I/O1–I/O4 into the internal temporary write mask register. When 0 is programmed to the register, writing to the corresponding bit is inhibited.

The temporary write mask register is reset at the rising edge of $\overline{RAS}$.

Table 3-1 Operation Modes of HM53461/HM534251

At the Falling Edge of $\overline{RAS}$					SAM Modes	
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WE}$	$\overline{SOE/SE}$	RAM Modes	SI/O direction	Notes
H	H	H	X	Read/write	S_{in}/S_{out}	1, 2, 3
H	H	L	X	Temporary write mask data program	S_{in}/S_{out}	1, 2, 3
H	L	H	X	Read transfer	S_{out}	2
H	L	L	L	Write transfer	S_{in}	
H	L	L	H	Pseudo transfer	S_{in}	
L	X	X	X	CBR refresh	S_{in}/S_{out}	1, 2

H: High, L: Low, X: Don't care

Notes:-

1. The transfer cycle executed previously defines SI/O direction.
2. SI/O is in a high impedance state with $\overline{SOE}$ high, even if the direction is S_{out}.
3. The HM53461/HM534251 starts write operation if $\overline{WE}$ is low at the falling edge of $\overline{CAS}$ or becomes low between the falling edge of $\overline{CAS}$ and the rising edge of $\overline{RAS}$.

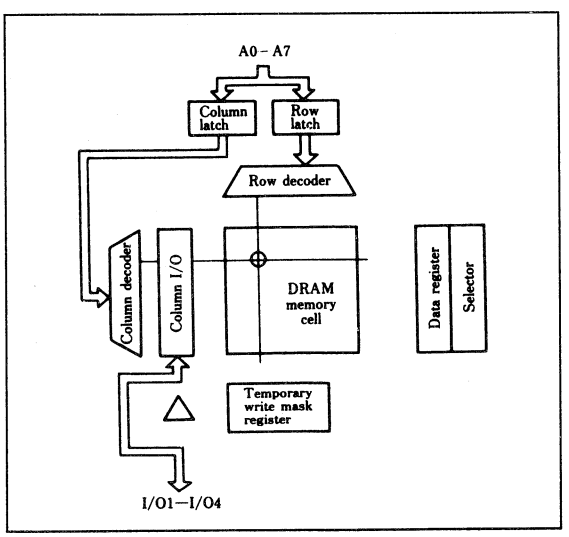


Figure 3-3 Read/Write Operation

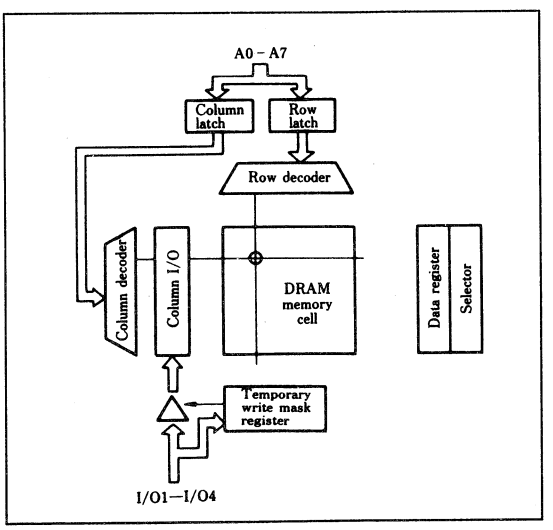


Figure 3-4 Temporary Masked Write Operation

Read Transfer Operation: In this cycle, the HM53461/HM534251 transfers the data of one row in RAM (1024 bits), at the address specified by the falling edge of $\overline{RAS}$, to SAM (Figure 3-5). The start address in SAM can be programmed at the falling edge of $\overline{CAS}$ in this cycle. After data transfer, the serial port is set to the serial read mode at the rising edge of $\overline{DT/OE}$.

Write Transfer Operation: In this cycle, the HM53461/HM534251 transfers the data in the SAM data register (1024 bits) to one row in RAM, at the address specified by the falling edge of $\overline{RAS}$ (Figure 3-6). The start address in SAM can be programmed in this cycle. After data transfer, the serial port is set to serial write mode.

Pseudo Transfer Operation: This operation switches the serial port to serial write mode (Figure 3-7). It does not perform data transfer between RAM and SAM. The SAM start address can be programmed in this cycle.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Operation: The HM53461/HM534251 performs refresh by using the internal address counter in this operation (Figure 3-8).

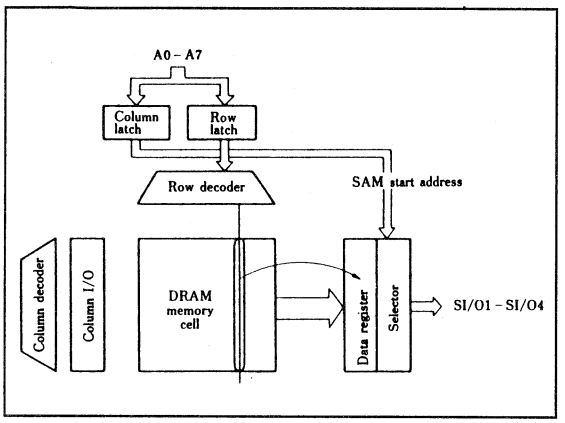


Figure 3-5 Read Transfer Operation

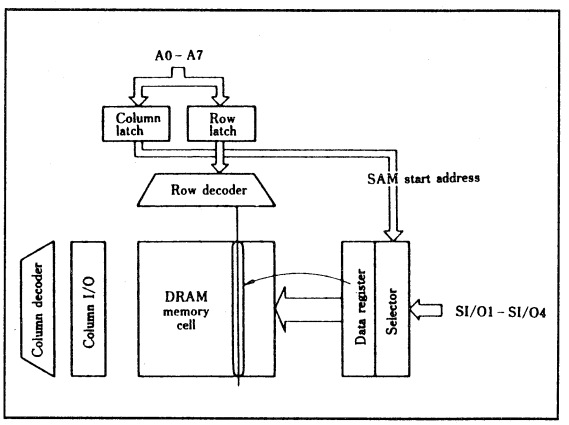


Figure 3-6 Write Transfer Operation

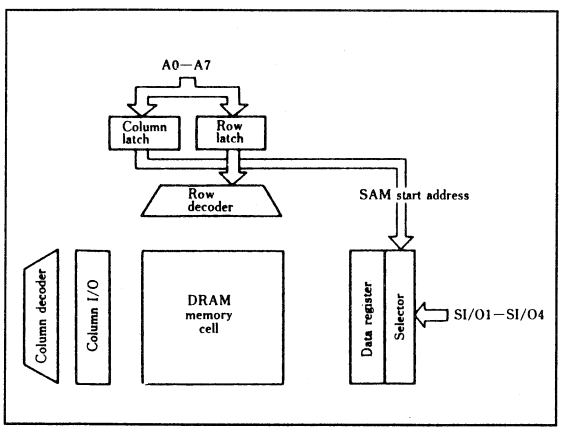


Figure 3-7 Pseudo Transfer Operation

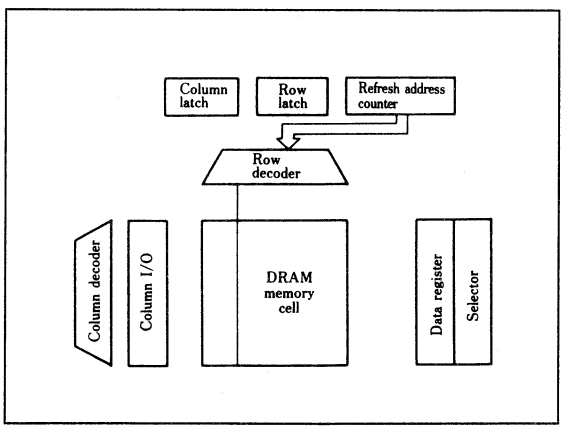


Figure 3-8 $\overline{CAS}$-Before-$\overline{RAS}$ Refresh

Serial Read/Write Operation: The HM53461/HM534251 reads/writes the contents of the SAM data register in serial mode at the rising edge of SC (serial clock input) (Figure 3-9). The address for serial access is generated by the internal address pointer, independent of the random port operation. It should be considered that serial access is restricted in transfer cycles. The SAM, employing static-type data registers, requires no refresh.

The HM53462/HM534252 is a multiport video RAM with logic operation capabilities advantageous in the HM53461/HM534251.

Figure 3-10 shows the block diagram of the HM53462/HM534252. Table 3-2 describes the operation modes.

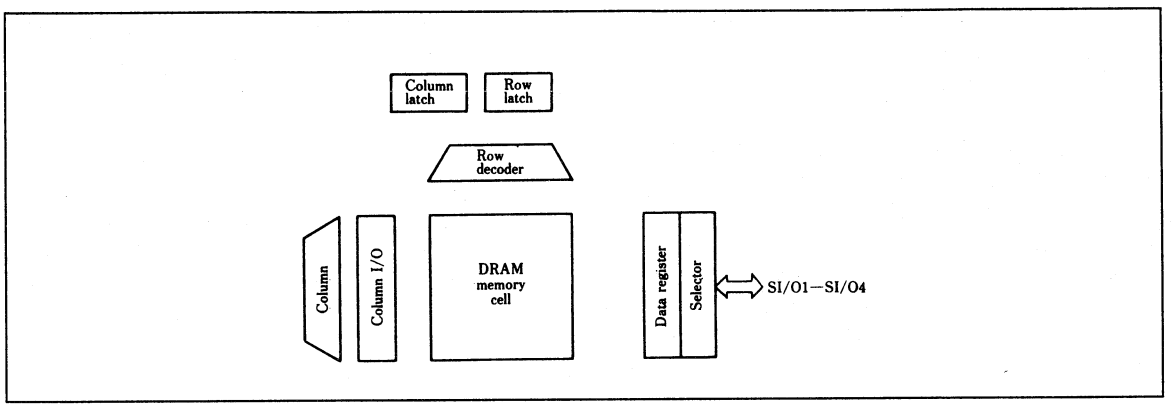


Figure 3-9 Serial Read/Write Operation

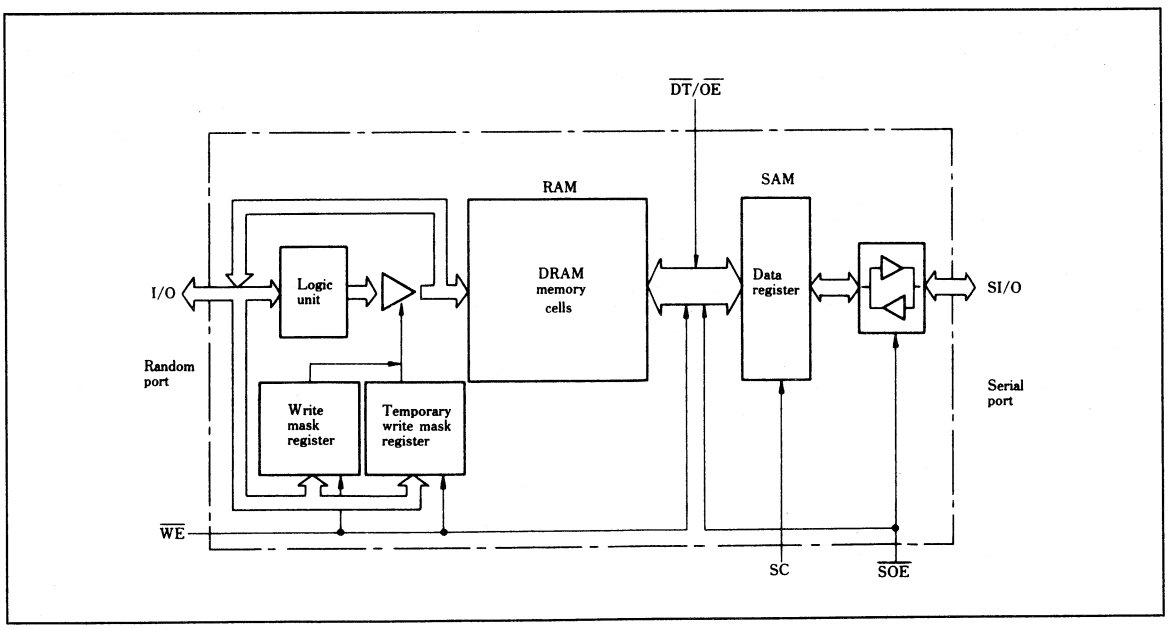


Figure 3-10 Block Diagram of HM53462/HM534252

Logic Operation Programming: This function programs a logic operation (Figure 3-11). The logic operation is available until the device is reprogrammed or reset. In the logic operation mode, the HM53462/HM534252 performs read-modify-write internally when data is written into the random port. The result of the logic operation between memory data and written data is placed into the address from which the memory data is transferred.

In the logic operation programming cycle, the mask register, which differs from the temporary mask register, is also programmed. It is available until reprogrammed.

Notes: Notes on using HM53461/HM534251/HM53462/HM534252 are as follows.

- Dummy $\overline{RAS}$ cycle
  Devices should be initialized by eight dummy $\overline{RAS}$ cycles (minimum) before accessing the random port. The refresh cycle can be inserted for initialization. It is recommended that the system be initialized by a dummy $\overline{RAS}$ cycle in the automatic reset time of the processor.

- Bypass capacitor
  One bypass capacitor should be inserted between V_{CC} and V_{SS} to each device. The V_{CC} pin should be connected to the capacitor by the shortest path. A capacitor of several μF is suitable.

- Negative voltage input
  A negative polarity input level to an input pin or I/O pin should be above −1 V. In this range, it has no effect on the device characteristics or RAM/SAM data retention.

- Initialization of logic operation mode (HM53462/HM534252)
  The logic operation programming cycle should be executed before accessing the random port to initialize the logic operation mode after power on. At this time, the operation codes (0101) and all 1 write mask data are recommended.

Table 3-2 Operation Modes of HM53462/HM534252

At the Falling Edge of $\overline{RAS}$					SAM Modes	
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WE}$	$\overline{SOE/SE}$	RAM Modes	SI/O Direction	Notes
H	H	H	X	Read/write	S_{in}/S_{out}	1, 2, 3
H	H	L	X	Temporary masked write	S_{in}/S_{out}	1, 2, 3
H	L	H	X	Read transfer	S_{out}	2
H	L	L	L	Write transfer	S_{in}	
H	L	L	H	Pseudo transfer	S_{in}	
L	X	X	X	$\overline{CAS}$-before-$\overline{RAS}$ refresh	S_{in}/S_{out}	1, 2
L	X	L	X	Logic operation program (CBR Refresh)	S_{in}/S_{out}	1, 2

H: High, L: Low X: Don't care

Notes:

1. The transfer cycle previously executed defines SI/O direction.
2. SI/O is in high impedance with $\overline{SOE}$ high, even if the direction is S_{out}.
3. The HM53462/HM534252 writes if $\overline{WE}$ is low at the falling edge of $\overline{CAS}$ or becomes low between the falling edge of $\overline{CAS}$ and the rising edge of $\overline{RAS}$.

3.2 Line Memory

Hitachi has produced a line memory for video line buffers with simple circuits providing specific functions as described below.

The line buffer can improve picture quality by storing one horizontal line of data. It has the following features.

- Capacity to store one horizontal line data.
- High speed operation matching the sampling speed of PAL TV signal (4 f_{SC}/8 f_{SC}) or NTSC TV signal (4 f_{SC}/8 f_{SC}).
- Separate data inputs/outputs and capability of serial data inputs and outputs.

The conventional line buffer, composed of high speed static RAM, requires separate input/output capabilities for a double buffered organization. It also requires interleaving for high speed operation, matching 4 f_{SC}/8 f_{SC}, where f_{SC} is the subcarrier frequency. In addition, external circuits are needed for serial address scan.

The line memory provides all of these functions. Figure 3-12 shows the standard organization of a conventional memory buffer, and Figure 3-13 shows the block diagram of line memory.

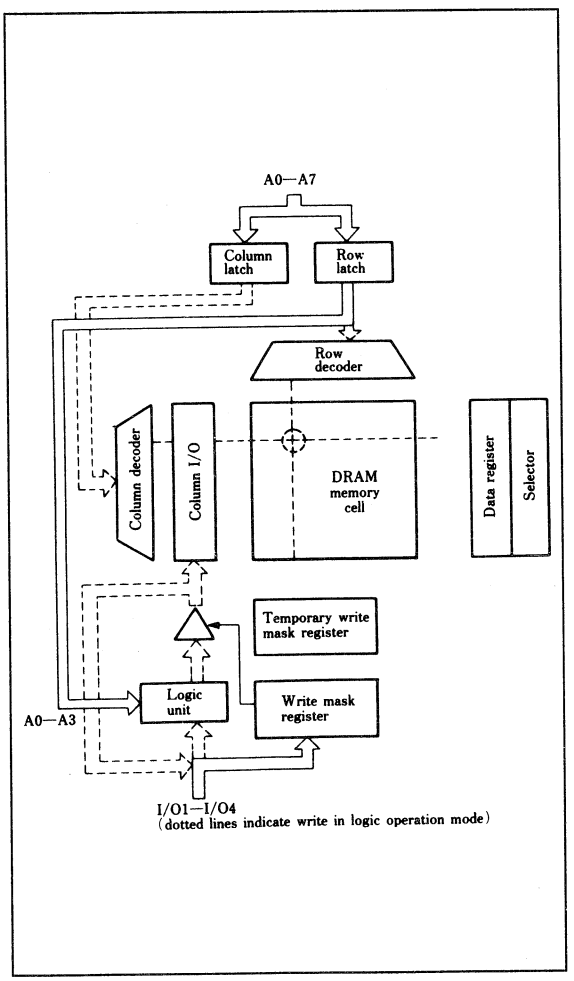


Figure 3-11 Logic Operation Programming

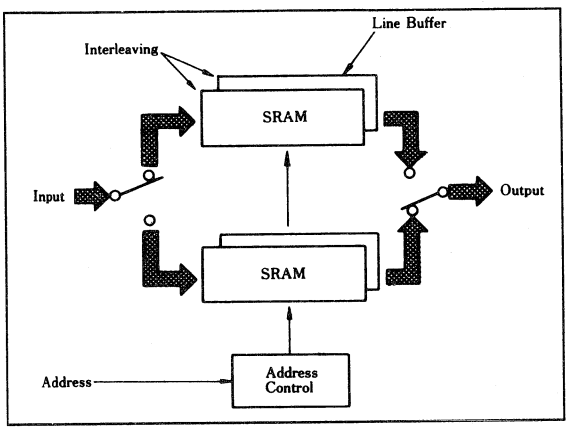


Figure 3-12 Standard Organization of Conventional Line Buffer

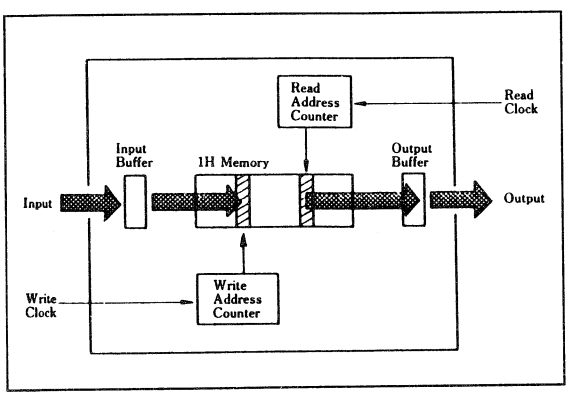


Figure 3-13 Block Diagram of Line Memory

Application

The Hitachi HM63021 is a 2048 word × 8-bit line memory storing two horizontal lines of data.

It has five different modes for various video graphic system applications. It realizes high speed operations for PAL and NTSC TV signals, and dissipates little power, employing 1.3 µm CMOS technology and static-type memory cells.

The features of the HM63021 are described as follows.

- Five modes for various video graphic system applications
  - — Delay line mode
  - — Alternate 1H/2H delay mode
  - — TBC (Time-Base Corrector) mode
  - — Double speed conversion mode
  - — Time-base compression/expansion mode
- High speed cycle time
  - — HM63021-45: 45 ns min
  - — HM63021-34: 34 ns min (corresponds to 8 f_{sc} of NTSC TV signal)
  - — HM63021-28: 28 ns min (corresponds to 8 f_{sc} of PAL TV signal)

The line memory in a system using digital signal processing technologies offers the following features.

- — Comb filter
- — Double-speed conversion (non-interlace)
- — Compression/expansion of graphics (picture-in-picture)
- — Dropout canceller
- — Time-base corrector
- — Noise reducer

4. Dynamic RAM (4-Mbit DRAM)

4.1 Dynamic RAM Memory Cell

The dynamic RAM memory cell consists of 1 MOS transistor and 1 capacitor, as shown in Figure 4-1. It detects the data in the cell (1 or 0) by the charge stored in the capacitor. Dynamic RAM offers a higher density than static RAM because it uses fewer components per chip.

However, dynamic RAM data must be rewritten (called refresh) in a defined cycle, because the charge stored in the capacitor leaks.

4.2 Power On Procedure

After turning on the power to set the internal memory circuitry, wait for more than 100 μs, then apply eight or more dummy cycles before operation. The dummy cycles must be either $\overline{RAS}$- only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles. When using an internal refresh counter, eight or more $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required as dummy cycles.

4.3 Address Multiplexing

Dynamic RAM devices are used to increase capacity because of their smaller cell area. In using dynamic RAM in systems, however, it is desirable to increase memory density by using even smaller packages. To reduce the number of pins and the package size, address multiplexing is used.

Using a 4-Mbit dynamic RAM, 22 address signals are necessary to select one of 4,194,304 memory cells. Address multiplexing allows address signals to be applied to each address pin. Thus only 11 address input pins are required to select one of 4,194,304 addresses. The multiplexed address inputs are latched as follows: $\overline{RAS}$ (row address strobe) selects one word line according to the row address signal, and one column decoder is selected by $\overline{CAS}$ (column address strobe) following a column address signal. Although two extra signals, $\overline{RAS}$ and $\overline{CAS}$, are required, the number of address pins is reduced by one-half. Figure 4-2 shows the pin arrangement, address latch waveform, and the block diagram of address-multiplexed 4-Mbit dynamic RAM. Systems require an address multiplexer in order to latch the multiplexed address signals into the device.

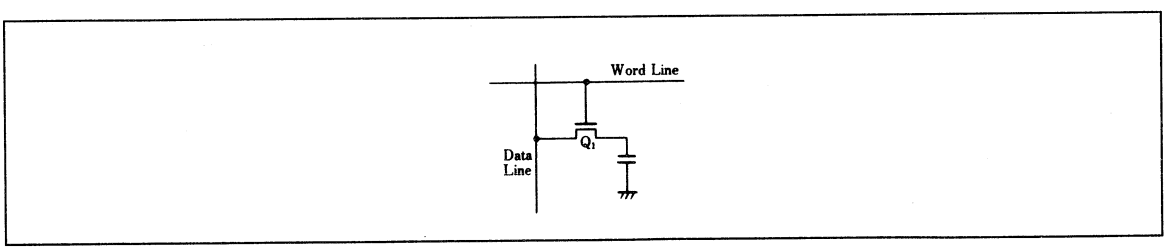
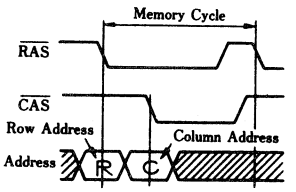


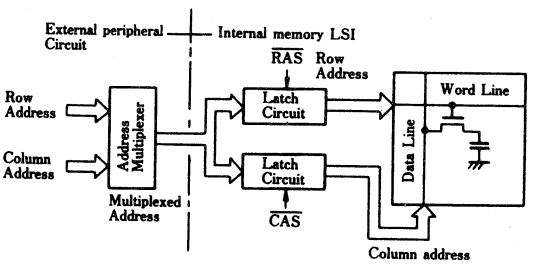
Figure 4-1 Memory Cell of Dynamic RAM

A_0 to A_{10}	Address input
$\overline{CAS}$	Column address strobe
D_{in}	Data in
D_{out}	Data out
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Read/write input
V_{CC}	Power (+5 V)
V_{SS}	Ground
A_0 to A_9	Refresh address inputs

(a) Pin Arrangement



(b) Address Latch



(c) Block diagram of Address Multiplexing

Figure 4-2 Address Multiplexing of Dynamic RAMs

4.4 Dynamic RAM Function

Figure 4-3 shows the normal function of the dynamic RAM.

Read Cycle: In the read cycle, a row address is latched at the falling edge of $\overline{RAS}$, and a column address is latched at the falling edge of $\overline{CAS}$ after the $\overline{RAS}$ falling edge. If $\overline{WE}$ is high, the data is read out from D_{out} with the access time of t_{CAC} (access time from $\overline{CAS}$) or t_{RAC} (access time from $\overline{RAS}$).

The t_{RCD} maximum ($\overline{RAS}$ to $\overline{CAS}$ delay time) is specified only to guarantee the specified minimum values of other timings such as the cycle time and $\overline{RAS}/\overline{CAS}$ pulse width. Therefore, when using these timings at values hgher than the specified minimum value, there is no need to limit the t_{RCD} to the specified maximum value.

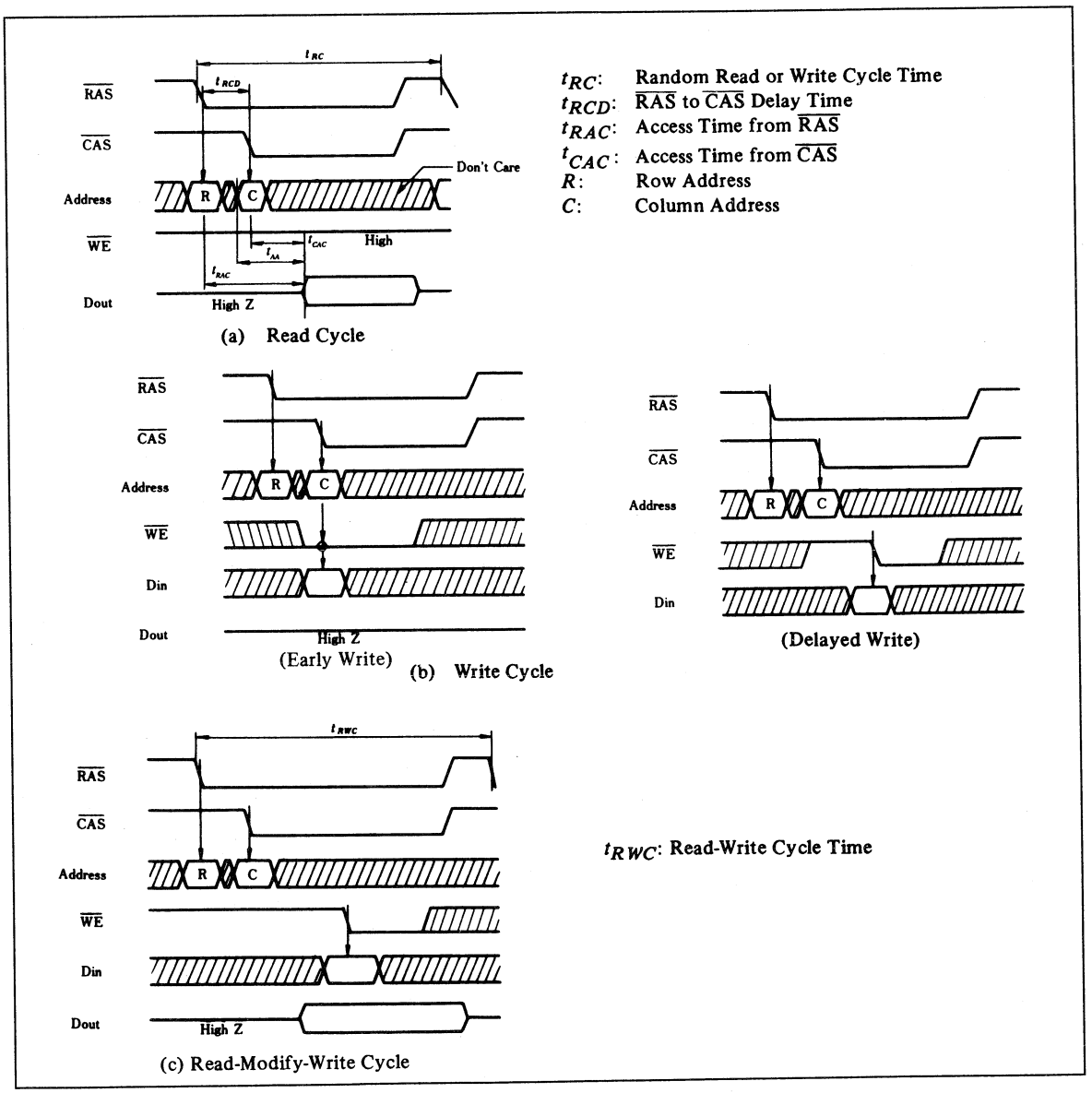


Figure 4-3 Normal Function of Dynamic RAM

Write Cycle: The dynamic RAM provides two write cycle modes: early write cycle and delayed write cycle. In the early write cycle, when $\overline{WE}$ is low, data is written into D_{in} at the falling edge of $\overline{CAS}$. In the delayed write cycle, data is written into D_{in} at the falling edge of $\overline{WE}$ after $\overline{CAS}$ falls.

Read-Modify-Write Cycle: The read-modify-write cycle is initiated by setting $\overline{WE}$ high. Data is read out from D_{out} at the falling edge of $\overline{CAS}$ with $\overline{WE}$ high. Then, if $\overline{WE}$ goes low, data is written into the same address from D_{in} in the same cycle.

The cycle time in the read-modify-write mode (t_{RWC}) is longer than the cycle time in read/write mode (t_{RC}).

4.5 High Speed Access Mode

The dynamic RAM access time is typically longer than that of static RAMs. To achieve a higher speed operation, high speed access modes are implemented. The read operation in the dynamic RAM is performed as follows:

When a word line is selected by the row address, all data in the memory cells connected to the selected word line are transferred to sense amplifiers. One of these sense amplifiers is then selected by the column address, and its contents are output.

Data output from other sense amplifiers are controlled only by the column address.

Access controlled only by the column address, with the row address fixed, is called the high speed access mode. Table 4-1 compares each mode.

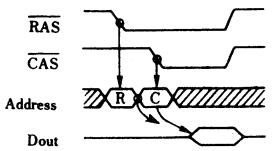
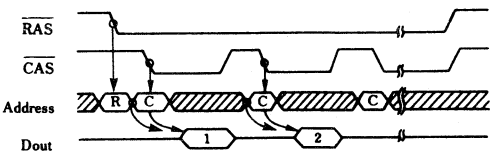
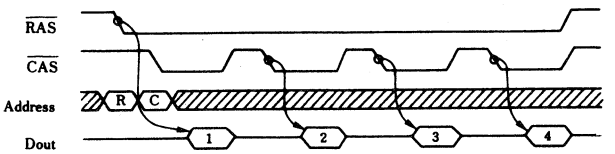
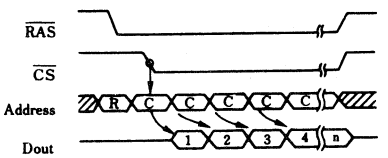
Fast Page Mode: This is the most typical access mode in dynamic RAM. The column address is switched synchronously with the $\overline{CAS}$ rising edge.

Nibble Mode: In a nibble mode dynamic RAM, data from four sequential addresses is stored in the 4-bit output latch circuits. The output is provided by the $\overline{CAS}$ signal which controls the latch circuits.

When four addresses are accessed sequentially, the row addresses on and after the second bit need not be selected. This facilitates timing design. In nibble mode, although the operation is limited to four addresses, however, it enables faster access (t_{NAC}) than page mode.

Static Column Mode: In the static column mode, the column address is switched without the synchronized signal by high speed static RAM technology in the peripheral circuits.

Table 4-1 Comparison of Dynamic RAM High Speed Access Modes

Normal mode	 R : Row Address C : Column Address
Fast Page mode	
Nibble mode	
Static column mode	

4.6 Refresh

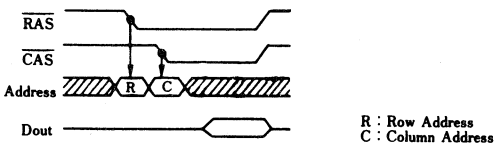
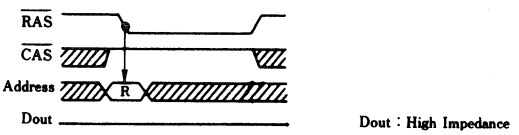
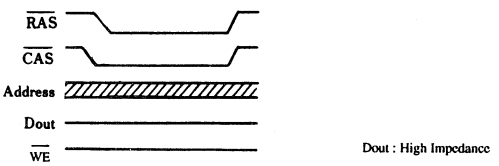
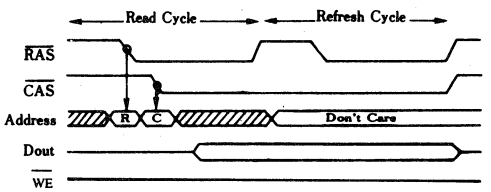
The refresh operation is performed by accessing every word line within the specified time (refresh cycle). Table 4-2 compares the following refresh modes in dynamic RAM.

$\overline{\text{RAS}}$-Only Refresh: In the $\overline{\text{RAS}}$-only refresh mode, refresh can be completed by selecting only row addresses synchronized with $\overline{\text{RAS}}$.

$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh: This mode refreshes by the $\overline{\text{CAS}}$ falling edge before $\overline{\text{RAS}}$ in the period defined by the internal refresh address generator. This mode simplifies the external address multiplexer.

Hidden Refresh: In the hidden refresh mode, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh is performed while output data is valid.

Table 4-2 Comparison of Dynamic RAM Refresh Modes

Read	
$\overline{\text{RAS}}$-only refresh	
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh	
Hidden refresh	

: Don't care

5. EEPROM

5.1 EEPROM Memory Cell

An EEPROM is an electrically erasable and programmable ROM which can be erased or written remotely while the system is in operation.

Hitachi EEPROM memory cells are MNOS-type (Metal Nitride Oxide Semiconductor) as shown in Figure 5-1.

A MNOS memory cell consists of two layers of oxide film and nitride film. The thickness of the oxide film is about 20 Å and the nitride film is 300 to 500 Å. There are traps in the boundary of the oxide and nitride films to catch electrons. The electrons move by the tunneling phenomenon between the substrate and traps.

5.2 CMOS EEPROM Function

Page Programming Function: The CMOS EEPROMs can latch page data and write them in single write cycle. The write cycle time is specified as 10 ms (max.). The effective byte programming speed in page write mode is 10 ms/32 bytes = 0.31 ms/byte in case of HN58C65.

Thus it takes only 2.56 seconds to write the entire HN58C65. Figure 5.2 shows the internal operation in case of HN58C65. The following describes the operation sequence:

1. The 32-byte memory cell data at the row address selected by address pins A5–A12 are latched.

2. Latched data at the column address specified by address pins A0–A4 are altered with write data, which is put into the D_{in} buffer from I/O pins I/O0–I/O7.
   The 32 bytes (max.) of latched data are altered by repeating this operation 32 times.

3. 32 bytes of memory cell data in the selected row 1 are erased (all set to 1).

4. Latched data is written into the selected row 3.

5. CPU acknowledges completion of the write cycle based on the internal timer. The HN58C65 provides RDY/$\overline{\text{BUSY}}$ and $\overline{\text{DATA}}$ polling to indicate the write completion.

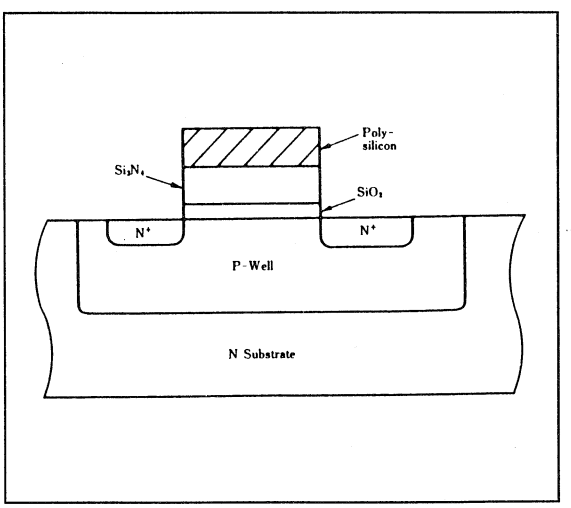


Figure 5-1 MNOS-Type Memory Transistor

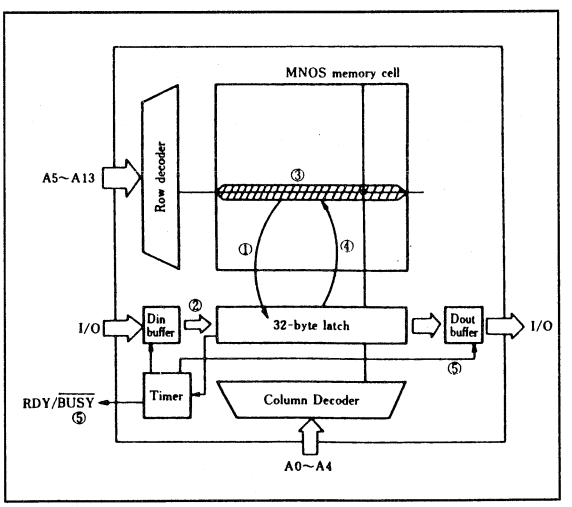


Figure 5-2 HN58C65 Page Write

Internal Timer: The CMOS EEPROMs indicates the completion of a data write to the CPU by using an internal timer. They enter the next cycle as soon as the completion of the write is detected. This function offers a high system throughput as the CPU can access other devices during a write cycle. They have two functions, RDY/$\overline{\text{BUSY}}$ and $\overline{\text{DATA}}$ polling, to indicate the completion of data write.

The RDY/$\overline{\text{BUSY}}$ approach indicates the completion of data write by using pin 1. It is low when the HN58C65 is in data write operation ($\overline{\text{BUSY}}$) and turns to the high impedance state at the end of data write (RDY). The RDY/$\overline{\text{BUSY}}$ pin should be pulled up as it uses open drain output. The RDY/$\overline{\text{BUSY}}$ pins can be OR-wired when using several EEPROMs.

The $\overline{\text{DATA}}$ polling approach, implemented in software, indicates the completion of data write through pin 19 (I/O7). While the data write is not completed, I/O7 shows an inverted version of what was written in the last cycle. In using this approach, the RDY/$\overline{\text{BUSY}}$ pin should be opened or grounded. The $\overline{\text{DATA}}$ polling approach can acknowledge the completion of a data write in an individual EEPROM, even if several HN58C65's are used in the system.

Data Protection: The EEPROM performs a data write with a higher voltage (V_{PP}) than the power supply voltage (V_{CC}). The CMOS EEPROMs internally generate V_{PP} by a high voltage generator with the combination of control pins ($\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$). It supports the following functions to avoid accidental data write (data protection).

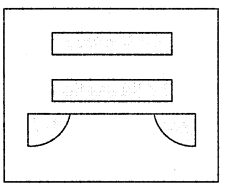
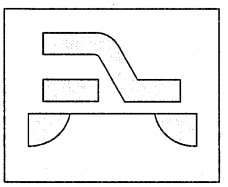
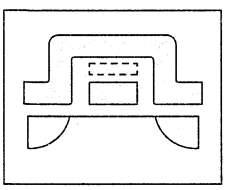
1. Data protection against noise on the control pins ($\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$) during operation.
2. Data protection against noise at power on/off.

6. FLASH MEMORY

Table 6-1 shows the sectional structure of a Flash Memory which is called stack cell. The upper gate, one of the gates made of two layered poly silicon is called the control gate and is connected to a word line. The lower layer is called the floating gate and is not connected.

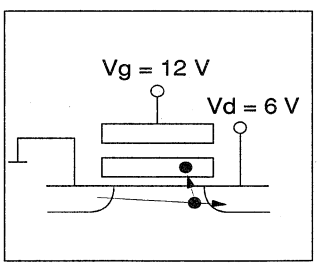
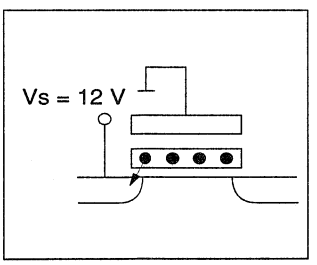
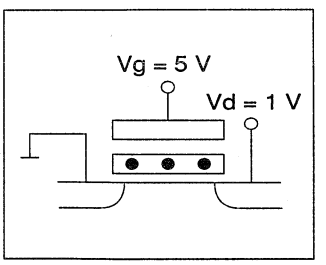
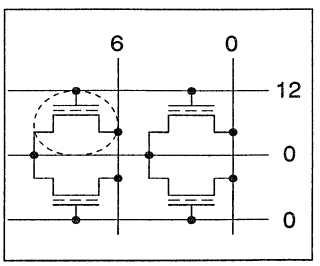
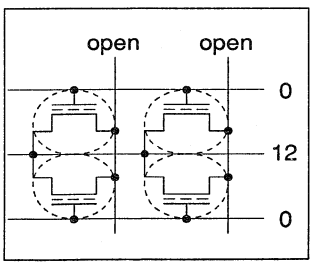
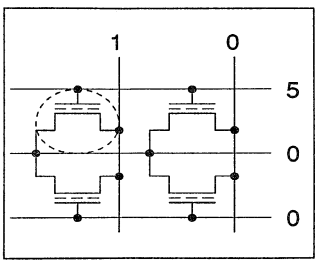
The advantage of the stack type cell are small memory size, fast programming time, and process simplicity. Table 6-2 shows the operation of the stack memory cell.

Table 6-1 Comparison of Memory Cell Types

Type	Stack	Split Gate	Three-Layer Poly-Si
Structure			
Cell Size	EA		
Programming Time	A		
Erasing Time			A
Programming Durability	A		A
Sector Erasing		A	

EA: Especially advantageous A: Advantageous

Table 6-2 Operation Principle of Stack Type Memory Cell

	Program	Erase	Read
Memory Cell			
Memory Array			

Programming is accomplished by applying a high voltage to the gate and drain, so that hot electrons are injected into the floating gate and data is programmed. The threshold voltage increases after programming like EPROMs.

Erasure is accomplished as chip erase by grounding the gate and applying a high voltage to the source so that electrons accumulated on floating gates are taken out by the tunnel effect. The threshold voltage decreases after erasure. The threshold voltage increases after programming.

Read operation is accomplished by applying V_{CC} voltage to the gate and detecting the drain current corresponding to the threshold voltage level. An excessive erasure makes the threshold voltage negative to cause miss operation.

Erase operation has to be accomplished after all bits of data are programmed to equalize the threshold voltage level. Then, the erase operation advances step by step with verifying memory data, and finishes with having verified all bits erased. The erase operation has to be controlled by the algorithm shown in Figure 6-1. Hitachi adopts not only conventional erasure function controlled by external CPU, but also automatic erasure function controlled by built-in erase circuits, so that the automatic erasure function releases CPU from controlling the complicated algorithm. Block Diagram of automatic erase is shown in Figure 6-2.

Programming Durability Data is shown in Figure 6-3.

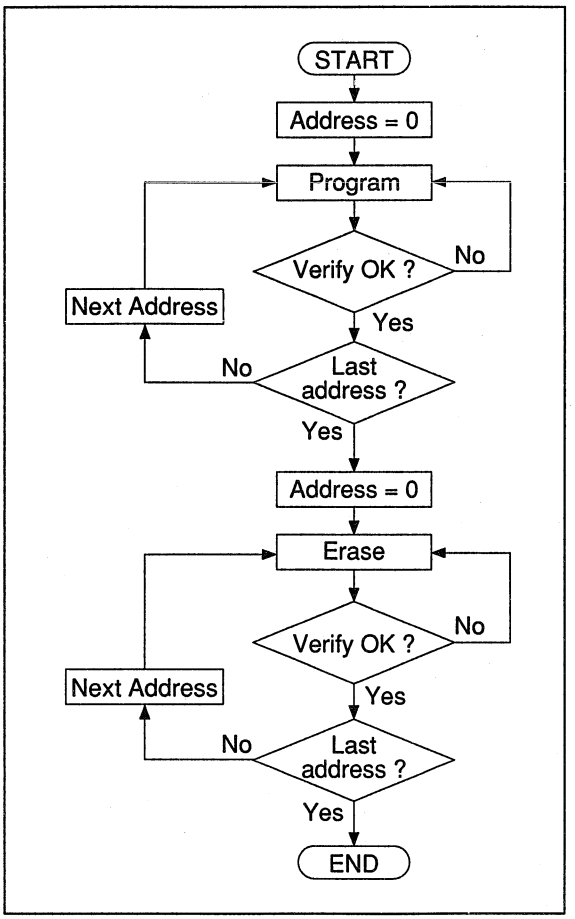


Figure 6-1 Most Suitable Erase Algorithm

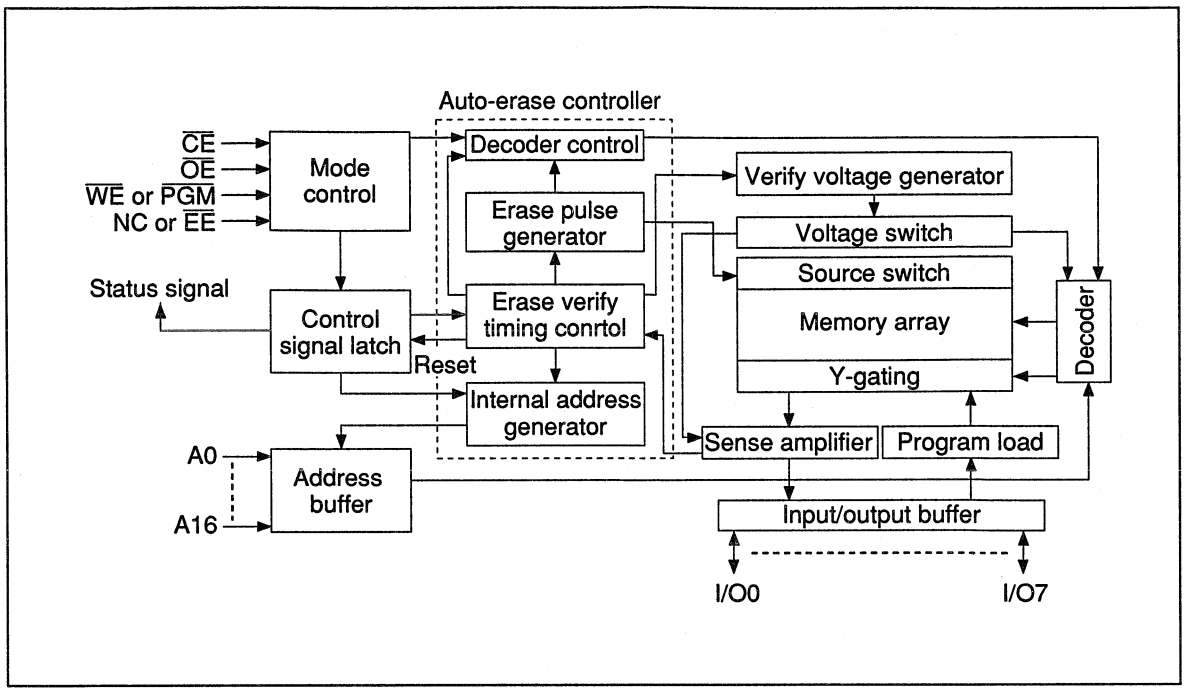


Figure 6-2 Block Diagram of On-chip Automatic Erase

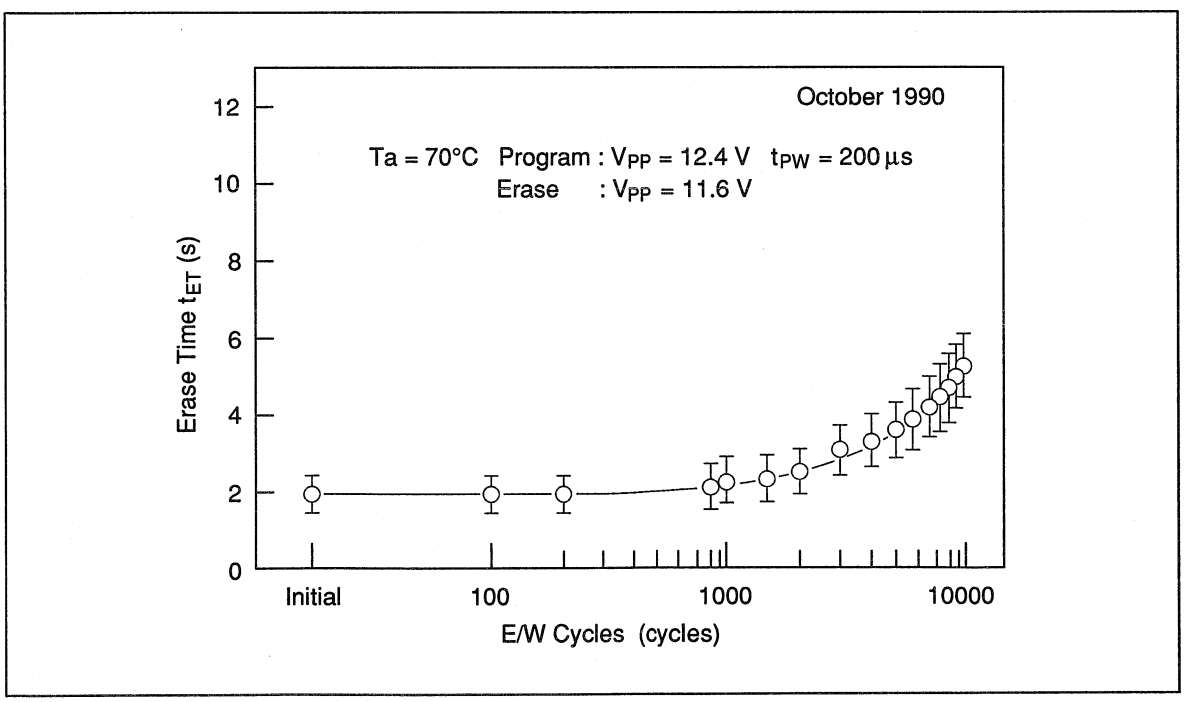


Figure 6-3 Erase Time vs. E/W Cycles (Programming Durability Data)

7. EPROM/OTPROM

7.1 EPROM Programming

Figure 7-1 shows the sectional structure of an EPROM memory cell. The upper gate, one of the gates made of two-layered polycrystalline silicon, is called the control gate and is connected to a word line. The lower layer is called the floating gate and is not connected. This memory cell is programmed as follows.

With the substrate and source grounded, apply a high voltage between the drain and control gate. An electrical potential incline will occur between the source and drain so that the intensity of the electric field will become high near the drain. Because of this electric field, electrons are accelerated and the so-called hot electrons will be generated, which jump over the energy barrier of SiO_2 film. The hot electrons are pulled by the electric potential of the control gate and poured into the floating gate. Electrons stored in the floating gate remain stable as they fall into a well surrounded by an energy barrier of SiO_2 film. Therefore, it is evident that the quality of the SiO_2 film surrounding the floating gate is essential for good data retention characteristics. To keep data retention in the 5- or 10-year range, high quality SiO_2 film is needed.

Figure 7-2 shows the fundamental characteristics of the EPROM transistor. While I_D in a non-programmed transistor begins to flow with V_G of about 1 V, the current in a programmed transistor does not flow until V_G rises to 7 to 10 V. Therefore, if the voltage of the word line applied to the control gate is about 5 V in the readout, a non-programmed memory transistor will be on, and the programmed memory transistor will be off. This means that the data can be read out by means of the same structure as a NOR-type mask ROM.

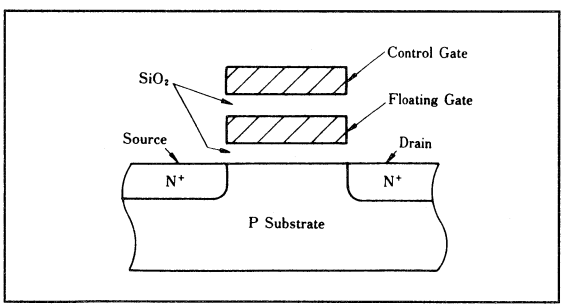


Figure 7-1 Cross Section of a EPROM Memory Cell

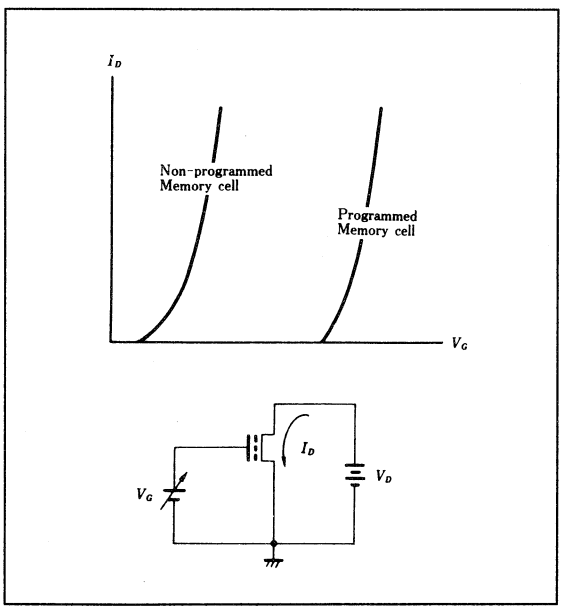


Figure 7-2 Fundamental Characteristics of a EPROM Memory Cell

7.2 Erasing EPROM

When shipped, all bits of the EPROM are at logic 1 with all electrons in the floating gate released (erased). Changing the logic 1 to logic 0, through the application of the specified waveform and voltage, programs the necessary information. The higher the V_{PP} voltage and the longer the program pulse width t_{PW}, the more electrons can be programmed in as shown in Figure 7-3. If V_{PP} exceeds the rated value, such as by overshoot, the pn junction of the memory may yield to permanent breakdown. To avoid this, check V_{PP} overshoot of the PROM programmer. Also, check negative-voltage-induced noise at other terminals, which can create a parasitic transistor effect and reduce the yield voltage. Hitachi's EPROMs can usually be written and erased more than 100 times.

EPROMs are erased by ultraviolet light exposure through a transparent window on the package. Electrons in the floating gate get energy from photons and become hot electrons again with enough energy to go over the energy barrier of SiO_2 film. The hot electrons go through to the control gate or the substrate and erasure is completed. Therefore, light with enough energy to get the electrons over the energy barrier of SiO_2 film is needed for erasure. Light energy is proportional to its frequency, and described as E = hv. E is the energy of light, h is Planck's constant, and v is light frequency. Erasure is not caused by light over certain wavelengths and under certain wavelengths. However, the erasure time depends upon the quantity of photons, therefore the erasure time cannot be shortened by using a shorter wavelength. Figure 7-4 shows the relation between wavelength and erasure effectiveness. Erasure starts at about 4000 Å and is saturated at about 3000 Å.

For erasure, the wavelength and minimum irradiation rate of ultraviolet light must be 2537 Å and 15 W·s/cm^2 respectively. These conditions can be met by placing the device 2 to 3 cm below a 12,000 W/cm^2 UV lamp for about 20 minutes.

The UV transmittance of the transparent lid materials is about 70%. However, it is influenced by contamination or foreign materials on the lid surface. The contamination or foreign materials should be removed with a solvent that does not damage the package.

Figure 7-5 shows the EPROM standard erasure characteristics.

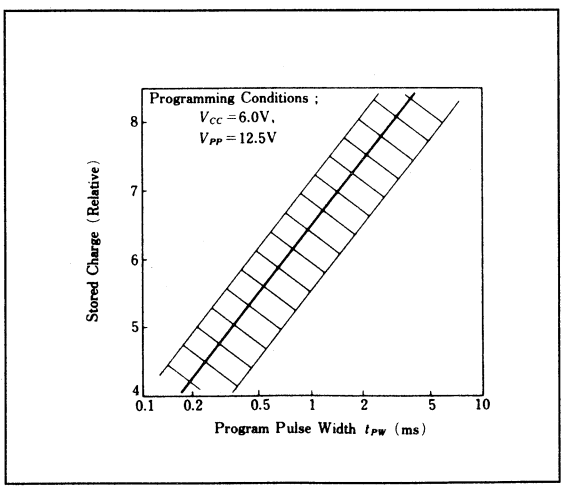


Figure 7-3 Standard Programming Characteristics of EPROMs

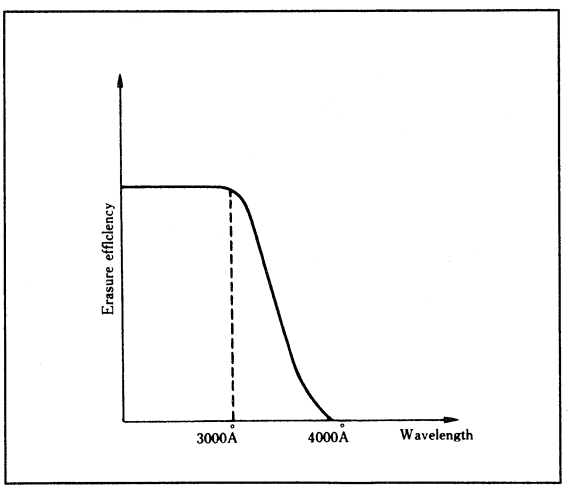


Figure 7-4 Erasure Efficiency of EPROM

7.3 EPROM Data Retention Characteristics

About 2 to 20 × 10^{-14} coulombs of electrons are accumulated in the floating gate when programmed. However, these electrons dissipate with time and the data may be inverted. The mechanism of electron dissipation is generally explained as follows.

Data Dissipation by Heat: The electrons at the floating gate are in a non-equilibrium state, so the dissipation of electrons by thermal energy is unavoidable. Therefore, the data retention time depends on temperature. Figure 7-6 shows typical data retention characteristics. The data retention time is proportional to the reciprocal of absolute temperature.

Data Dissipation by Ultraviolet Light: Ultraviolet light at a wavelength no greater than 3000 to 4000 Å is capable of releasing the electric charge at the floating gate of the EPROM with varying efficiencies. Fluorescent light and sunlight contain some ultraviolet light, and so prolonged exposure to these lights can cause data corruption as a result of electric charge dissipation. Figure 7-7 shows the standard data retention time under an ultraviolet eraser, sunlight, and fluorescent lighting.

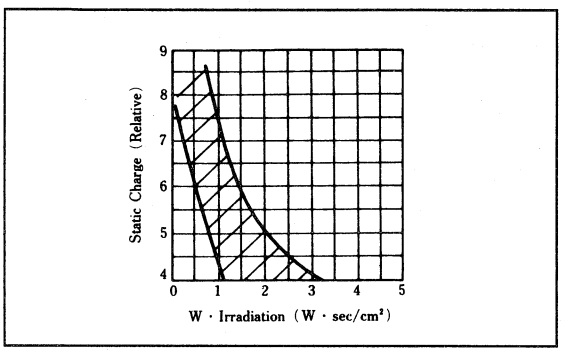


Figure 7-5 Standard Erasure Characteristics

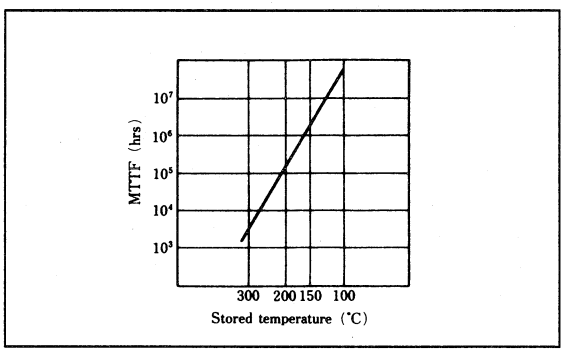


Figure 7-6 EPROM Data Retention Characteristics

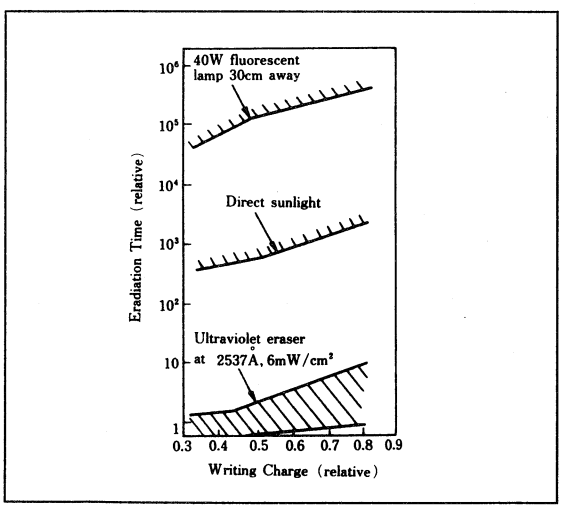


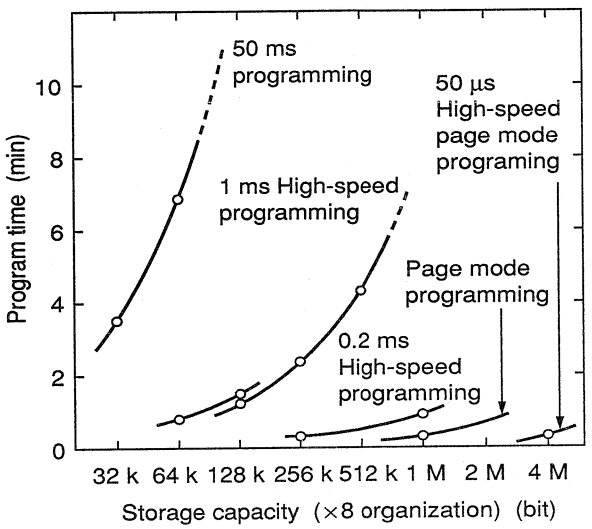
Figure 7-7 EPROM Data Retention Time

7.4 Optimized High Speed Programming

With the increase of EPROM density, the time for programming becomes more important. Methods for high speed programming have been developed and put into practical use for each EPROM generation.

There are three methods for high speed programming.

Figure 7-8 shows the relative programming times of these methods.
Please refer to the data sheet about each programming method.



Note: Actual programing time differs depending on the programmer.

Figure 7-8 Comparison of Shortened Programming Time

7.5 Device Identifier Code

EPROM programming conditions depend on the EPROM manufacturers' standards and specific device types. Confusion on the proper use of varying methods required may cause poor or failing operation. As a countermeasure, some EPROMs provide embedded device identifier codes including such information as the manufacturer and device type. Some newly developed commercial EPROM programmers can set write conditions automatically by recognizing this code.

Different programming conditions are as follows.

1. Program voltage
2. Program timing
3. High performance programming algorithm
4. Pin configuration

The Hitachi EPROM has a device identifier code area adjacent to the memory access area as shown in Figure 7-9.

Table 7-1 describes how to use the device identifier code. Setting A9 at 12 V and A1–A8 and A10–A13 at V_{IL}, access the device identifier code area and I/O0–I/O7, and output the programming condition code with V_{IL} or V_{IH} of A0.

Table 7-1 Hitachi EPROM Device Identifier Code

		A_0	I/O8–I/O15	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Hex Data
Manufacturer code	Hitachi	V_{IL}	—	0	0	0	0	0	1	1	1	07
ROM code	HN27128A	V_{IH}	—	0	0	0	0	1	1	0	1	0D
	HN27256	V_{IH}	—	0	0	0	1	0	0	0	0	10
	HN27C256	V_{IH}	—	1	0	1	1	0	0	0	0	B0
	HN27C256H	V_{IH}	—	0	0	1	1	0	0	0	1	31
	HN27C256A	V_{IH}	—	0	0	1	1	0	0	0	1	31
	HN27512	V_{IH}	—	1	0	0	1	0	1	0	0	94
	HN27C1024H	V_{IH}	—	1	0	1	1	1	0	1	0	BA
	HN27C101A	V_{IH}	—	0	0	1	1	1	0	0	0	38
	HN27C301A	V_{IH}	—	1	0	1	1	1	0	0	1	B9
	HN27C4096	V_{IH}	—	1	0	1	0	0	0	1	0	A2
	HN27C4001	V_{IH}	—	0	0	1	0	0	0	0	0	20

A9: 12 V

A1–A8, A10–A13: V_{IL}

A14, A15: Don't care

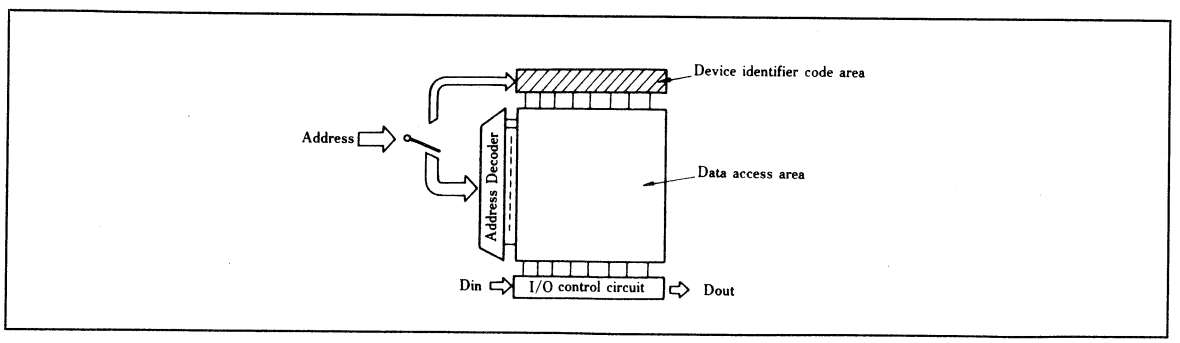


Figure 7-9 Device Identifier Code

7.6 Shielding Label

When using an EPROM in an environment where it can be exposed to ultraviolet light, Hitachi recommends placing a shielding label over the transparent lid to absorb the ultraviolet light. In choosing a shielding label, the following points should be carefully checked.

1. Adhesiveness (mechanical strength)
   Avoid repeated removal and reattachments, or exposure to dust that may reduce the adhesive strength. Ultraviolet erasure and reprogram-ming are recommended after stripping off an attached label. (When the need arises to change a label, it is advisable to place a new one over the old one since peeling may create a static charge.)

2. Allowable temperature range
   Use the shielding label in an environment where temperature is stable within the specified allowable temperature range. Beyond the specified temperature range, the paste on the label may harden or stick too tightly. When it hardens, the label may come off easily. When it sticks too tightly, the paste may remain on the window glass after the label has been removed.

3. Moisture resistance
   Use the shielding label in an environment where humidity is stable within the specified allowable humidity range.

7.7 EPROM Programmer

The EPROM programmer stores the user's program in its internal RAM and writes the program in the EPROM. For this programming, at least three functions are necessary: the blank check function prior to programming, programming function, and verify function after program-ming. Figure 7-10 shows the programming flowchart. Some programmers check for pin contact failure or reverse insertion before the blank check.

The outline of each check is as follows.

1. Pin contact check
   In the ROM pin and socket connection test, checking is normally performed by detecting forward current at each EPROM pin. Care is necessary as this forward biased resistance differs in products of each company.

2. Reverse insertion check
   This check detects the reverse insertion of the device, then places the equipment in reset mode and protects the device and equipment if the condition is found.

3. Blank check
   This check is performed before programming. It checks whether the device is an erased EPROM, or it prevents EPROM reprogram-ming. Since output data in the erased condi-tion is high, the check is for whether the data in the EPROM are all 1s. It will fail even if one bit is 0. Normally, it is designed to provide a warning with a lamp or buzzer.

4. Programming
   The function of programming the data from the internal RAM of the programmer into the EPROM will fail when programming cannot be done. The normal flow is as shown in Figure 7-11. The EPROM data for a target location will be read out prior to programming and compared with the programming data intended for that location. If the data matches, programming will be skipped. If they differ, programming will be performed. Then, the data will be read back and compared with the original programming data, and if they match, the programmer will progress to the next address.

5. Verify
   This function checks after programming completion whether or not the programming is correct when comparing with the data in the internal RAM of the programmer. It will fail when they do not match. Normally, when it fails, it lights the fail lamp and displays the address and data.

6. How to input a program
   Table 7-2 shows several methods for inputting the program data to the internal RAM of the programmer. Normally, paper tape input and teletypewriter input are preferred options.

7.8 Handling EPROMs

If touched by a charged human body or rubbed with plastics or dry cloth, the glass window of an EPROM generates static electricity which causes device malfunctions. Typical malfunctions are faulty blanking and write margin setting that give the false impression that information has been correctly written in. As already reported at international conferences concerning the reliability of LSI chips, this is due to the prolonged retention of electric charge (resulting from static electricity) on the glass window. Such malfunctions can be eliminated by neutralizing the charges by irradiating the EPROM with ultraviolet rays for a short time. The EPROM should be reprogrammed after this irradiation since it also reduces the electric charges in the floating gates. The basic countermeasure is to prevent the charging of the window, which can be achieved by the following methods, as in the prevention of common static breakdown of ICs.

1. Ground operators who handle the EPROM. Avoid using things such as gloves that may generate static electricity.
2. Avoid rubbing the glass window with plastic or other materials that may generate static electricity.
3. Avoid the use of coolant sprays which may contain some free ions.
4. Use shielding labels (especially those containing conductive substances) that can evenly distribute any established charge.

Table 7-2 EPROM Data Input

Method	Content
Copy input	Input by copying the master ROM.
Manual input	Input by the keyswitches on the front panel. Used for correction or revision of programs.
Paper tape input	Paper tape furnished from the host system is read with the tape reader.
Teletypewriter input	Input with the teletypewriter. Preparation, correction, and list preparation of the program can be made.

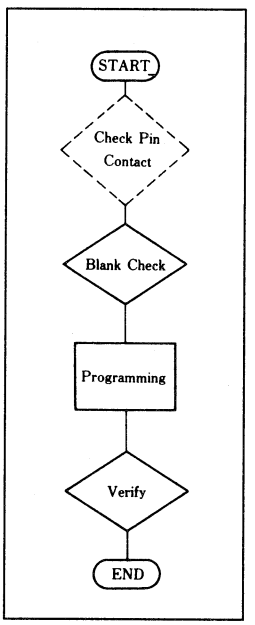


Figure 7-10 Programming Flowchart of EPROM Programmer (1)

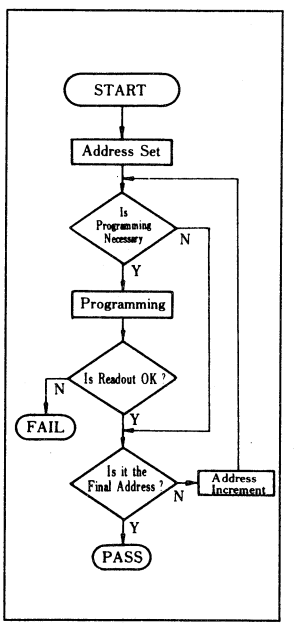


Figure 7-11 Programming Flowchart of EPROM Programmer (2)

7.9 Ensuring OTPROM Reliability

The one-time-programmable ROM (OTPROM) has two forms: standard dual in-line package (DIP) and small outline package (SOP). It is only one-time programmable because it has no window for ultraviolet light exposure; testing by programming and erasure cannot be performed after it is assembled.

As a means of improving reliability, Hitachi performs screening tests for programming, access time, and data retention on OTPROM wafers during the manufacturing process.

However, rare defects may occur in the assembly process that cannot be completely removed in the final test screening which is only a reading test. Therefore, Hitachi recommends that users perform high temperature baking after programming these devices to ensure the highest reliability.

Detailed conditions and procedures for screening are shown in Figure 7-12. First, program and verify the devices. Then leave them without bias at 125 to 150°C for 24 to 48 hours.

After that, check the readout function, and discard chips with data retention failures.

From the results of devices in which the recommended screening test is properly performed, we find the data retention characteristics of OTPROMs are generally equal to EPROMs.

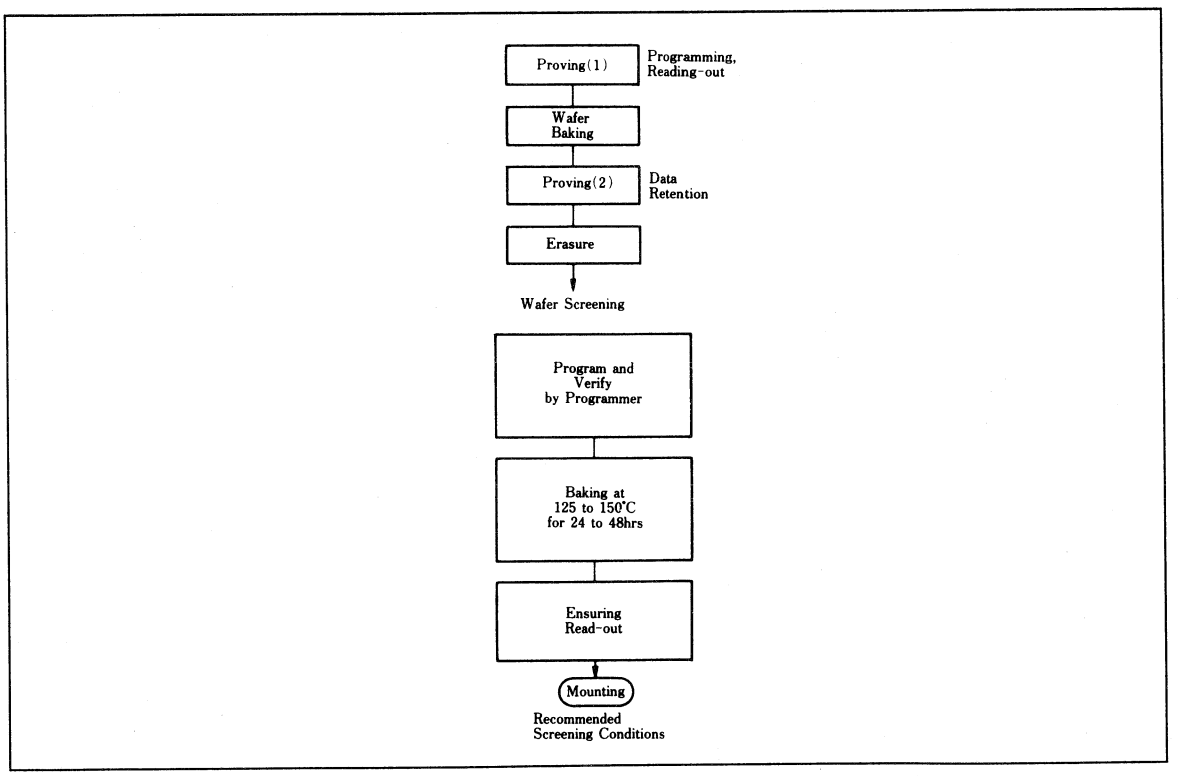


Figure 7-12 Screening Flowchart of OTPROM

8. Mask ROM Programming Instruction

The writing of custom program code into mask ROMs is performed by a CAD system on a large-scale computer. ROM code data should conform to the specifications given below, using either EPROM or floppy disk. Additional instructions, such as chip select or customer part numbers, should be noted on the "ROM Specification Identification Sheet."

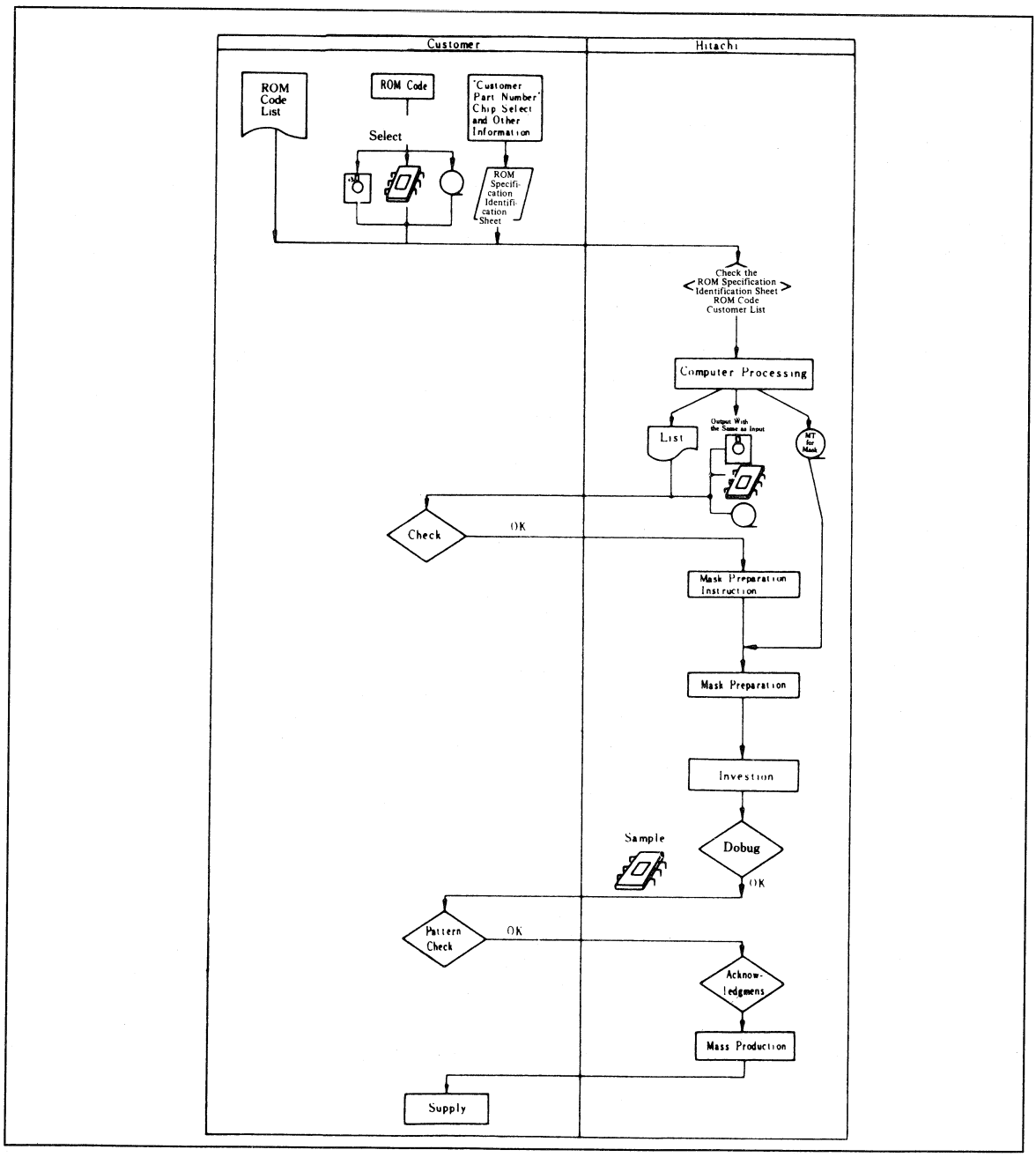


Figure 8-1 Mask ROM Development Flowchart

9. Instructions for Using Memory Devices

9.1 Prevention of Electrostatic Discharge

As semiconductor memory designs are based on a very fine pattern, they can be subject to malfunction or defects caused by static electricity. Though the built-in protection circuits assure unaffected reliability in normal use, devices should be handled with these precautions:

1. In transporting and storing memory devices, place them in a conductive magazine or wrapper, or put all pins of each device into a conductive mat, so that they are kept at the same potential. Manufacturers should give sufficient consideration on proper packing when shipping their products.

2. When the devices are to be touched during mounting or inspection, the handler must be grounded. Do not forget to connect a resistor (1 MΩ approximately is desirable) in series for protect 10 n against electrical shock.

3. Keep the relative ambient humidity at about 50% during processing.

4. For working clothes, cotton is preferable to synthetic fabrics.

5. Use a soldering iron operating at low voltage (12 V or 24 V, if possible) with its tip grounded.

6. When transporting a board with memory devices mounted on it, enclose it with conductive materials.

7. Use conductive materials of high resistance (about 10^9 ohms) to protect the devices from electrostatic discharge. Otherwise, if accidentally put in contact with conductive materials such as a metal sheet, the devices may deteriorate or even breakdown, owing to the sudden release of charge stored on the surface.

8. Never set a system in which memory devices are used near anything that generates high voltage (e.g., a CRT anode electrode, etc.).

9.2 Using CMOS Memories

As shown in Figure 9-1, the input of a CMOS memory is connected to the gate of an inverter consisting of PMOS and NMOS transistors. Figure 9-2 shows the relationship between the input voltage and current within the inverter. The top and bottom transistors turn on and create a current flow when the input voltage reaches an intermediate level. Therefore it is necessary to keep the input voltage below 0.2 V or above V_{CC} – 0.2 V in order to minimize power consumption. The data sheet specifies the standby current for two cases of input level (with minimum V_{IH} and maximum V_{IL}, and with 0.2 V or V_{CC} – 0.2 V), and the difference in values as being remarkably great. Some memory devices are designed to cut off such current flow in the standby mode by the control of input signals, but this depends on the specific device type. This should be confirmed in data sheets for each device type.

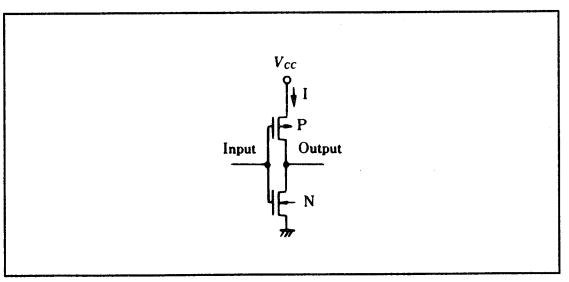


Figure 9-1 CMOS Inverter

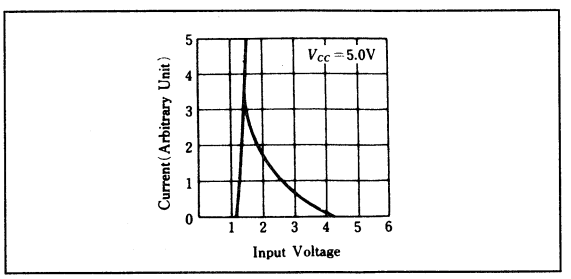


Figure 9-2 Relationship Between Input Voltage and Current in a CMOS Inverter

Another problem peculiar to CMOS devices is latch up. Figure 9-3 shows the cross section of a CMOS inverter and the structure of a parasitic bipolar transistor. The equivalent circuit of the parasitic thyristor is shown in Figure 9-4. When positive DC current or pulse noise is applied (Figure 9-4a), T_{R3} is turned on owing to the bias voltage generated between the base and emitter. Also, trigger current flows to ground through R_P, the base resistance of T_{R2}. As a result, T_{R2} becomes conductive and the current flows from power supply (V_{CC}) through the base resistance of T_{R1} (R_N), which also puts T_{R1} into conduction. Then as the base of T_{R2} is rebiased by the collector current from T_{R1}, the closed loop consisting of T_{R1} and T_{R2} reacts. Thus, current flows constantly between the power supply (V_{CC}) and ground even without the trigger current caused by outside noise.

Latch up can also be caused by a negative pulse (Figure 9-4 b). Most semiconductor memory manufacturers are trying to improve latch up immunity in their products. Hitachi provides a broad enough guard band by applying a diffusion layer around the inputs and outputs, taking care not to connect the input to the p^+ diffusion layer. The input voltage for the 64-kbit static RAM HM62256, for example, is specified as follows:

V_{IH} max 6.0 V (not dependent on V_{CC})
V_{IL} min 3.0 V (pulse width = 50 ns)
–0.5 V (DC level)

Thus almost no consideration for latch up is required in system designs using these devices.

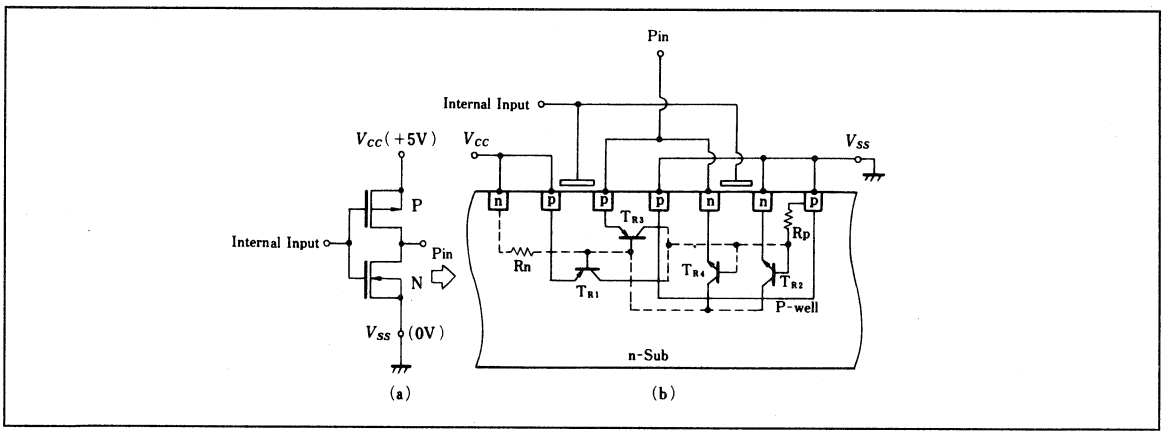


Figure 9-3 Cross Section Structure of CMOS Inverter

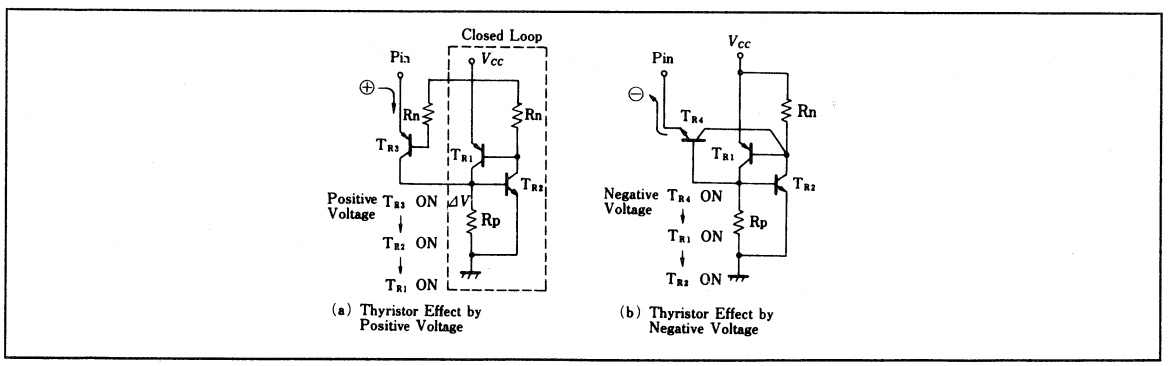


Figure 9-4 Equivalent Circuit of Parasitic Thyristor

9.3 Noise Prevention

Noise in semiconductor memories is roughly classified as input signal noise and power supply noise.

Input Signal Noise: Input signal noise is caused by overshoot and undershoot. If either of them exceeds the recommended DC operating conditions, normal operation is hindered, and a voltage over the absolute maximum rating will break the device. When operating high speed systems, special care is required to prevent input signal noise.

The noise can be prevented by inserting a serial resistance of less than 50 ohms into each input or a terminating resistance into the input line. Actually, however, input signal noise can be simply reduced by a stable power supply line, because the noise is often caused by an unstable reference voltage (ground level).

Power Supply Noise: Power supply noise can be classed as low-frequency and high-frequency as shown in Figure 9-5. To assure a stable memory operation, combined low- and high-frequency noise should be held below 10 percent of the standard level of the peak-to-peak power supply voltage.

Devices like dynamic RAMs, which operate from clock signals, or high speed CMOS static RAMs, through which current flows during the transition of signals, consume high peak current. When a power supply does not have enough capacity for the peak current, the voltage drops. And if the recovery rate of the power supply synchronizes with its time constant, it may start oscillating. To reduce the influence of the peak current, a bypass capacitor of 0.1–0.01 μF should be inserted near the device. The following points must be considered in designing the layout of a board:

1. For bypass capacitors, use titanium, ceramic, or tantalum capacitors which have better high-frequency characteristics.

2. Bypass capacitors must be applied to the power supply pins of memory devices as near as possible, and inductance in the path from the V_{CC} pin to V_{SS} pin through the bypass capacitor must be kept as low as possible.

3. The line connected to the power supply on the board should be as wide as possible.

4. It is preferable for the power supply line to be at right angles to devices selected at the same time, otherwise too much peak current will flow through one power supply line at a time.

9.4 Address Input Waveform of Hi-BiCMOS Memory

Data stored in memory might be destroyed in a case where the address input of a HM6716, HM6719, HM6787, HM6788, or HM6789 series device floats and sticks near threshold voltage (e.g., CPU sets the address bus to off state in Figure 9-7). Consequently, the following three methods are recommended to prevent malfunctions of a Hi-BiCMOS memory device.

A: Insert the latch as shown in Figure 9-7 to keep the address input from floating.
B: Set $\overline{CS}$ high while the address input floats.
C: Insert a pull-up resistor (R) to hold the time constant of the rising edge waveform on the address input pin ($t_r = R \times C$) below 150 ns.

Stable operation can be assured if the above three methods (A, B, C) have been adopted. Should any further problems arise, please contact one of our sales offices.

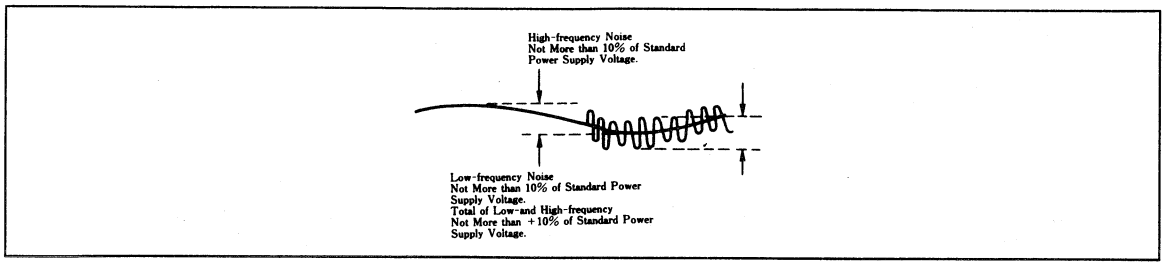


Figure 9-5 Power Supply Noise

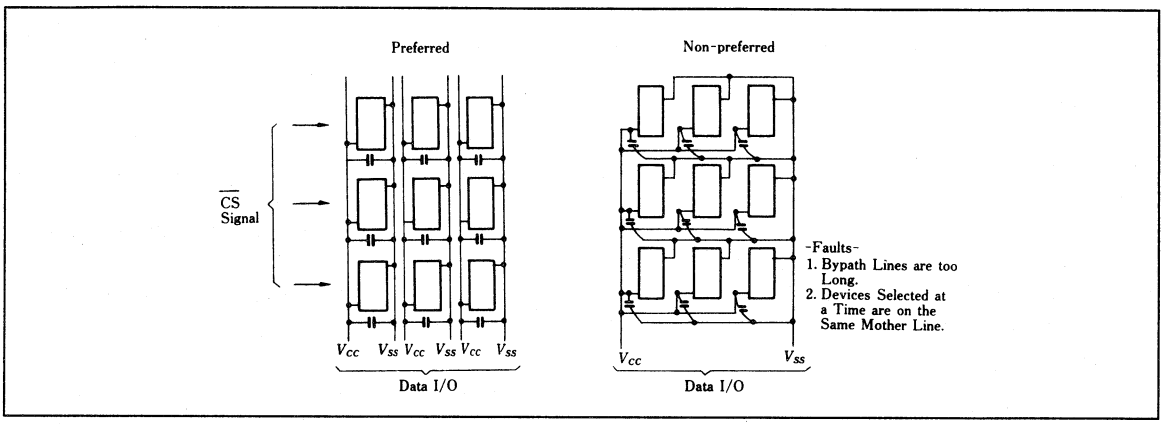


Figure 9-6 Examples of a Power Supply Board Pattern

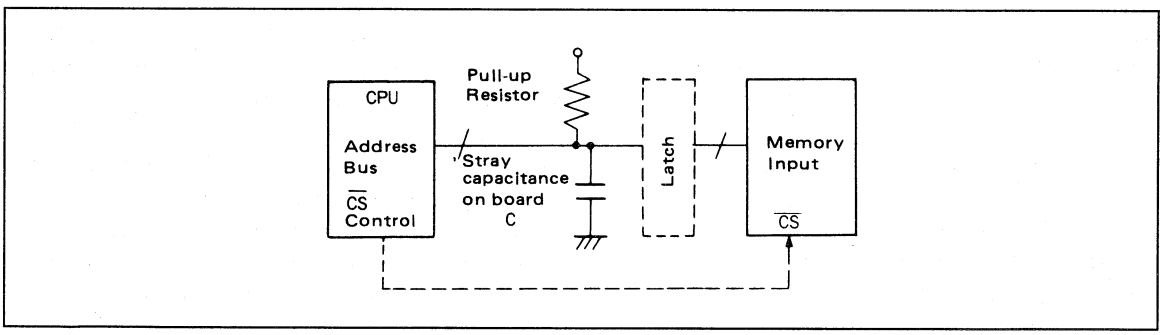


Figure 9-7

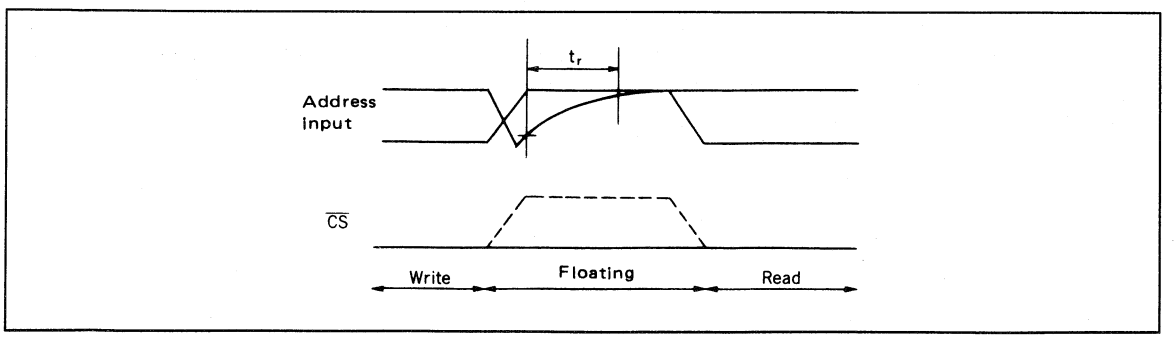


Figure 9-8

DATA SHEETS

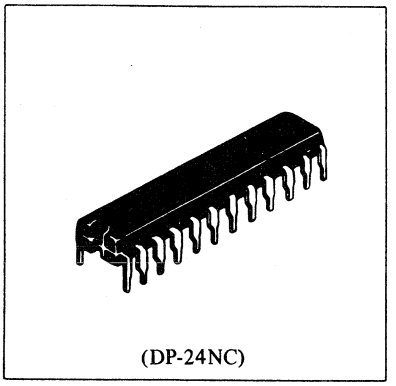
MOS
Static
RAM

HM6716, HM6719 Series

2048-word x 8-bit High Speed Hi-BiCMOS Static RAM (with $\overline{OE}$)
2048-word x 9-bit High Speed Hi-BiCMOS Static RAM

■ Features

- Fast Access Time: 25/30ns (max)
- Low Power Dissipation (DC): 280mW (typ.)
- +5V Single Supply
- Completely Static Memory
- No Clock or Timing Strobe Required
- Fully TTL Compatible Input and Output

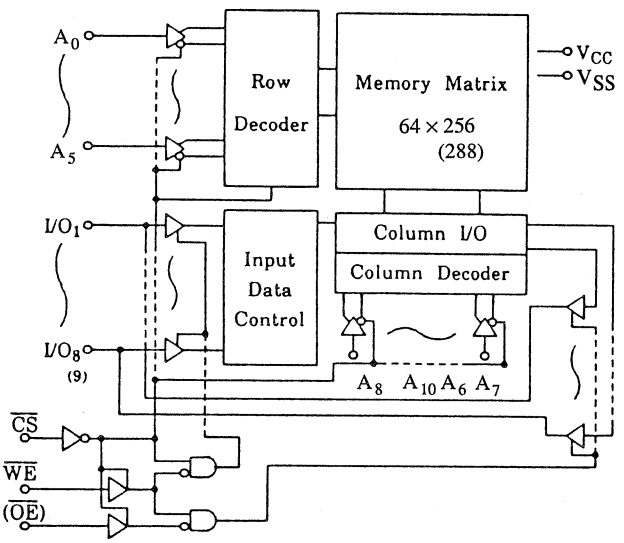


(DP-24NC)

■ Ordering Information

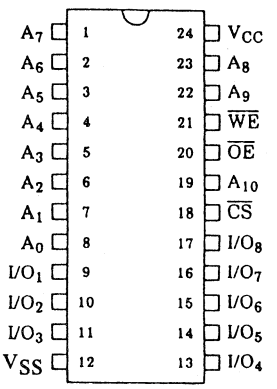
Type No.	Access Time	Package
HM6716P-25	25ns	300 mil 24 Pin Plastic DIP
HM6716P-30	30ns	
HM6719P-25	25ns	
HM6719P-30	30ns	

■ Block Diagram



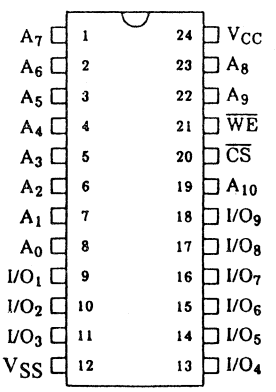
■ Pin Arrangement

● **HM6716**



(Top View)

● **HM6719**



(Top View)

■ Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range (with bias)	T_{stg} (bias)	−10 to +85	°C

■ Truth Table

● HM6716

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	Pin	Ref. Cycle
H	H or L	H or L	Not selected	I_{SB}, I_{SB1}	High Z	–
L	L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (2)
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	–

● HM6719

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (2) (3)
L	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (2)

■ Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}*)	−3.0	–	0.8	V

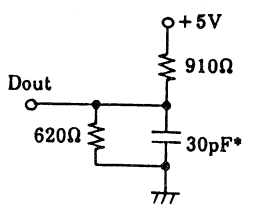
*) Pulse Width: 20ns, DC: −0.5V

■ DC and Operating Characteristics (V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

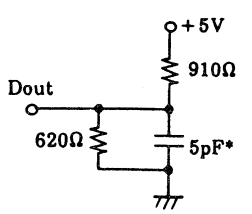
Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{IN}= V_{SS} to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, $V_{I/O}$= V_{SS} to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	–	–	120	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%, $I_{I/O}$=0mA	–	–	130	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	–	–	30	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{CC}−0.2V V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC}−0.2V	–	–	10	mA
Output Low Voltage	V_{OL}	I_{OL}=4mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−1mA	2.4	–	–	V

■ AC Test Conditions

Input pulse levels: V_{SS} to 3.0V
Input and Output reference levels: 1.5V
Input rise and fall time: 4ns
Output Load: See Figure



Output Load A



Output Load B

*including scope and jig

(t_{CHZ}, t_{WHZ}, t_{CLZ}, t_{OW}, t_{OHZ}, t_{OLZ})

■ Capacitance (T_a = 25°C, f = 1.0 MHz)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	–	–	6	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	–	8	pF

Note) This parameter is sampled and not 100% tested.

■ AC Characteristics (V_{CC} 5V ± 10%, T_a = 0 to +70°C, unless otherwise noted.)

● Read Cycle

Item	Symbol	HM6716-25 HM6719-25		HM6716-30 HM6719-30		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	25	–	30	–	ns	–
Address Access Time	t_{AA}	–	25	–	30	ns	–
Chip Select Access Time	t_{ACS}	–	25	–	30	ns	–
Chip Selection to Output in Low Z	t_{CLZ}	0	–	0	–	ns	*2
Output Enable to Output Valid	t_{OE}	0	20	0	20	ns	*1
Output Enable to Output in Low Z	t_{OLZ}	0	–	0	–	ns	*1, *2
Chip Deselection to Output in High Z	t_{CHZ}	0	10	0	12	ns	*2
Chip Disable to Output in High Z	t_{OHZ}	0	10	0	10	ns	*1, *2
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	–
Input Voltage Rise/Fall Time	t_T	–	150	–	150	ns	*3

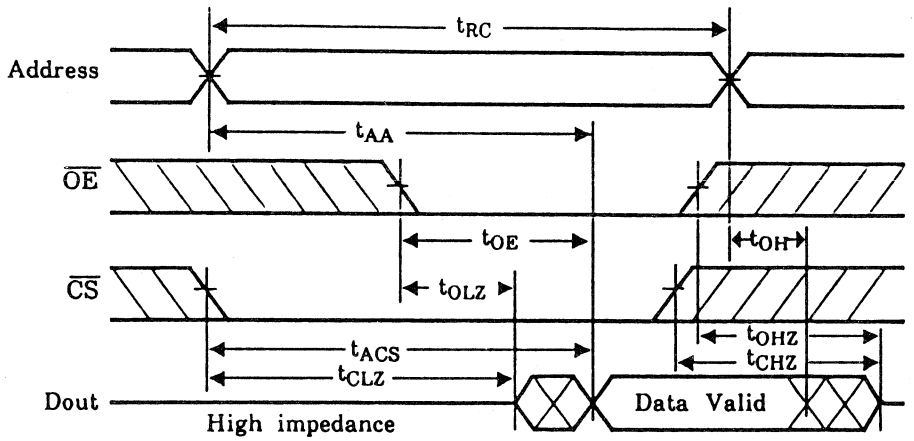
● Write Cycle

Item	Symbol	HM6716-25 HM6719-25		HM6716-30 HM6719-30		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	25	–	30	–	ns	–
Chip Selection to End of Write	t_{CW}	20	–	25	–	ns	–
Address Setup Time	t_{AS}	0	–	0	–	ns	–
Address Valid to End of Write	t_{AW}	20	–	25	–	ns	–
Write Pulse Width	t_{WP}	20	–	25	–	ns	–
Write Recovery Time	t_{WR}	0	–	0	–	ns	–
Output Disable to Output in High Z	t_{OHZ}	0	10	0	10	ns	*1, *2
Write to Output in High Z	t_{WHZ}	0	10	0	12	ns	*2
Data Valid to End of Write	t_{DW}	15	–	15	–	ns	–
Data Hold Time	t_{DH}	5	–	5	–	ns	–
Output Active from End of Write	t_{OW}	0	–	0	–	ns	*2

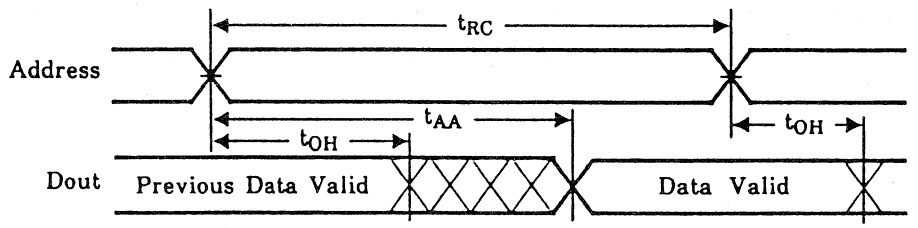
Notes) *1. These parameters are for HM6716.
*2. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
*3. Please contact your nearest Hitachi's Sale Dept. regarding specification.

■ Timing Waveforms

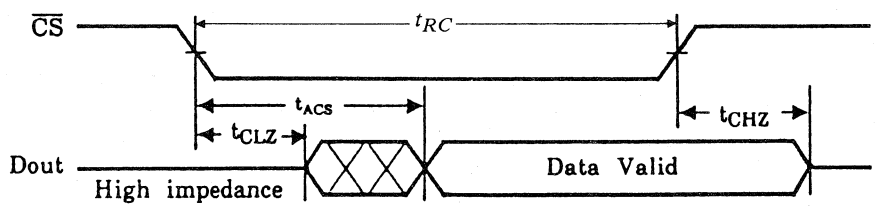
● Read Cycle (1)*1



● Read Cycle (2)*1,*2,*4

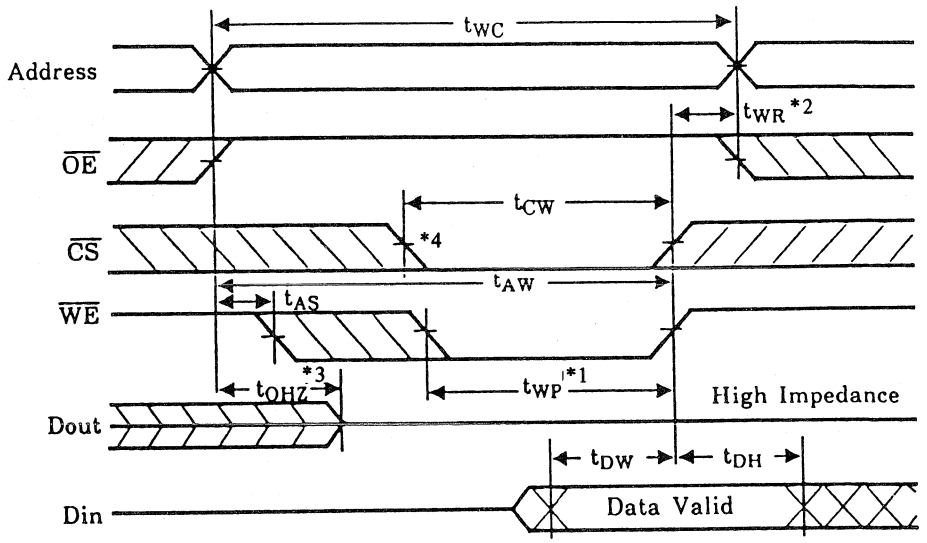


● Read Cycle (3)*1,*3,*4

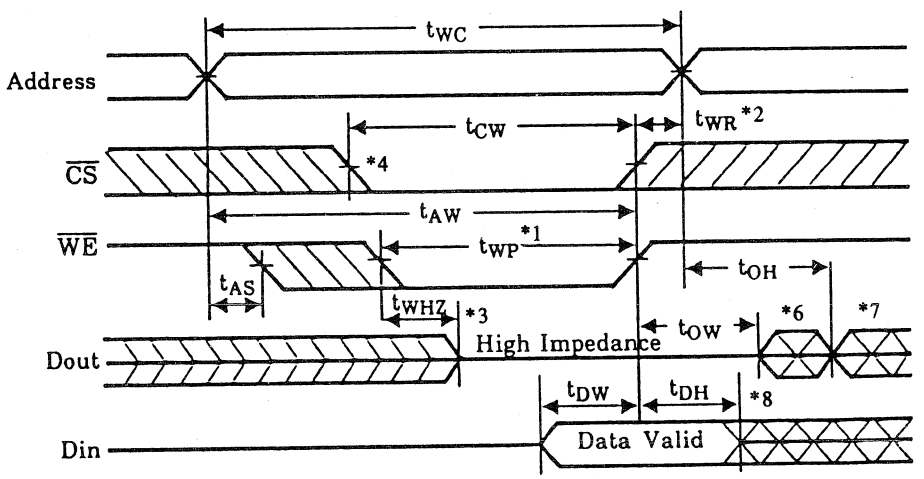


Notes) *1. $\overline{WE}$ is High for Read Cycle.
*2. Device is continuously selected, $\overline{CS}=V_{IL}$.
*3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
*4. $\overline{OE}=V_{IL}$.

- **Write Cycle (1)**



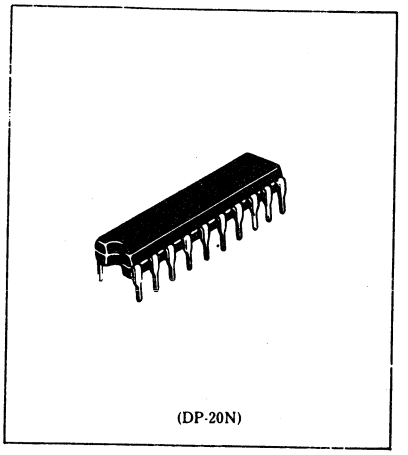
- **Write Cycle (2)** *5



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
*5. $\overline{OE}$ is continuously low. ($\overline{OE}=V_{IL}$).
*6. Dout is the same phase of write data of this write cycle.
*7. Dout is the read data of next address.
*8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

HM6268 Series

4096-word x 4-bit High Speed CMOS Static RAM



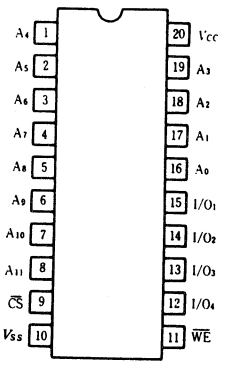
■FEATURES

- Single 5V Supply and High Density 20 Pin Package.
- High Speed: Fast Access Time 25/35/45ns (max.)
- Low Power Standby: 100μW typ, 5μW typ (L-version)
  Active: 250mW typ.
- Completely Static Memory: No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible – All Inputs and Outputs
- Capability of Battery Back Up Operation (L-version)

■ORDERING INFORMATION

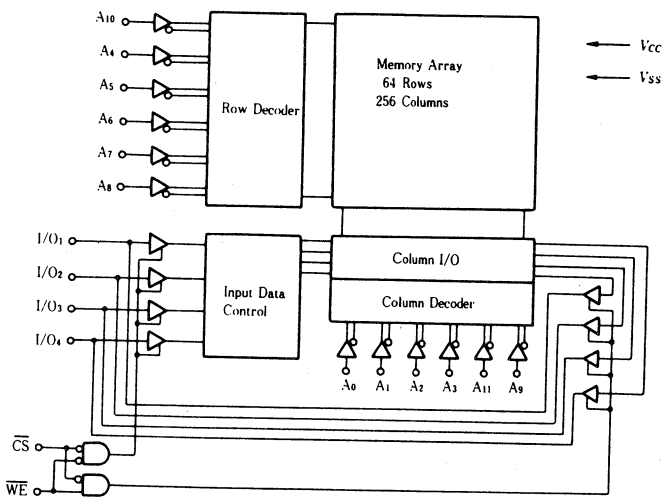
Type No.	Access Time	Package
HM6268P-25 HM6268P-35 HM6268P-45	25ns 35ns 45ns	300mil 20pin Plastic DIP
HM6268LP-25 HM6268LP-35 HM6268LP-45	25ns 35ns 45ns	

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

Note) *1. −3.5V for pulse width≦10ns.

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	Not Selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	Din	Write Cycle

■RECOMMENDED OPERATING CONDITIONS (Ta=0 to +70℃)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	–	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width≦10ns.

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}= 0V, Ta=0 to +70℃)

Parameter	Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC}=5.5V, V_{in}= V_{SS} to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}$= V_{IH}, $V_{I/O}$= V_{SS} to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$= V_{IL}, $I_{I/O}$=0mA, min. cycle	–	50*3	90	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$= V_{IH}, min. cycle	–	15	25	mA
Standby Power Supply Current (1)	I_{SB1}	$\overline{CS}$≧ V_{CC}−0.2V, 0V≦ V_{IN} ≦0.2V or V_{CC} −0.2V≦ V_{IN}	–	0.02	2.0	mA
			–	1*2	50*2	μA
Output Low Voltage	V_{OL}	I_{OL}=8mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH}= −4.0mA	2.4	–	–	V

Notes) *1. Typical limits are at V_{CC}=5.0V, Ta= +25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.
*3. 40mA typ. for 45ns version.

■CAPACITANCE (Ta=25°C, f=1.0MHz)

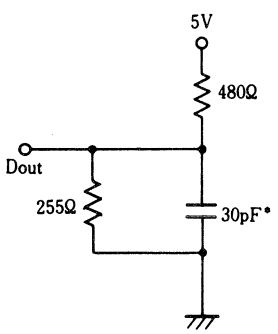
Parameter	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	9	pF

Note: This parameter is sampled and not 100% tested.

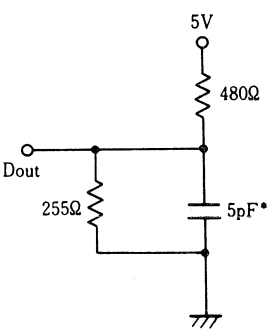
■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70℃, unless otherwise noted.)

- **AC Test Conditions**
  Input pulse levels: V_{SS} to 3.0V
  Input rise and fall times: 5ns
  Input and Output timing reference levels: 1.5V
  Output load: See Figure

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



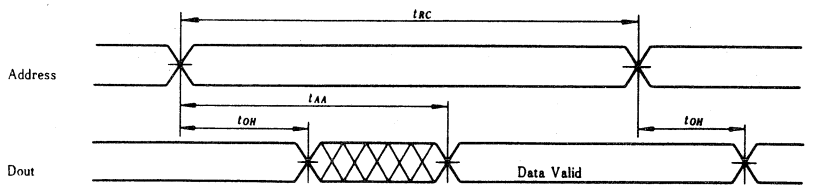
*Including scope and jig.

● READ CYCLE

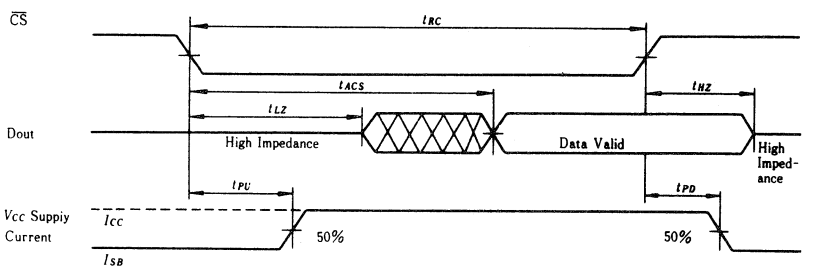
Parameter	Symbol	HM6268-25		HM6268-35		HM6268-45		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	25	—	35	—	45	—	ns
Address Access Time	t_{AA}	—	25	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	—	45	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}*1	10	—	10	—	10	—	ns
Chip Deselection to Output in High Z	t_{HZ}*1	0	15	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	25	—	25	—	30	ns

Note) * 1. Transition is measured ± 200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Read Cycle No. 1(1),(2)



● Timing Waveform of Read Cycle No. 2(1),(3)



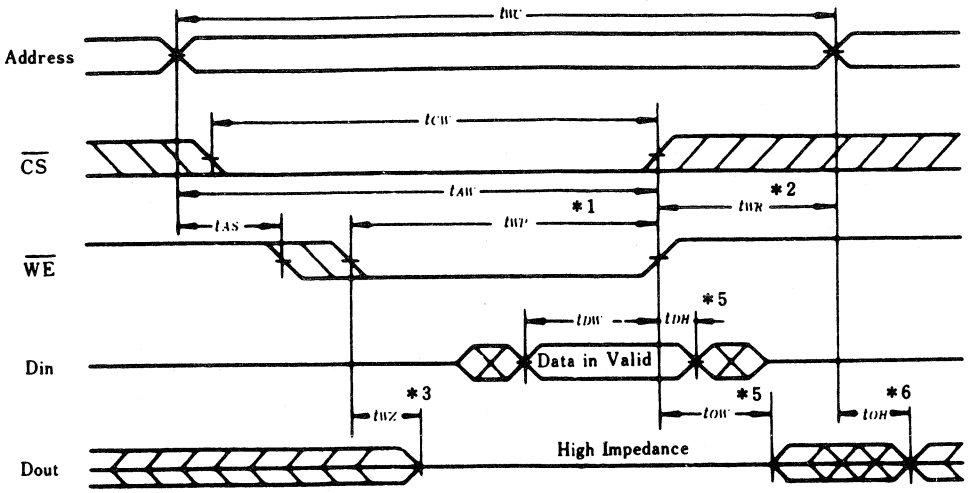
Notes: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

● WRITE CYCLE

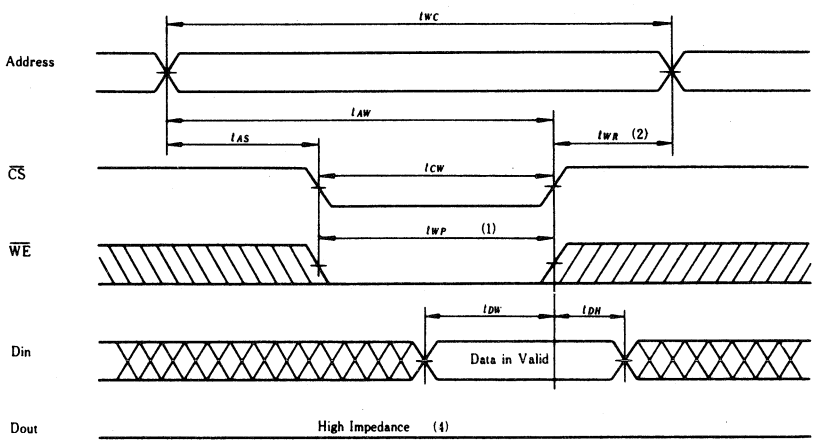
Parameter	Symbol	HM6268-25		HM6268-35		HM6268-45		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	25	—	35	—	45	—	ns
Chip Selection to End of Write	t_{CW}	20	—	30	—	40	—	ns
Address Valid to End of Write	t_{AW}	20	—	30	—	40	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	20	—	30	—	35	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns
Data Valid to End of Write	t_{DW}	12	—	20	—	20	—	ns
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns
Write Enabled to Output in High Z	t_{WZ}*1	0	8	0	10	0	15	ns
Output Active from End of Write	t_{OW}*1	0	—	0	—	0	—	ns

Note) * 1. Transition is measured ± 200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

- Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



- Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)



Notes:
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

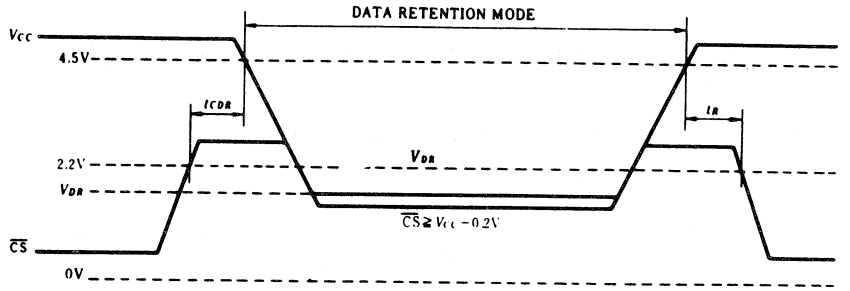
■LOW V_{CC} DATA RETENTION CHARACTERISTICS ($0°C \leqq Ta \leqq 70°C$)

This characteristics guaranteed only for L-version.

Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC}-0.2V$ $V_{in} \geqq V_{CC}-0.2V$ or $0V \leqq V_{in} \leqq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}		—	—	30 *2 20 *3	μA
Chip Deselect to Data Retention Time	t_{CDR}	See retention waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC} *1	—	—	ns

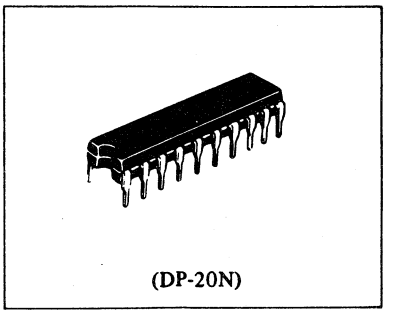
Notes) *1. t_{RC} = Read Cycle Time.
*2. V_{CC} = 3.0V
*3. V_{CC} = 2.0V

●LOW V_{CC} DATA RETENTION WAVEFORM



HM6267 Series

16384-word x 1-bit High Speed CMOS Static RAM



(DP-20N)

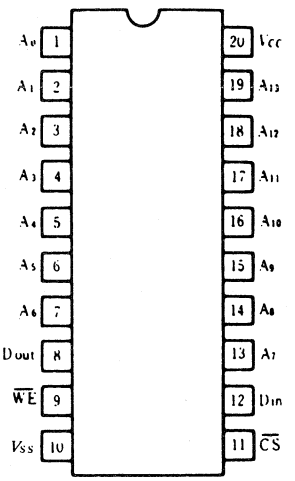
■ FEATURES

- High Speed: Fast Access Time 35/45/55ns (max.)
- Low Power Standby and Low Power Operation
  Standby: 0.1mW (typ.)/5μW (typ.) (L-version),
  Operation: 200mW (typ.)
- Single 5V Supply and High Density 20 Pin Package
- Completely Static Memory ..... No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Input and Output
- Capability of Battery Back Up Operation (L-version)

■ ORDERING INFORMATION

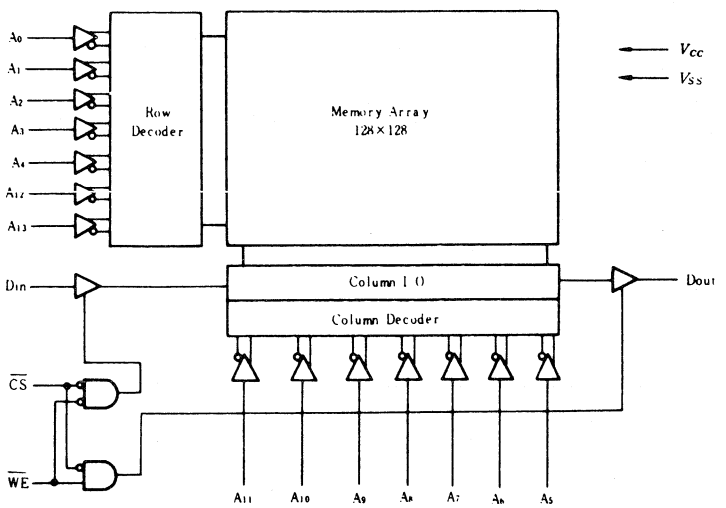
Type No.	Access Time	Package
HM6267P-35	35ns	300 mil 20 pin Plactic DIP
HM6267P-45	45ns	
HM6267P-55	55ns	
HM6267LP-35	35ns	
HM6267LP-45	45ns	
HM6267LP-55	55ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin*1	V_T	-0.5*2 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature Under Bias	T_{bias}	-10 to +85	°C

Notes) *1. With respect ot V_{SS}.
*2. -3.5V for pulse width ≦ 20ns.

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	-0.5*1	–	0.8	V

Note) *1. -3.0V for pulse width ≦ 20ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	HM6267-35			HM6267-45/55			Unit
			min	typ*1	max	min	typ*1	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{IN}=V_{SS} to V_{CC}	–	–	10	–	–	10	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, V_{OUT}=V_{SS} to V_{CC}	–	–	10	–	–	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, I_{OUT}=0mA, min. cycle	–	40	100	–	40	80	mA
Stand by Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, min cycle	–	10	20	–	10	20	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{CC} – 0.2V, 0V ≦ V_{IN} ≦ 0.2V or V_{CC} – 0.2V ≦ V_{IN}	–	0.02	2	–	0.02	2	mA
			–	1*2	50*2	–	1*2	50*2	μA
Output Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	–	–	0.4	V
	V_{OH}	I_{OH} = -4mA	2.4	–	–	2.4	–	–	V

Notes) *1. Typical limts are at V_{CC} = 5V, T_a = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	typ.	max	Unit	Conditions
Input Capacitance	C_{IN}	—	5	pF	V_{IN}=0V
Output Capacitance	C_{OUT}	—	7	pF	V_{OUT}=0V

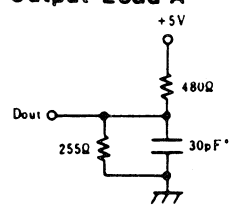
Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_a = 0 to +70°C, unless otherwise noted)

● AC TEST CONDITIONS

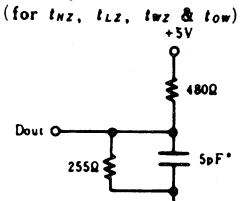
Input pulse levels: V_{SS} to 3.0V
Input rise and fall times: 5ns
Input and Output timing reference levels: 1.5V
Output load: See Figure

Output Load A



* Including scope and jig.

Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

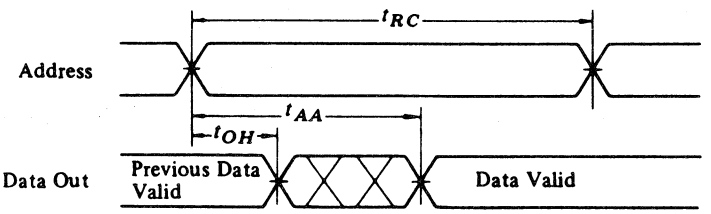


* Including scope and jig.

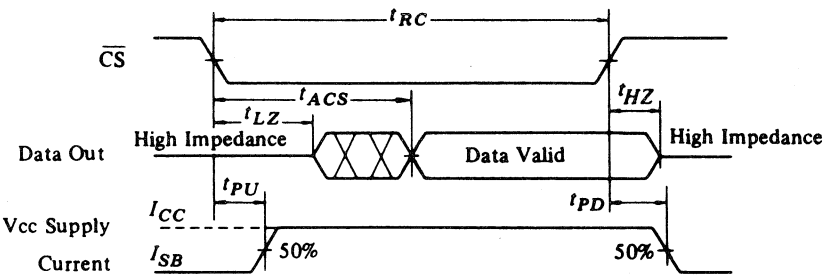
• Read Cycle

Item	Symbol	HM6267-35		HM6267-45		HM6267-55		Unit	Notes
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	35	-	45	–	55	–	ns	1
Address Access Time	t_{AA}	–	35	–	45	-	55	ns	
Chip Select Access Time	t_{ACS}	–	35	–	45	–	55	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	5	–	ns	2,3,7
Chip Deselectio to Output in High Z	t_{HZ}	0	30	0	30	0	30	ns	2,3,7
Chip Selectio to Power Up Time	t_{PU}	0	–	0	–	0	–	ns	
Chip Deselection to Power Down Time	t_{PD}	–	20	–	30	–	30	ns	

• TIMING WAVEFORM OF READ CYCLE NO. 1 [4) 5)]



• TIMING WAVEFORM OF READ CYCLE NO. 2 [4) 6)]

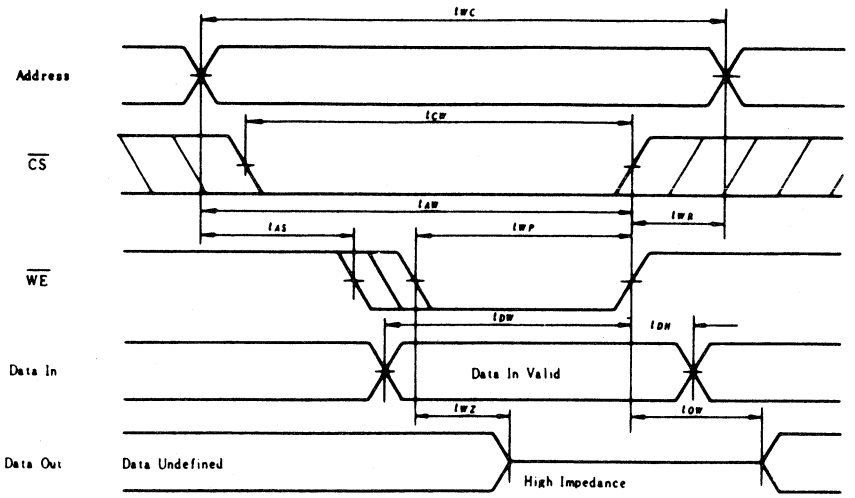


Notes) 1. All Read Cylce timing are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is High for READ cycle.
5. Device is continuously selected, $\overline{CS}$ = V_{IL}.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

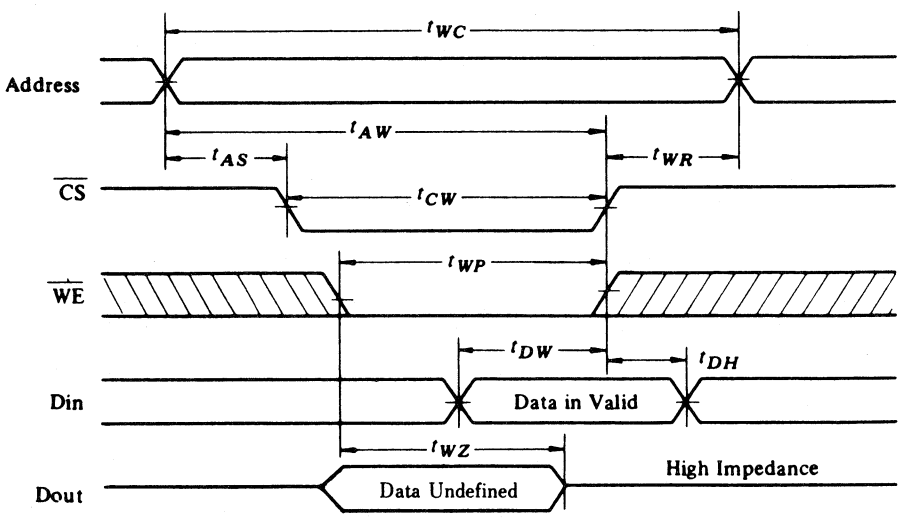
• Write Cycle

Item	Symbol	HM6267-35		HM6267-45		HM6267-55		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	35	–	45	–	55	–	ns	2
Chip Selection to End of Write	t_{CW}	30	–	40	–	50	–	ns	
Address Valid to End of Write	t_{AW}	30	–	40	–	50	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns	
Write Pulse Width	t_{WP}	20	–	25	–	35	–	ns	
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns	
Data Valid to End of Write	t_{DW}	20	–	25	–	25	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	0	–	ns	
Write Enabled to Output in High Z	t_{WZ}	0	20	0	25	0	25	ns	3,4
Output Active from End of Write	t_{OW}	0	–	0	–	0	–	ns	3,4

● **TIMING WAVEFORM OF WRITE CYCLE NO. 1** ($\overline{WE}$ Controlled)



● **TIMING WAVEFORM OF WRITE CYCLE NO. 2** ($\overline{CS}$ Controlled)



Notes) 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
2. All Write Cycle timings are referenced from the last valid address to the first transitions address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

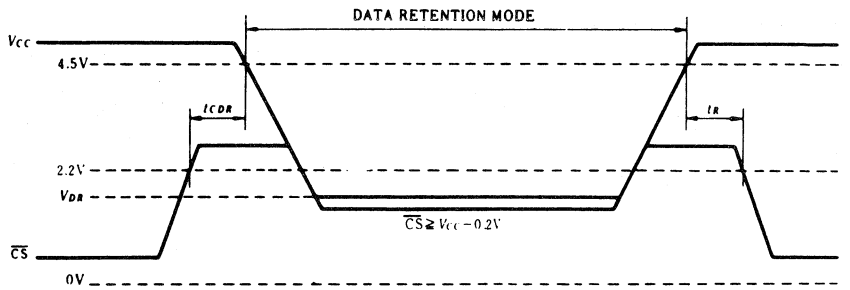
■LOW V_{CC} DATA RETENTION CHARACTERISTICS ($0°C \leqq Ta \leqq 70°C$)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC}-0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}	$V_{in} \geqq V_{CC}-0.2V$ or $0V \leqq V_{in} \leqq 0.2V$	—	—	30*2 20*3	μA
Chip Deselect to Data Retention Time	t_{CDR}	see retention waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC} *1	—	—	ns

Notes) *1. t_{RC} = Read Cycle Time.
*2. V_{CC} = 3.0V
*3. V_{CC} = 2.0V

●LOW V_{CC} DATA RETENTION WAVEFORM



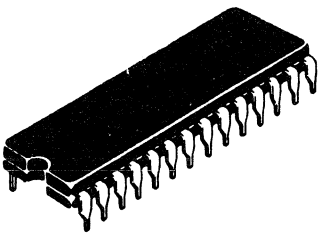
HM6264A Series

8192-word x 8-bit High Speed CMOS Static RAM

■ FEATURES

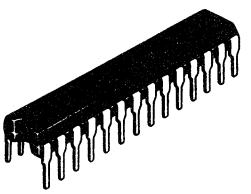
- Low Power Standby — Standby: 0.1mW (typ.) / 10μW (typ.) L-/LL-version
- Low Power Operation — Operating: 15mW/MHz (typ.)
- Fast access Time — 100ns/120ns/150ns (max.)
- Single +5V Supply
- Completely Static Memory. . . . . No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Capability of Battery Back Up Operation (L-/LL-version)

HA6264AP Series



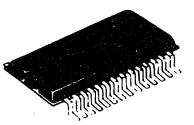
(DP-28)

HM6264ASP Series



(DP-28N)

HM6264AFP Series



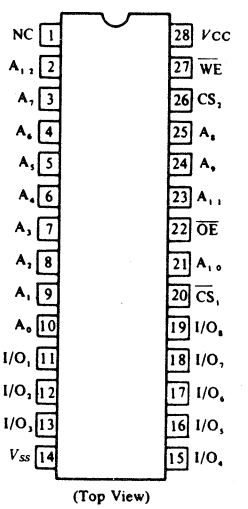
(FP-28D/DA)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6264AP-10	100ns	600 mil 28 pin Plastic DIP
HM6264AP-12	120ns	
HM6264AP-15	150ns	
HM6264ALP-10	100ns	
HM6264ALP-12	120ns	
HM6264ALP-15	150ns	
HM6264ALP-10L	100ns	
HM6264ALP-12L	120ns	
HM6264ALP-15L	150ns	
HM6264ASP-10	100ns	300 mil 28 pin Plastic DIP
HM6264ASP-12	120ns	
HM6264ASP-15	150ns	
HM6264ALSP-10	100ns	
HM6264ALSP-12	120ns	
HM6264ALSP-15	150ns	
HM6264ALSP-10L	100ns	
HM6264ALSP-12L	120ns	
HM6264ALSP-15L	150ns	
HM6264AFP-10	100ns	28 pin Plastic SOP (Note)
HM6264AFP-12	120ns	
HM6264AFP-15	150ns	
HM6264ALFP-10	100ns	
HM6264ALFP-12	120ns	
HM6264ALFP-15	150ns	
HM6264ALFP-10L	100ns	
HM6264ALFP-12L	120ns	
HM6264ALFP-15L	150ns	

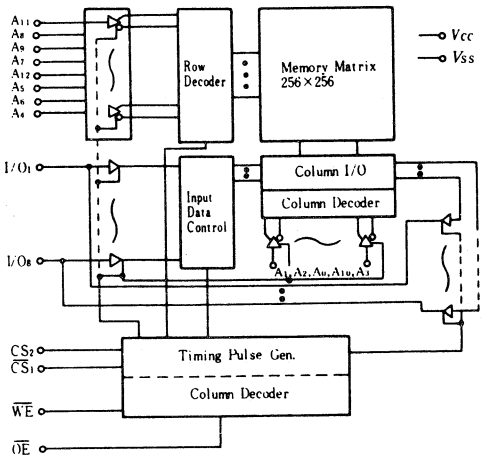
Note) T is added to the end of the type no. for a SOP of 3.00 mm (max.) thickness.

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage*1	V_T	−0.5*2 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

Notes) *1. With respect to V_{SS}.
*2. −3.0V for pulse width ≦ 50ns

■ TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB},I_{SB1}	
X	X	L	X		High Z	I_{SB},I_{SB1}	
H	L	H	H	Output Disabled	High Z	I_{CC}	
H	L	H	L	Read	Dout	I_{CC}	Read Cycle
L	L	H	H	Write	Din	I_{CC}	Write Cycle (1)
L	L	H	L		Din	I_{CC}	Write Cycle (2)

X: H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	--	6.0	V
	V_{IL}	−0.3*1	--	0.8	V

Note) *1. −3.0V for pulse width ≦ 50ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current	$\|I_{LI}\|$	$V_{in}=V_{SS}$ to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS1}=V_{IH}$ or CS2=V_{IL} or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, $V_{I/O}=V_{SS}$ to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CCDC}	$\overline{CS1}=V_{IL}$, CS2=V_{IH}, $I_{I/O}$=0mA	–	7	15	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $\overline{CS1}=V_{IL}$, CS2=V_{IH} $I_{I/O}$=0mA	–	30	45*5	mA
				30	55*6	
	I_{CC2}	Cycle time = 1μs, duty = 100%, $I_{I/O}$ = 0mA, $\overline{CS1} \leqq 0.2V$, CS2 $\geqq V_{CC}-0.2V$ $V_{IH} \geqq V_{CC}-0.2V$, $V_{IL} \leqq 0.2V$	–	3	5	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}=V_{IH}$ or CS2=V_{IL}	–	1	3	mA
	I_{SB1}*2	$\overline{CS1} \geqq V_{CC}-0.2V$, CS2 $\geqq V_{CC}-0.2V$ or $0V \leqq OS2 \leqq 0.2V$, $0V \leqq V_{in}$	–	0.02	2	mA
			–	2*3	100*3	μA
			–	2*4	50*4	
Output Voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	–	–	V

Notes) *1. Typical limits are at V_{CC}=5.0V, T_a=25°C and specified loading.
*2. V_{IL} min=−0.3V
*3. This characteristics is guaranteed only for L-version.
*4. This characteristics is guaranteed only for LL-version.
*5. For 120ns/150ns version.
*6. For 100ns version.

■ CAPACITANCE (f = 1MHz, T_a = 25°C)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	7	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V±10%, Ta = 0 to +70°C)

• AC TEST CONDITIONS

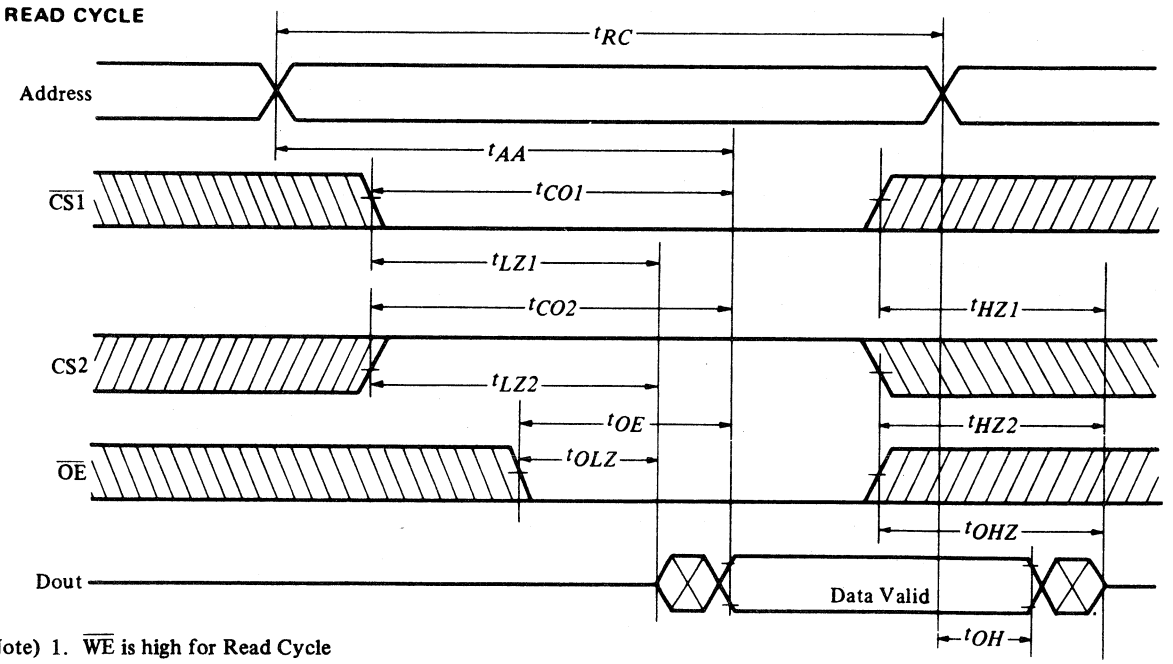
Input Pulse Levels: 0.8V/2.4V
Input Rise and Fall Time: 10ns
Input Timing Reference Level: 1.5V
Output Timing Reference Level: HM6264A-10 1.5V
HM6264A-12/15 0.8V/2.0V
Output Load: 1TTL Gate and C_L (100pF) (including scope and jig)

• READ CYCLE

Item		Symbol	HM6264A-10		HM6264A-12		HM6264A-15		Unit
			min	max	min	max	min	max	
Read Cycle Time		t_{RC}	100	–	120	–	150	–	ns
Address Access Time		t_{AA}	–	100	–	120	–	150	ns
Chip Selection to Output	$\overline{CS1}$	t_{CO1}	–	100	–	120	–	150	ns
	CS2	t_{CO2}	–	100	–	120	–	150	ns
Output Enable to Output Valid		t_{OE}	–	50	–	60	–	70	ns
Chip Selection to Output in Low Z	$\overline{CS1}$	t_{LZ1}	10	–	10	–	15	–	ns
	CS2	t_{LZ2}	10	–	10	–	15	–	ns
Output Enable to Output in Low Z		t_{OLZ}	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	$\overline{CS1}$	t_{HZ1}	0	35	0	40	0	50	ns
	CS2	t_{HZ2}	0	35	0	40	0	50	ns
Output Disable to Output in High Z		t_{OHZ}	0	35	0	40	0	50	ns
Output Hold from Address Change		t_{OH}	10	–	10	–	10	–	ns

Notes) 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from d device to device.

• READ CYCLE

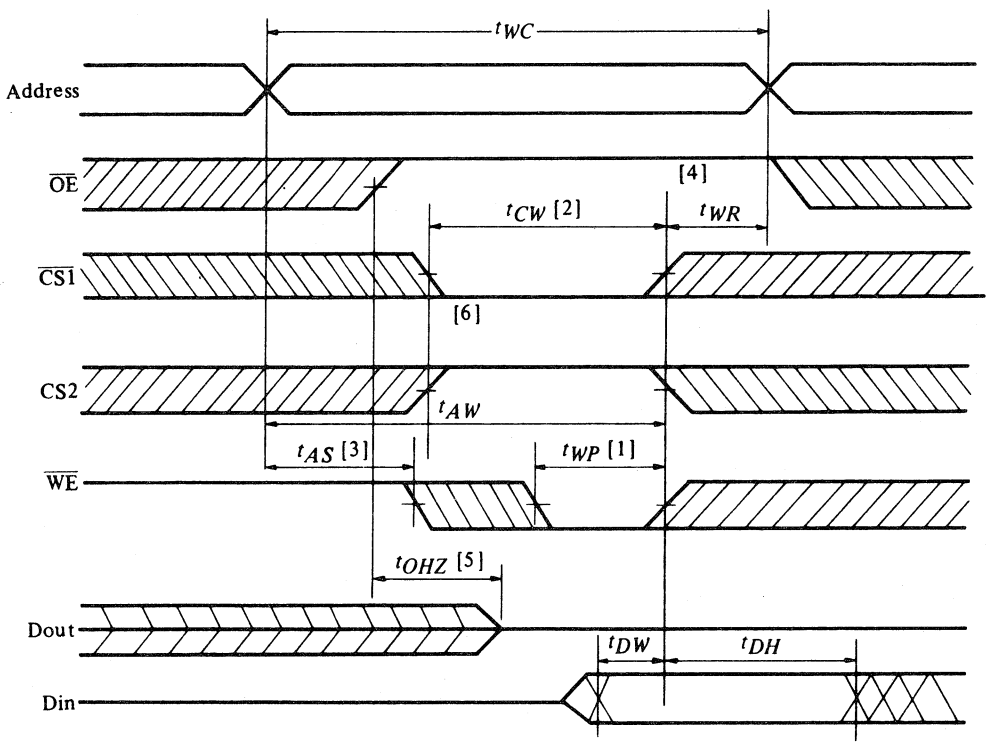


Note) 1. $\overline{WE}$ is high for Read Cycle

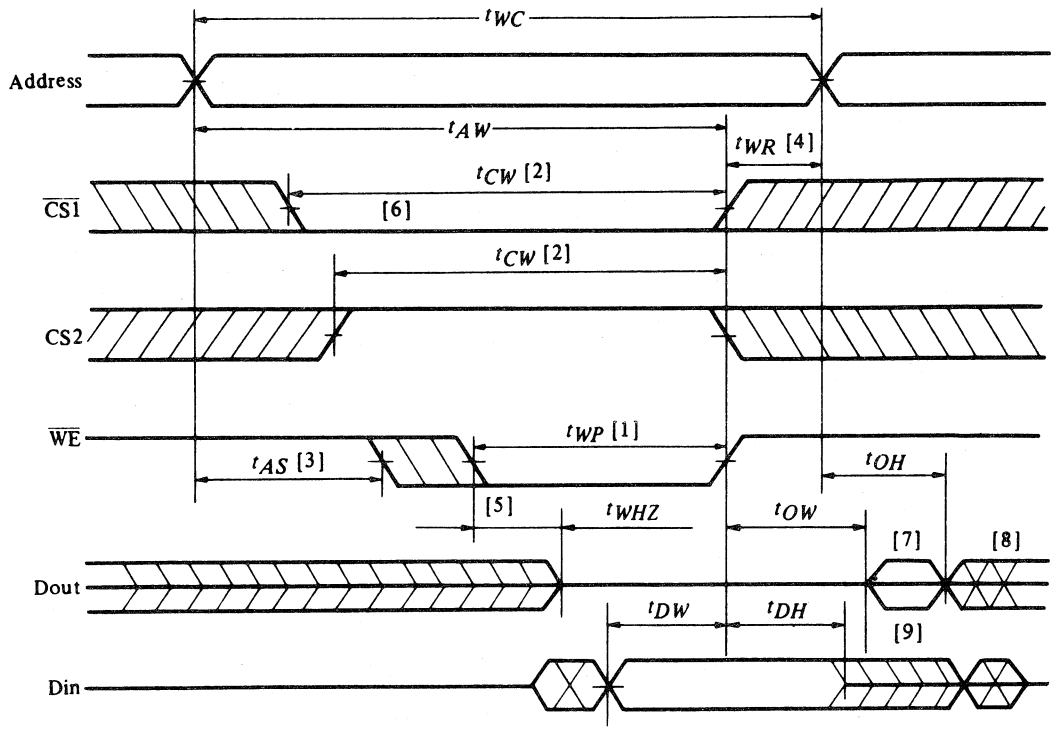
• **WRITE CYCLE**

Item	Symbol	HM6264A-10		HM6264A-12		HM6264A-15		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	100	–	120	–	150	–	ns
Chip Selection to End of Write	t_{CW}	80	–	85	–	100	–	ns
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns
Address Valid to End of Write	t_{AW}	80	–	85	–	100	–	ns
Write Pulse Width	t_{WP}	60	–	70	–	90	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	–	40	–	50	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	ns
Output Enable to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	ns

• **WRITE CYCLE (1) ($\overline{OE}$ clock)**



• WRITE CYCLE (2) (OE Low Fix)



NOTES: 1) A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.

2) t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.

3) t_{AS} is measured from the address valid to the beginning of write.

4) t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.

5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

6) If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.

7) Dout is the same phase of the latest written data in this write cycle.

8) Dout is the read data of next address.

9) If $\overline{CS1}$ is low and $\overline{CS2}$ is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

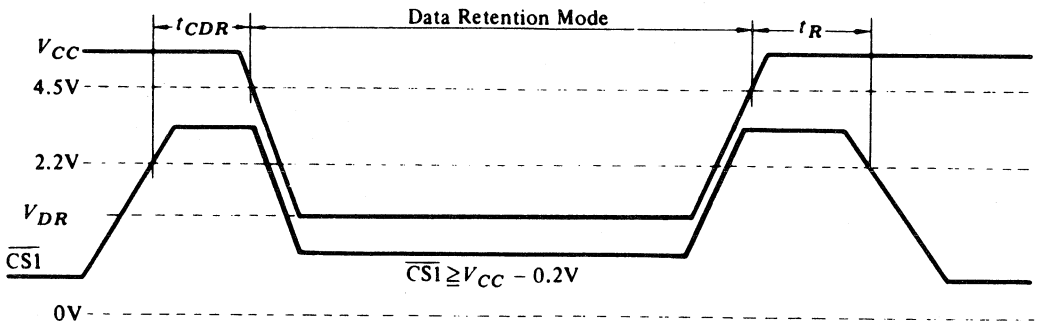
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

This characteristics is guaranteed only for L/LL-version.

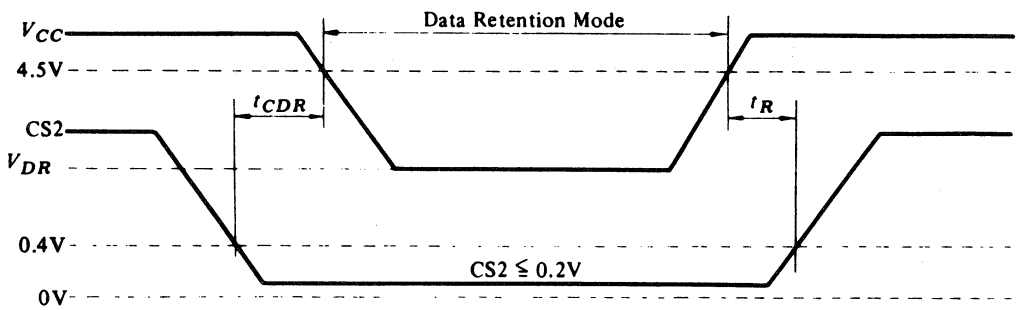
Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS1} \geqq V_{CC}-0.2V$, $CS2 \geqq V_{CC}-0.2V$ or $CS2 \leqq 0.2V$	2.0	–	–	V
Data RetentionCurrent	I_{CCDR}	V_{CC} = 3.0V, $\overline{CS1} \geqq V_{CC}-0.2V$, $CS2 \geqq V_{CC}-0.2V$ or $0V \leqq CS2 \leqq 0.2V, 0V \leqq V_{in}$	–	1*1	50*1	μA
			–	1*2	25*2	
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}*3	–	–	ns

Notes) *1. V_{IL} min = −0.3V, 20μA max at T_a=0 to 40°C, This characteristics is guaranteed only for L-version.
*2. V_{IL} min = −0.3V, 10μA max at T_a = 0 to 40°C, This characteristics is guarnteed only for LL-version.
*3. t_{RC} = Read Cycle Time

• LOW Vcc DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)



• LOW Vcc DATA RETENTION WAVEFORM (2) (CS2 Controlled)



Note) In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and Din buffer. If CS2 controls data retention mode, Vin for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either $CS2 \geqq V_{CC}-0.2V$ or $CS2 \leqq 0.2V$. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

HM6289 Series

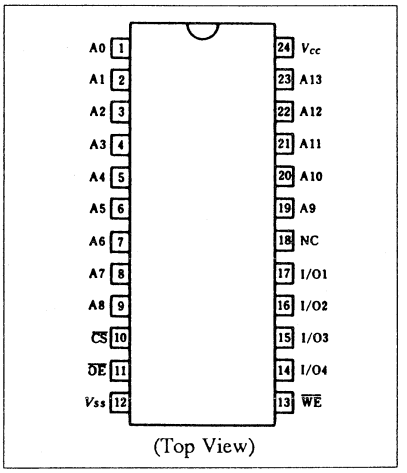
16384-Word × 4-Bit High Speed CMOS Static RAM (with $\overline{OE}$)

The Hitachi HM6289 is a high speed 64k static RAM organized as 16-kword x 4-bit. It realizes high speed access time (25/35/45 ns) and low power consumption, employing CMOS process technology.

It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM6289, packaged in a 300-mil SOJ, is available for high density mounting. Low power version retains the data with battery back up.

Pin Arrangement



(Top View)

Features

- High speed
  Access time:
  t_{AA}: 25/35 ns (max)
  t_{OE}: 12/15 ns (max)
- High density 24-pin SOJ package
- Low power
  Active mode: 300 mW (typ)
  Standby mode: 100 µW (typ)
- Single 5 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible: All inputs and outputs

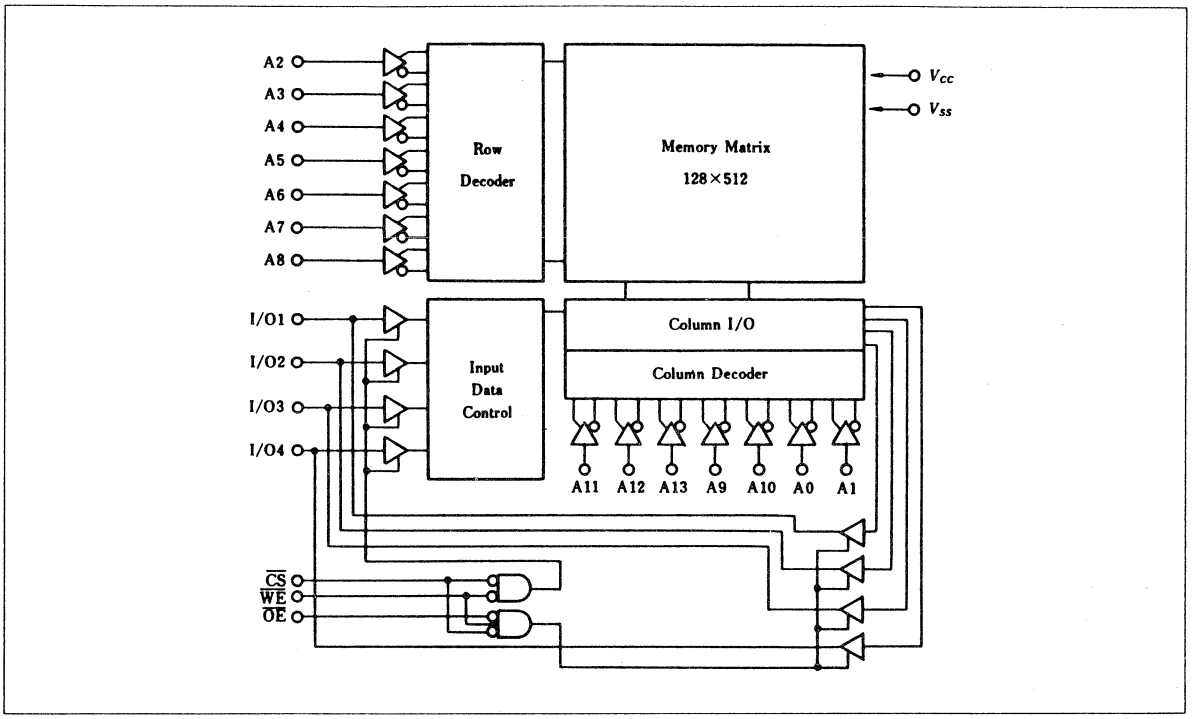
Ordering Information

Type No.	Access Time	Package
HM6289JP-25	25 ns	300-mil
HM6289JP-35	35 ns	24-pin
HM6289LJP-25	25 ns	SOJ
HM6289LJP-35	35 ns	(CP-24D)

Pin Description

Pin Name	Function
A0–A13	Address
I/O1–I/O4	Input/output
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Vcc Current	I/O pin	Ref. Cycle
H	×	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	Icc	Dout	Read cycle (1)–(3)
L	H	L	Write	Icc	Din	Write cycle (1)–(2)
L	L	L	Write	Icc	Din	Write cycle (3)–(6)

Note: ×; H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{in}	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range	T_{stg}	−55 to +125	°C
Storage temperature range under bias	T_{bias}	−10 to +85	°C

Note: *1. Vin min = −2.0 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: *1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min	Typ*1	Max	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	µA	V_{CC} = Max Vin = 0V to Vcc
Output leakage current	$\|I_{LO}\|$	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = 0 V to Vcc
Operating Vcc current	I_{CC}	—	60	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, Min. cycle
Standby Vcc current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}, Min. cycle
Standby Vcc current (1)	I_{SB1}*2	—	0.02	2.0	mA	$\overline{CS}$ ≥ Vcc – 0.2 V
	I_{SB1}*3	—	0.02	0.1	mA	0V ≤ Vin ≤ 0.2 V or Vcc – 0.2 V ≤ Vin
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4.0 mA

Notes: *1. Typical limits are at Vcc = 5.0 V, Ta = +25°C and specified loading.
*2. P-version
*3. LP-version

Capacitance (Ta = 25°C, f = 1MHz)

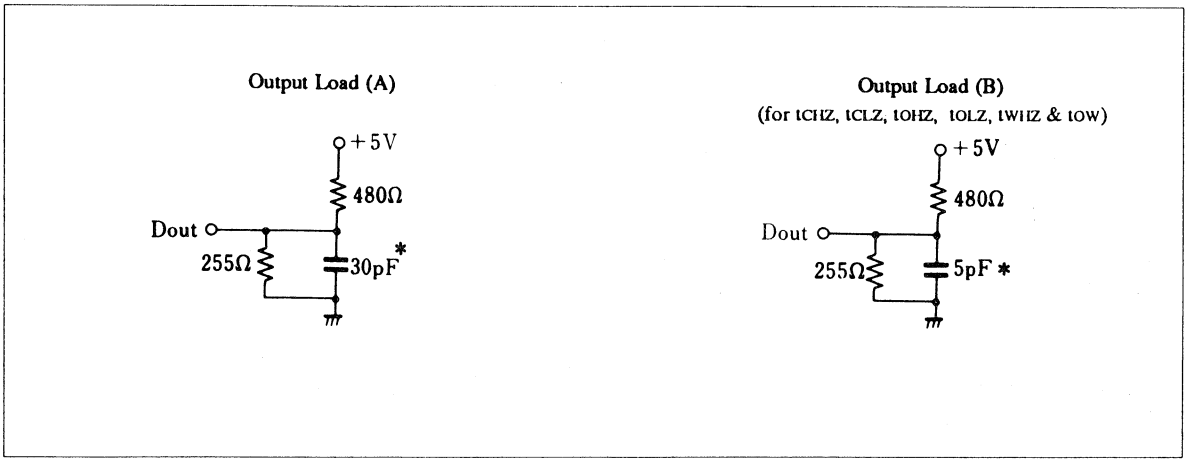
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	8	pF	V I/O = 0 V

Note: This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

Input pulse levels:	Vss to 3.0 V
Input rise and fall times:	5 ns
Input and output timing reference levels:	1.5 V
Output load:	See figures



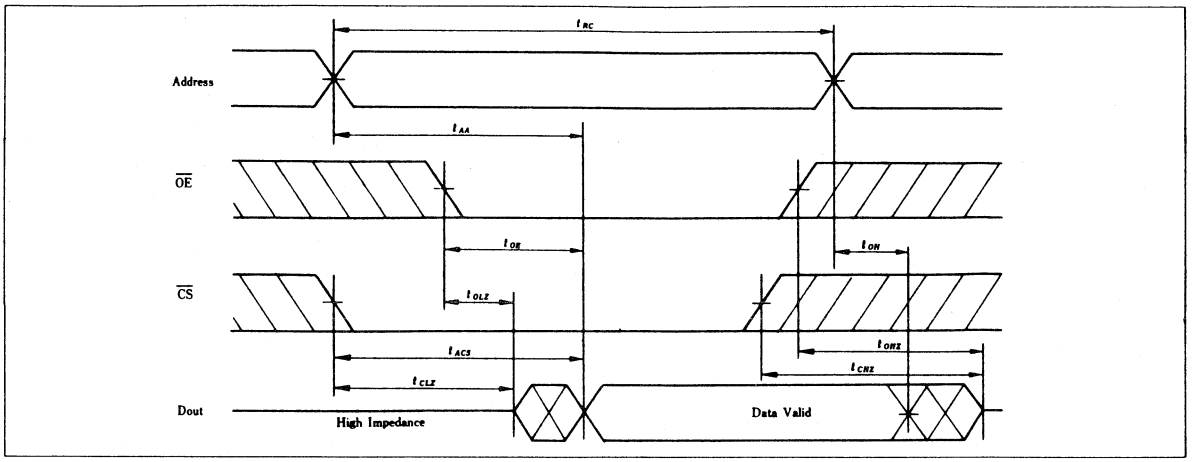
Note: * Including scope & jig.

Read Cycle

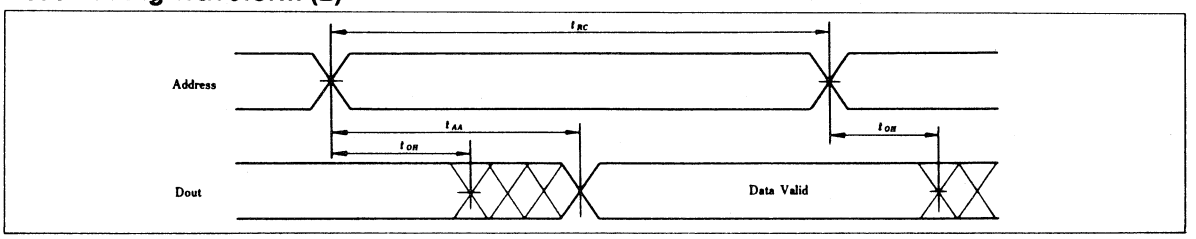
Item	Symbol	HM6289-25		HM6289-35		Unit
		Min	Max	Min	Max	
Read cycle time	t_{RC}	25	—	35	—	ns
Address access time	t_{AA}	—	25	—	35	ns
Chip select access time	t_{ACS}	—	25	—	35	ns
Chip selection to output in low-Z	t_{CLZ}*1	5	—	5	—	ns
Output enable to output valid	t_{OE}	—	12	—	15	ns
Output enable to output in low-Z	t_{OLZ}*1	0	—	0	—	ns
Chip deselection to output in high-Z	t_{CHZ}*1	0	12	0	20	ns
Chis disable to output in high-Z	t_{OHZ}*1	0	10	0	10	ns
Output hold from address change	t_{OH}	3	—	5	—	ns
Chip selection to power up time	t_{PU}	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	25	—	30	ns

Note: *1. Output transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

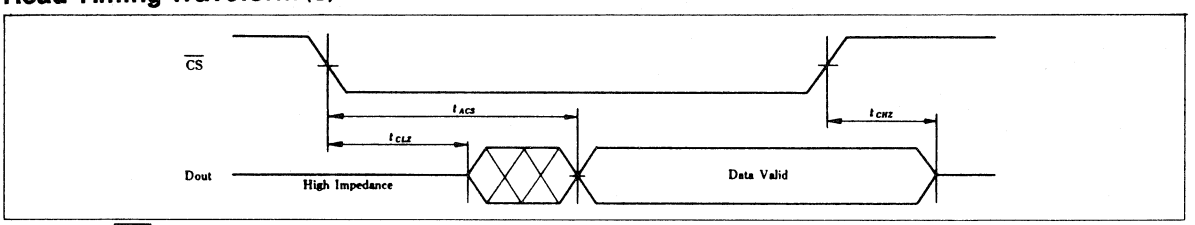
Read Timing Waveform (1) *1



Read Timing Waveform (2) *1,*2,*4



Read Timing Waveform (3) *1,*3,*4



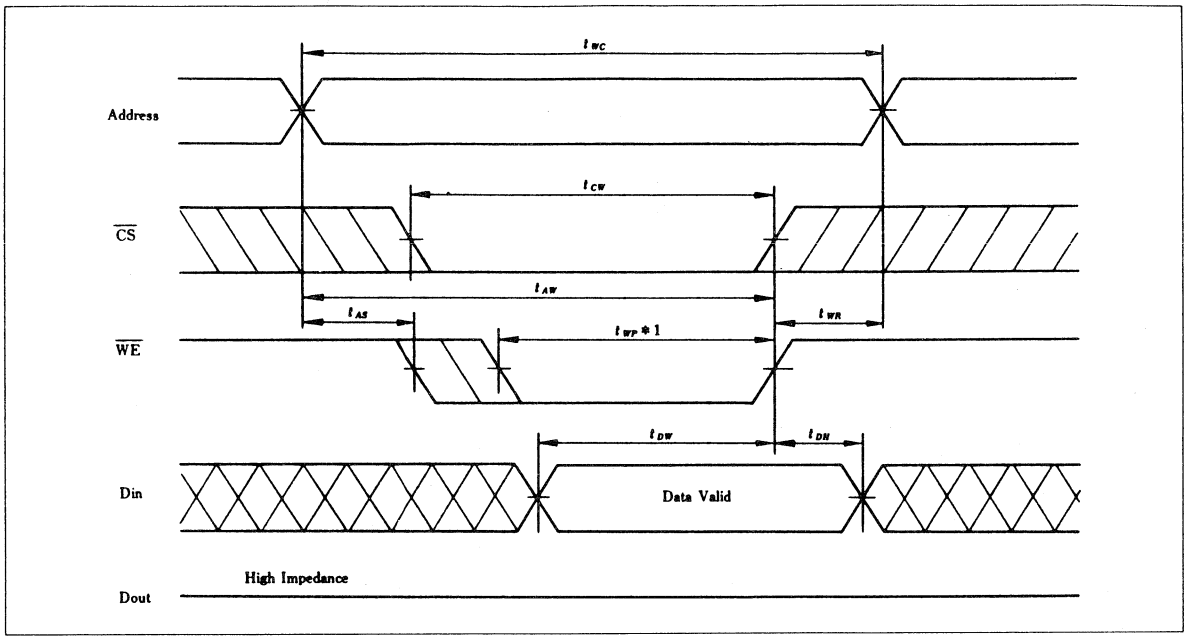
Notes: *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.
*4. $\overline{OE}$ = V_{IL}.

Write Cycle

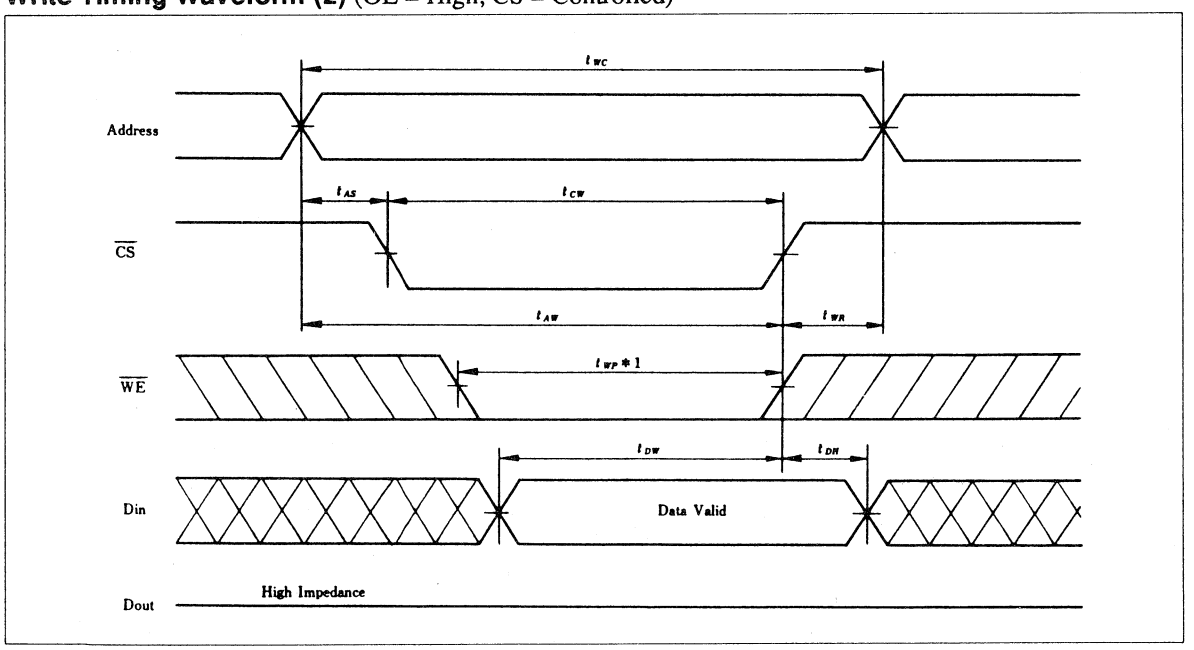
Item	Symbol	HM6289-25		HM6289-35		Unit
		Min	Max	Min	Max	
Write cycle time	t_{WC}	25	—	35	—	ns
Chip selection to end of write	t_{CW}	20	—	30	—	ns
Address valid to end of write	t_{AW}	20	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	30	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Output disable to output in high-Z*1	t_{OHZ}	0	10	0	10	ns
Write to output in high-Z*1	t_{WHZ}	0	8	0	10	ns
Data to write time overlap	t_{DW}	12	—	20	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Output active from end of write*1	t_{OW}	5	—	5	—	ns

Note: *1. Output transition is measured ± 200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

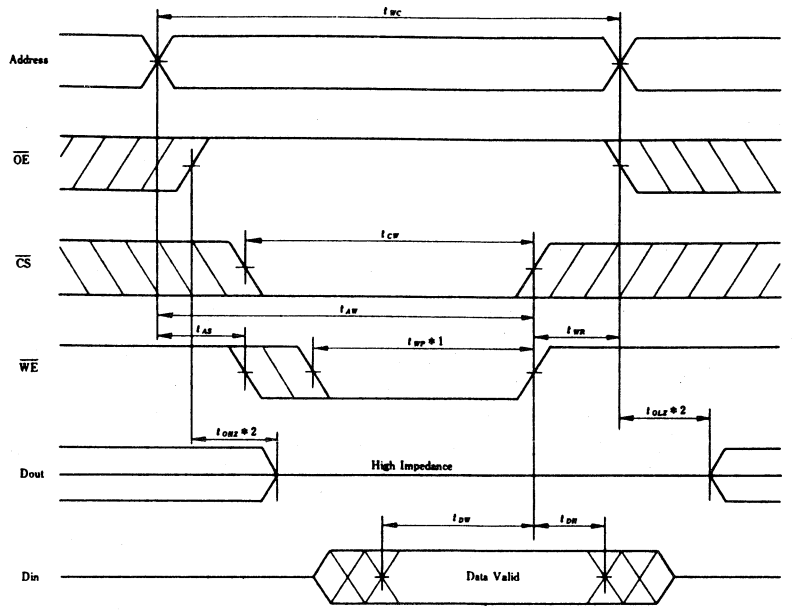
Write Timing Waveform (1) ($\overline{OE}$ = High, $\overline{WE}$ = Controlled)



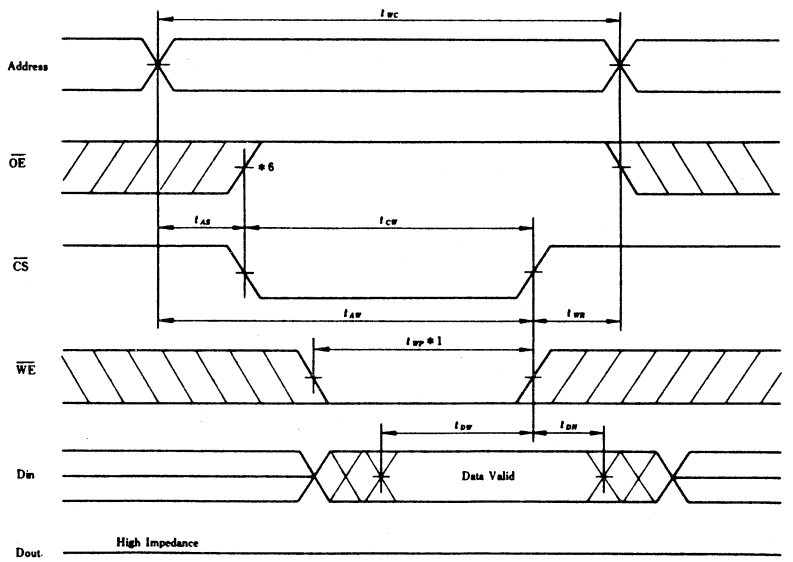
Write Timing Waveform (2) ($\overline{OE}$ = High, $\overline{CS}$ = Controlled)



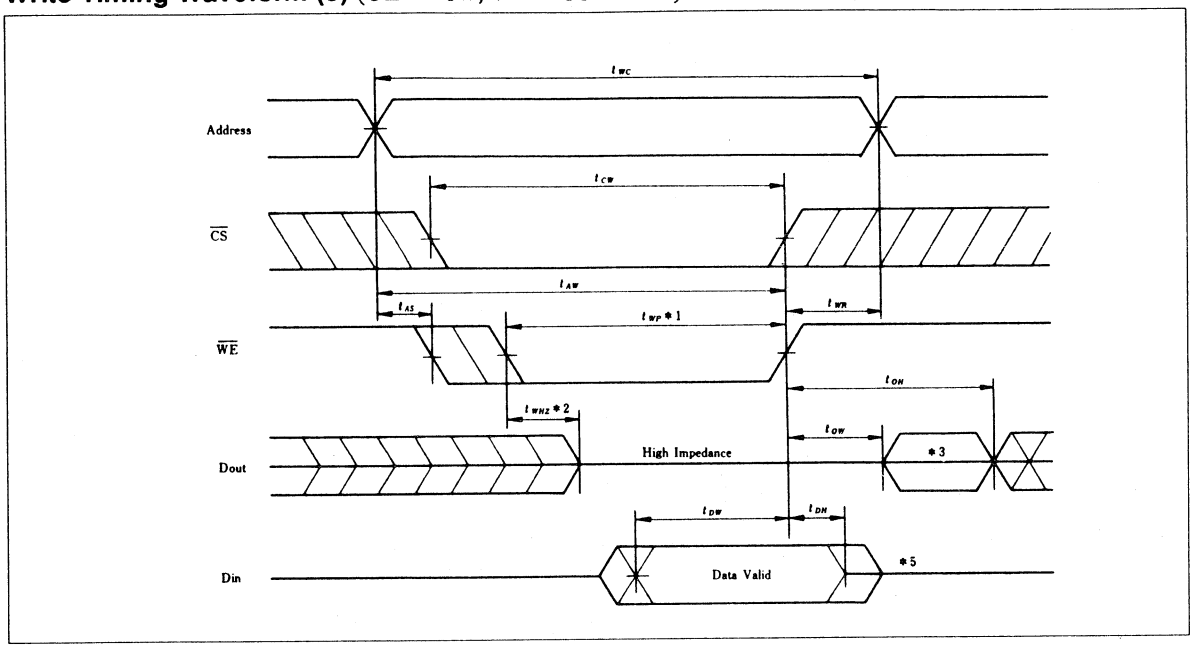
Write Timing Waveform (3) ($\overline{OE}$ = Clocked, $\overline{WE}$ = Controlled)



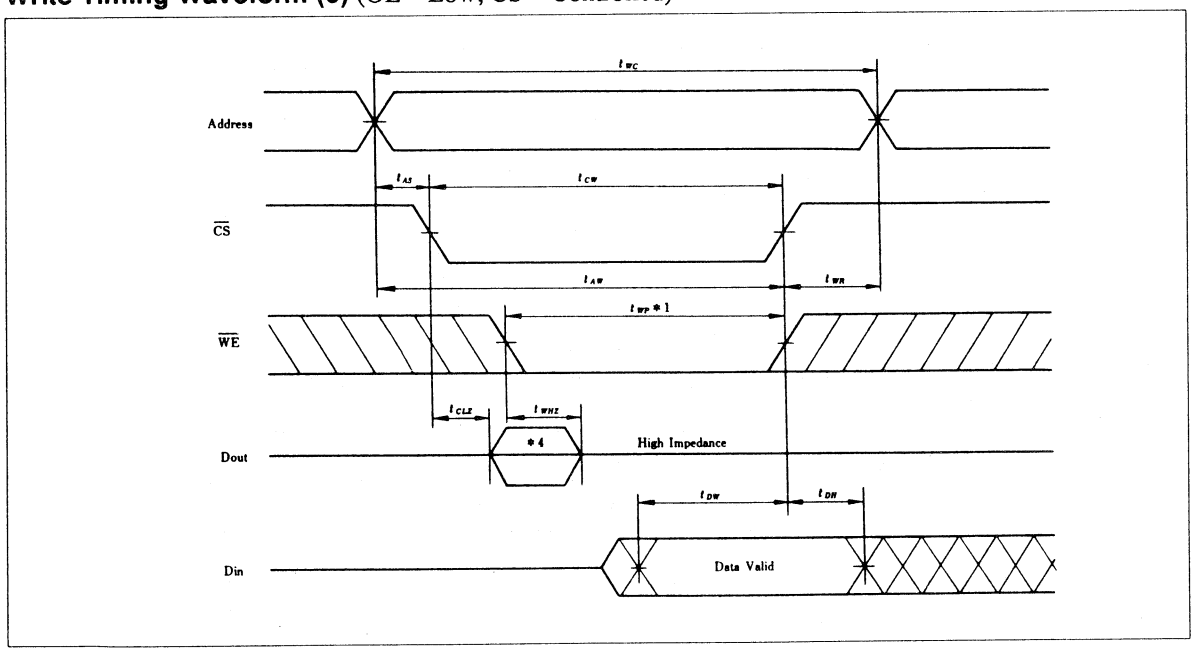
Write Timing Waveform (4) ($\overline{OE}$ = Clocked, $\overline{CS}$ = Controlled)



Write Timing Waveform (5) ($\overline{OE}$ = Low, $\overline{WE}$ = Controlled)



Write Timing Waveform (6) ($\overline{OE}$ = Low, $\overline{CS}$ = Controlled)



Notes: *1 A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (tWP)
*2. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state after tOW. Then the data input signals of opposite phase to the outputs must not be applied to them.
*6. Dout is the same phase of write data of this write cycle, if tWR is long enough.
*7. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

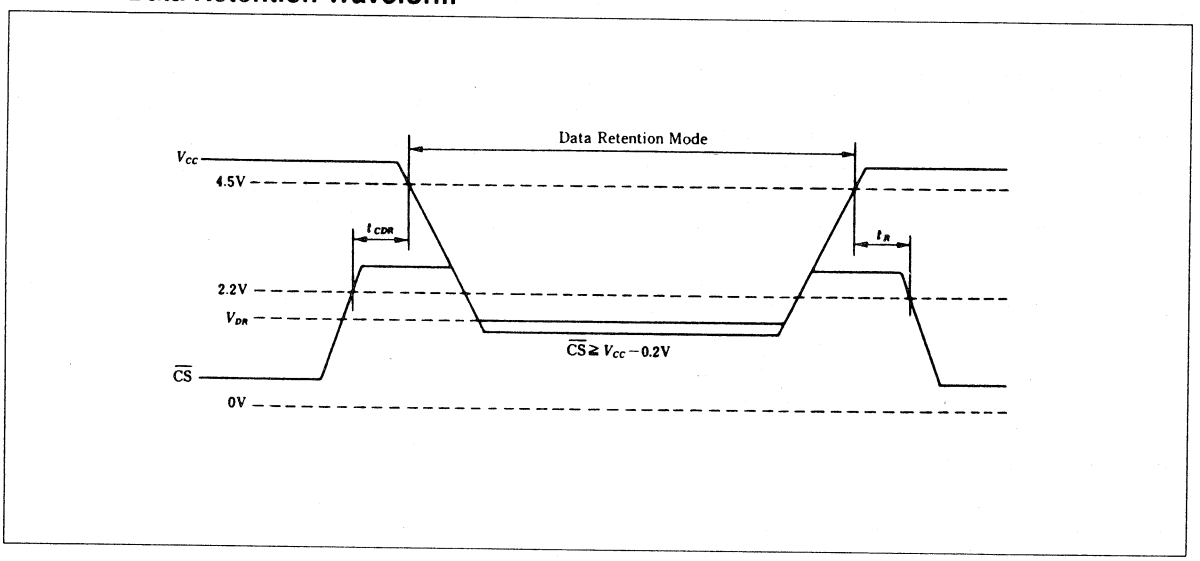
Low Vcc Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Vcc for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq Vcc - 0.2$ V,
Data retention current	I_{CCDR}	—	—	50*2	µA	Vin ≥ Vcc – 0.2 V or
				35*3		0 V ≤ Vin ≤ 0.2 V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*1	—	—	ns	

Note: *1. t_{RC} = Read cycle time
*2. Vcc = 3.0 V
*3. Vcc = 2.0 V

Low Vcc Data Retention Waveform



HM6789HA Series

16384-word × 4-bit High Speed Hi-BiCMOS Static RAM (with $\overline{OE}$)

Features

- 16384-word × 4bit organization
- 1.3 µm Hi-BiCMOS process
- Super fast access time: Add. 12/15 ns (max)
  $\overline{OE}$ 6/7 ns (max)
- Low power dissipation (DC) operating: 300 mW (typ)
- +5V single supply
- Completely static memory
  No clock or timing strobe required
- Fully TTL compatible input and output

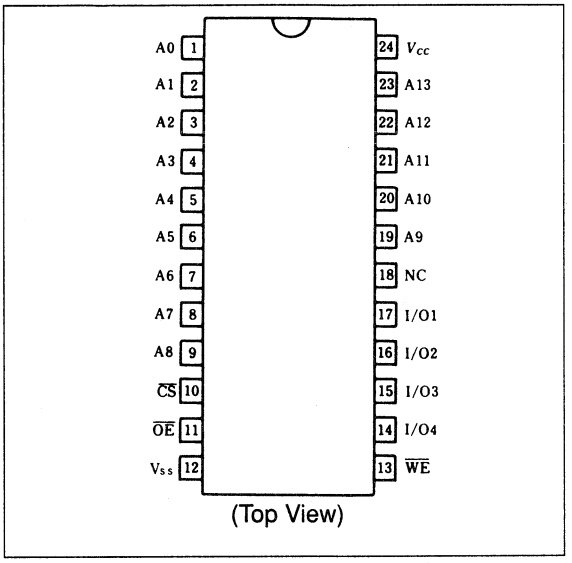
Ordering Information

Type No.	Access time	Package
HM6789HAP-12	12 ns	300-mil 24-pin plastic DIP (DP-24NC)
HM6789HAP-15	15 ns	
HM6789HAJP-12	12 ns	300-mil 24-pin plastic SOJ (CP-24D)
HM6789HAJP-15	15 ns	

Pin Description

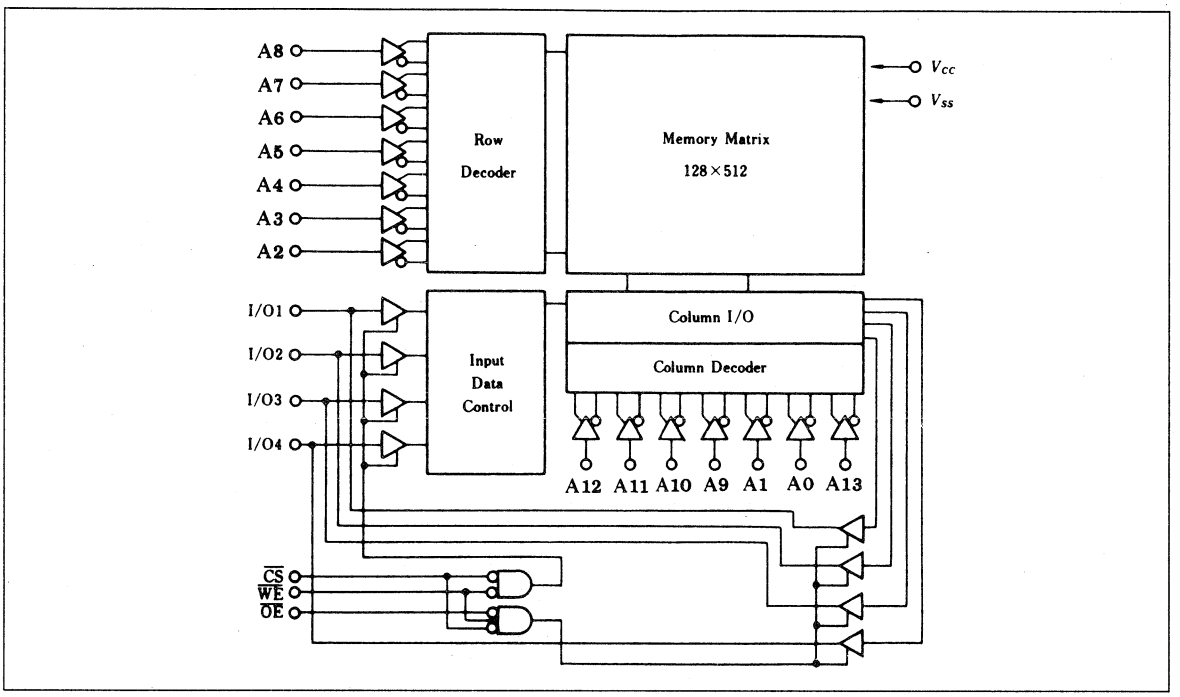
Pin Name	Function
A0 – A13	Address input
I/O1 – I/O4	Data input/output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
V_{SS}	Ground
V_{CC}	Power supply
NC	No connection

Pin Arrangement



(Top View)

Block Diagram



Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
H	H or L	H or L	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	H	Output disabled	I_{CC}, I_{CC1}	High-Z	—
L	L	H	Read	I_{CC}, I_{CC1}	Data out	Read cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Data in	Write cycle (1) (2) (3) (4)
L	L	L		I_{CC}, I_{CC1}	Data in	Write cycle (5) (6)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +7.0	V
Power dissipation	R_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range (with bias)	Tstg (bias)	–10 to +85	°C
Storage temperature range	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (0°C ≤ Ta ≤ 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input high voltage	V_{IH}	2.2	—	6.0	V
Input low voltage	V_{IL}*1	–3.0	—	0.8	V

Note: 1. Pulse Width ≤ 10 nS, DC : –0.5V

DC Characteristics (V_{CC} = 5V ± 10%, Ta = 0°C to +70°C, V_{SS} = 0V)

Item	Symbol	Min	Typ	Max	Unit	Test condition
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	V_{CC} = 5.5 V, Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	10	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $\overline{WE}$ = V_{IL} $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current	I_{CC}	—	—	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA
Average operating current	I_{CC1}	—	—	120	mA	min. cycle, Duty : 100%, $I_{I/O}$ = 0 mA
Standby power supply current	I_{SB}	—	—	30	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}	—	—	10	mA	$\overline{CS}$ ≥ V_{CC} –0.2 V Vin ≤ 0.2 V or Vin ≥ V_{CC} –0.2 V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4 mA

Capacitance (Ta = 25°C, f = 1.0 MHz)

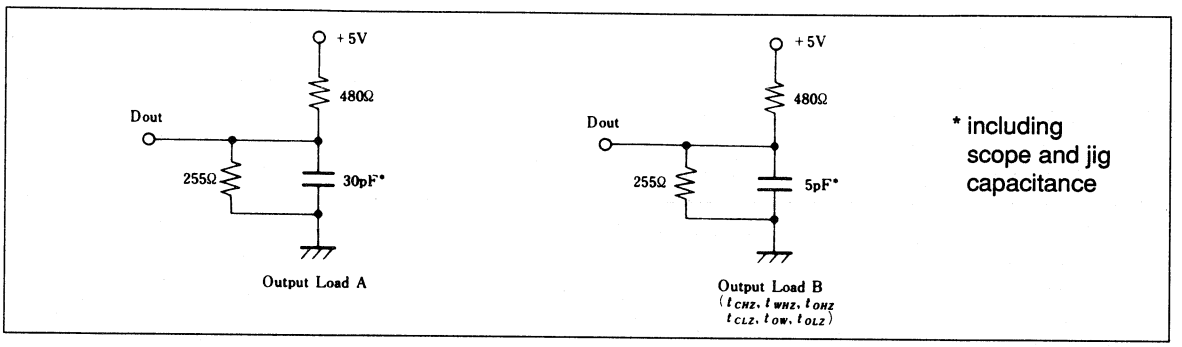
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input /output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note: This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC} = 5V ± 10%, Ta = 0°C to +70°C, unless otherwise noted)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input and output reference levels: 1.5 V ±200 mV from steady level (Output Load B)
- Input rise and fall time: 4 ns
- Output load: See figures



Read Cycle

Item	Symbol	HM6789HA–12 Min	HM6789HA–12 Max	HM6789HA–15 Min	HM6789HA–15 Max	Unit	Notes
Read cycle time	t_{RC}	12	—	15	—	ns	—
Address access time	t_{AA}	—	12	—	15	ns	—
Chip select access time	t_{ACS}	—	12	—	15	ns	—
Chip selection to output in low-Z	t_{CLZ}	3	—	5	—	ns	1, 2
Output enable to output valid	t_{OE}	0	6	0	7	ns	1
Output enable to output in low-Z	t_{OLZ}	1	—	1	—	ns	1, 2
Chip deselection to output in high-Z	t_{CHZ}	0	6	0	6	ns	1, 2
Output hold from address change	t_{OH}	4	—	4	—	ns	—

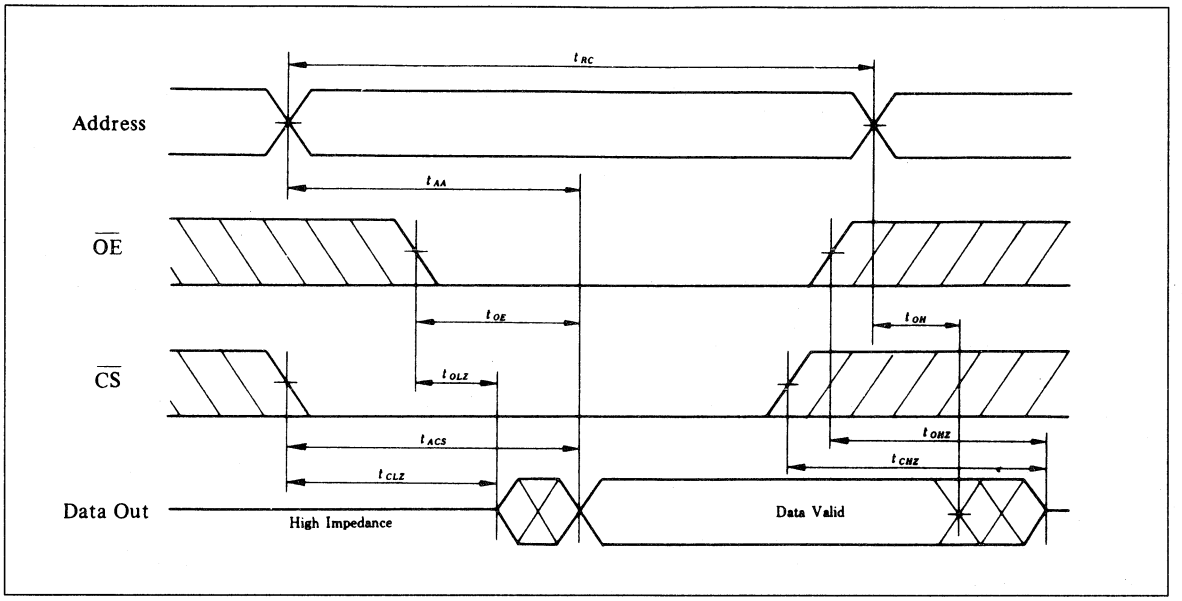
Write Cycle

Item	Symbol	HM6789HA–12 Min	HM6789HA–12 Max	HM6789HA–15 Min	HM6789HA–15 Max	Unit	Notes
Write cycle time	t_{WC}	12	—	15	—	ns	4
Chip selection to end of write	t_{CW}	8	—	10	—	ns	—
Address setup time	t_{AS}	0	—	0	—	ns	—
Address valid to end of write	t_{AW}	8	—	10	—	ns	—
Write pulse width	t_{WP}	8	—	10	—	ns	—
Write recovery time ($\overline{WE}$)	t_{WR}	0.5	—	0.5	—	ns	—
Write recovery time ($\overline{CS}$)	t_{WR1}	1	—	1	—	ns	—
Write to output in high-Z	t_{WHZ}	0	6	0	6	ns	1, 2
Data valid to end of write	t_{DW}	6	—	7	—	ns	—
Data hold time	t_{DH}	0	—	0	—	ns	—
Output disable to output in high-Z	t_{OHZ}	0	5	0	5	ns	1, 2
Output active from end of write	t_{OW}	3	—	3	—	ns	1, 2

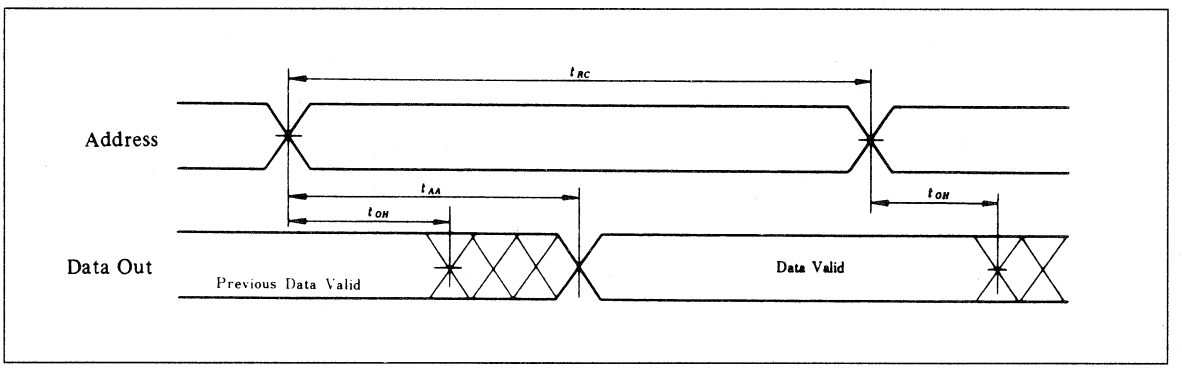
Notes: 1. Transition is measured ±200 mV from steady state voltage with Load (B).
2. This parameter is sampled and not 100% tested.
3. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
4. All write cycle timings are referenced from the last valid address to the first transitioning address.

Timing Waveform

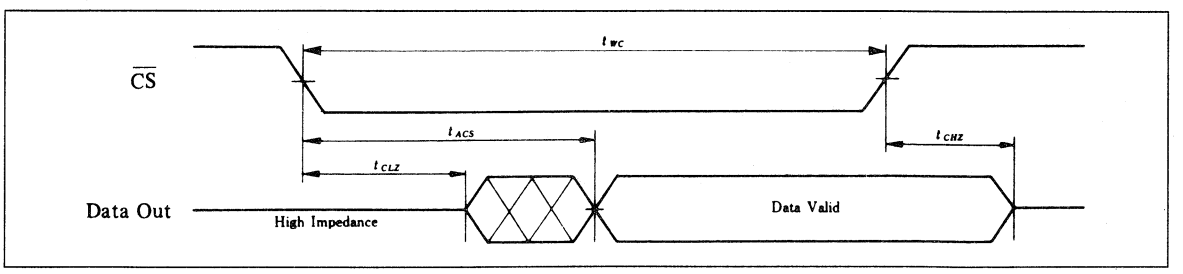
Read Cycle (1) *1



Read Cycle (2) *1, *2, *3

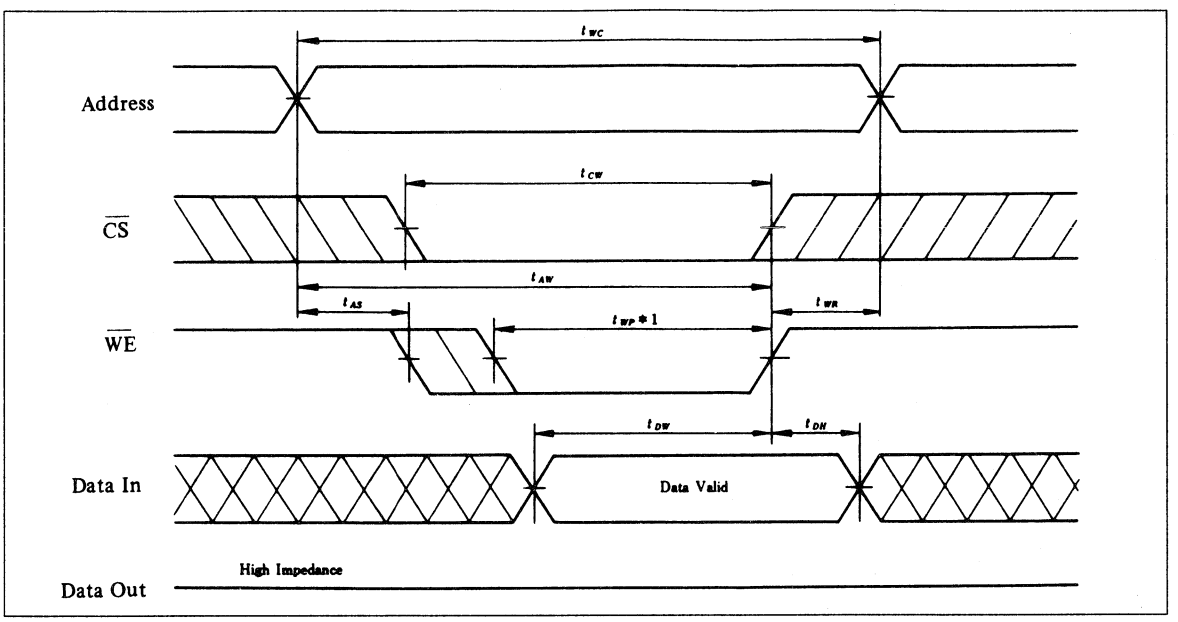


Read Cycle (3) *1, *3, *4

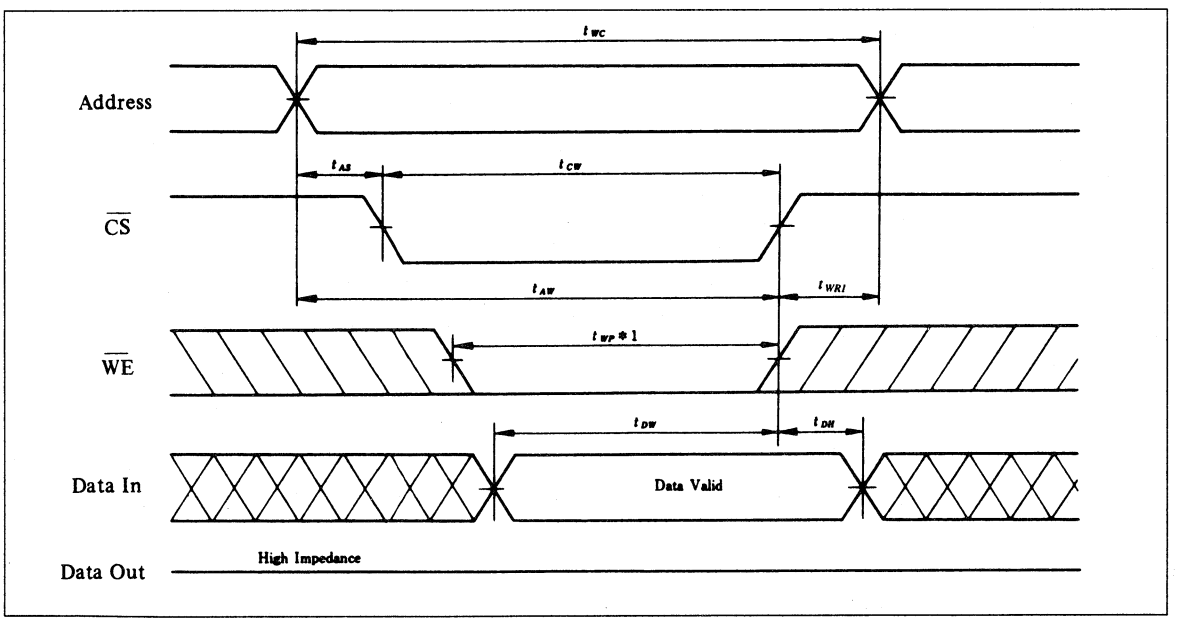


Notes: 1. $\overline{WE} = V_{IH}$
2. $\overline{CS} = V_{IL}$
3. $\overline{OE} = V_{IL}$
4. Address valid prior to or coincident with $\overline{CS}$ transition Low.

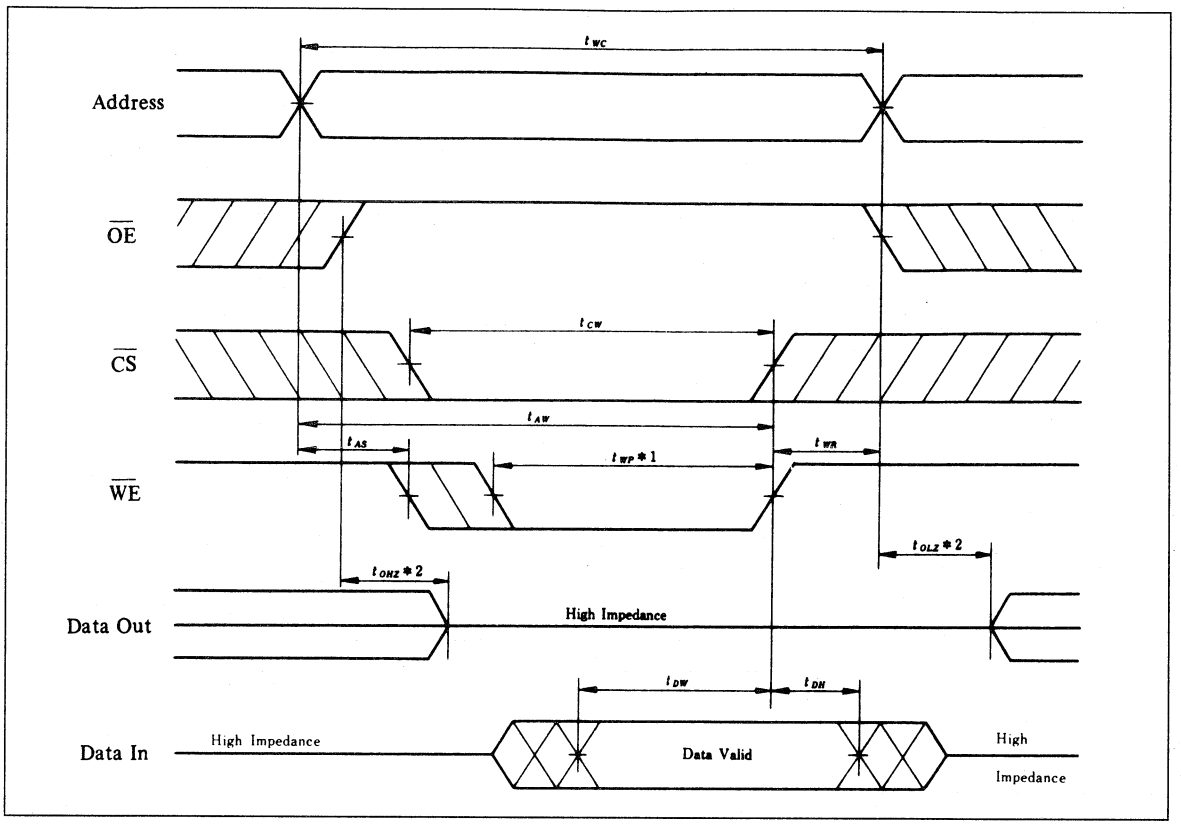
Write Cycle (1) ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



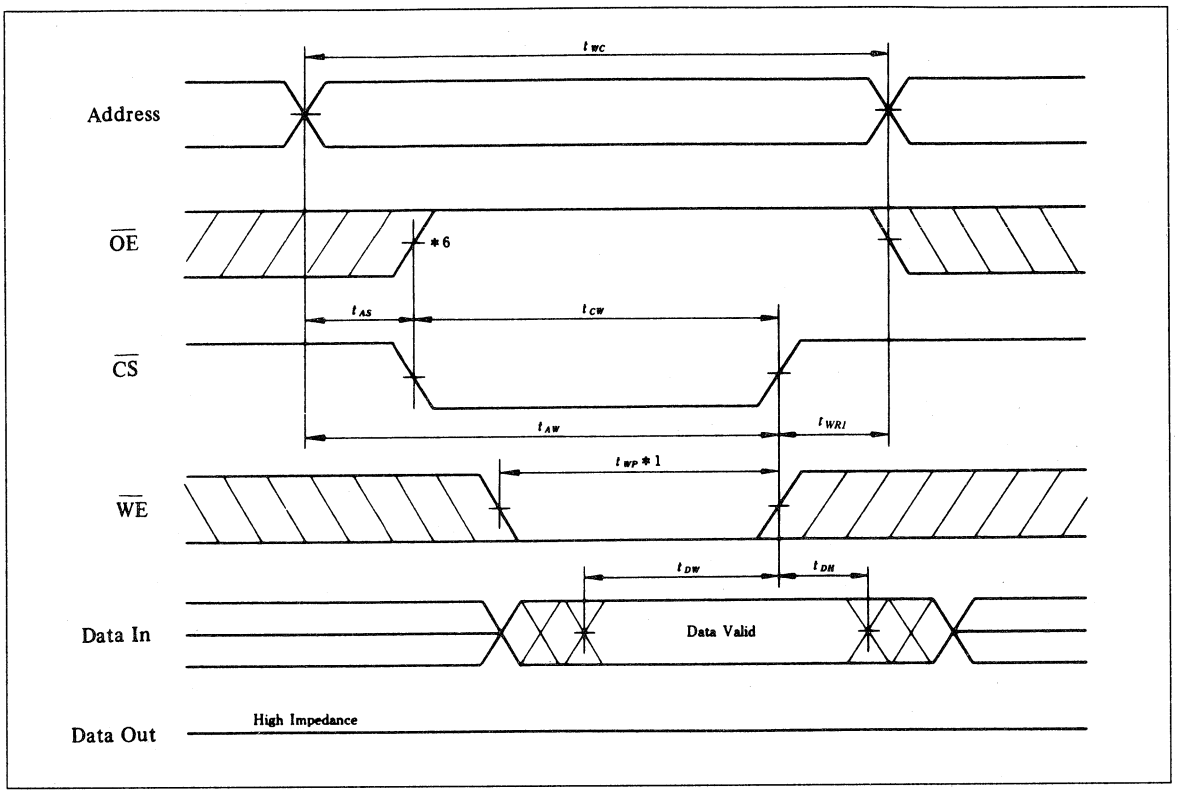
Write Cycle (2) ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



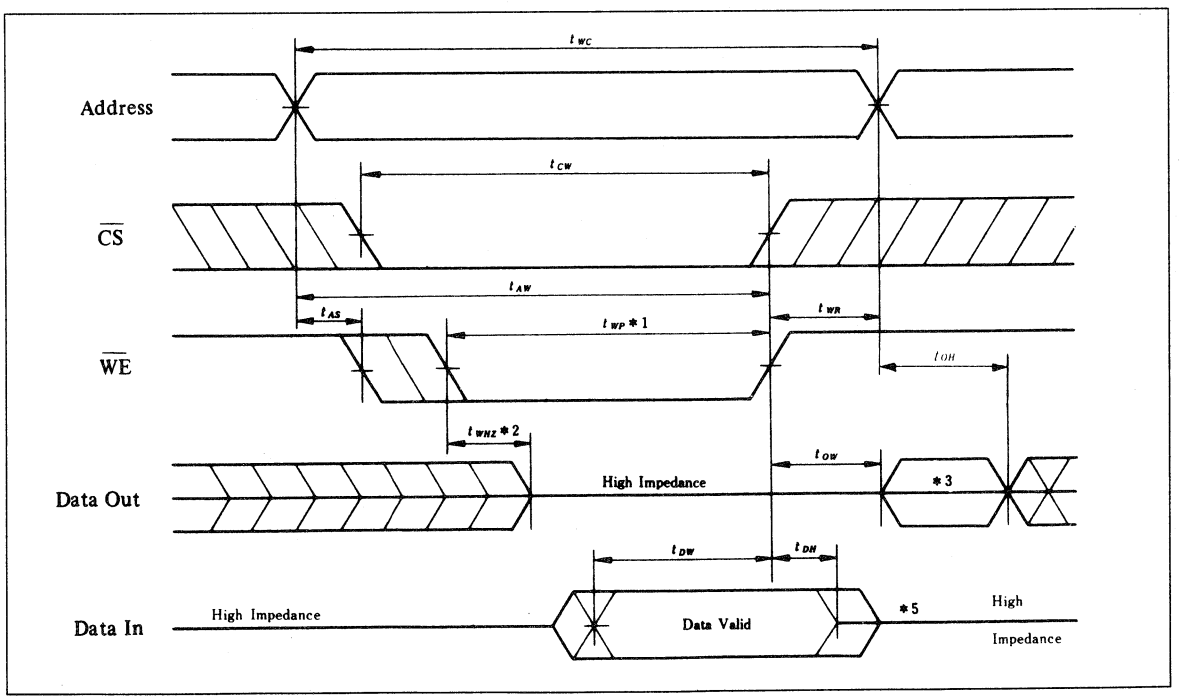
Write Cycle (3) ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



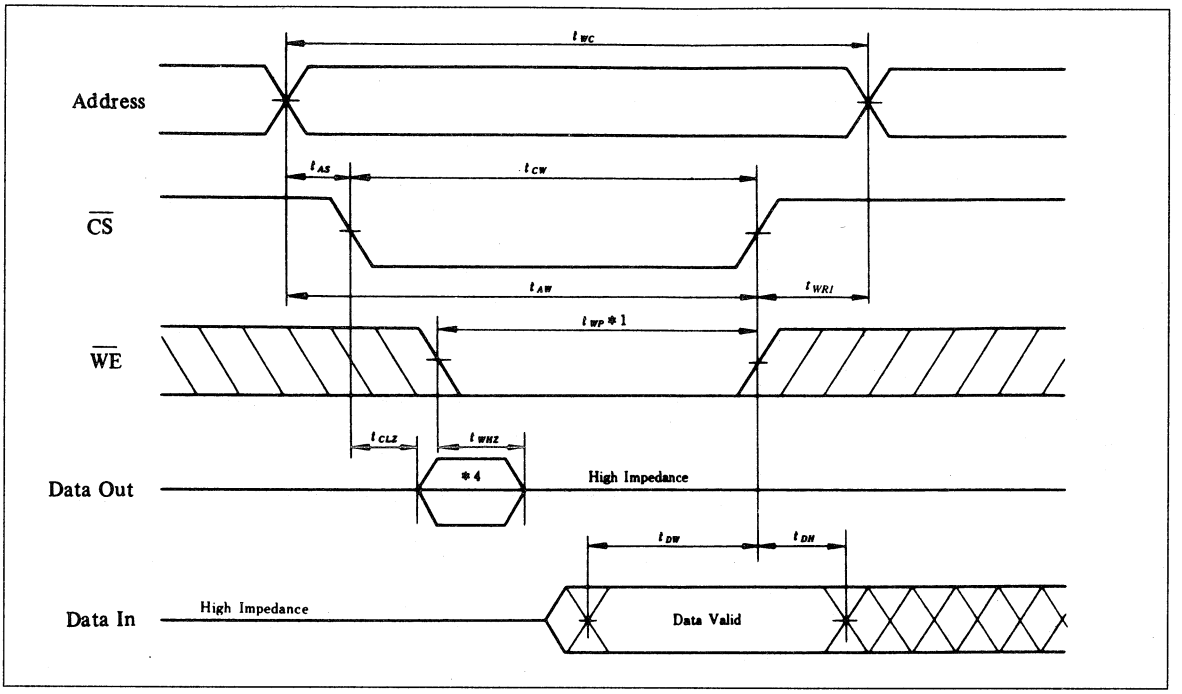
Write Cycle (4) ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



Write Cycle (5) ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



Write Cycle (6) ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



Notes:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
3. Dout is the same phase of write data of this write cycle.
4. If the $\overline{CS}$ is low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

HM6288 Series

16384-word×4-bit High Speed CMOS Static RAM

The Hitachi HM6288 is a high speed 64k static RAM organized as 16-kword x 4-bit. It realizes high speed access time (25/35/45 ns) and low power consumption, employing CMOS process technology.

It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM6288, packaged in a 300 mil plastic DIP and SOJ, is available for high density mounting. Low power version retains the data with battery back up.

■FEATURES

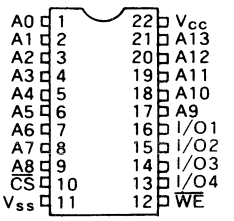
- Single 5V Supply and High Density Plastic Package.
- High Speed: Fast Access Time 25/35/45 ns (max.)
- Low Power dissipation
  - Active mode 300mW (typ.)
  - Standby mode 100μW (typ.)
- Completely Static Memory
  No Clock or Timing Strobe Required.
- Equal Access and Cycle Times.
- Directly TTL Compatible – All Inputs and Outputs.

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6288P-25 HM6288P-35	25ns 35ns	300 mil 22-pin Plastic DIP (DP-22NB)
HM6288LP-25 HM6288LP-35	25ns 35ns	
HM6288JP-25 HM6288JP-35	25ns 35ns	300 mil 24-pin SOJ (CP-24D)
HM6288LJP-25 HM6288LJP-35	25ns 35ns	

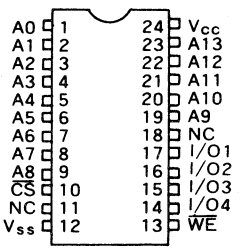
■PIN ARRANGEMENT

- HM6288P Series



(Top View)

- HM6288JP Series

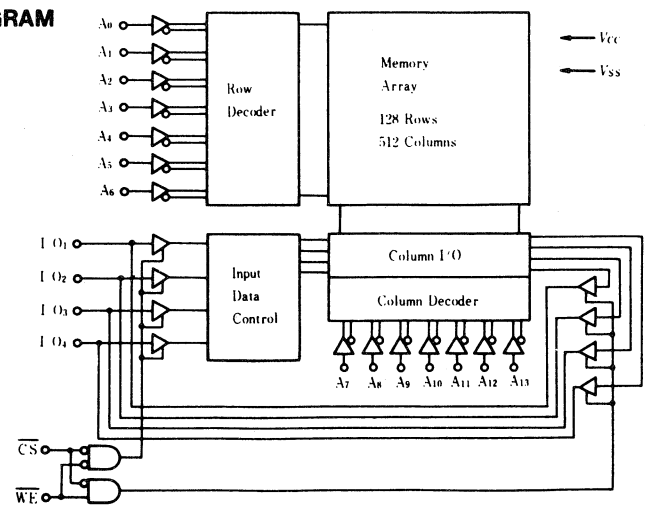


(Top View)

■Pin Description

Pin Name	Function
A0 - A13	Address
I/O1 – I/O4	Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-0.5^{*1} to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

Note: *1. V_T min. = −2.0V for pulse width ≦ 10ns

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	Standby	I_{SB}, I_{SB1}	High Z	--
L	H	Read	I_{CC}	Dout	Read'Cycle 1, 2
L	L	Write	I_{CC}	Din	Write Cycle 1, 2

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	–	6.0	V
Input Low (logic 0) Voltage	V_{IL}	-0.5^{*1}	–	0.8	V

Note: *1. V_{IL} min. = −2.0V for pulse width ≦ 10ns

■DC AND OPERATING CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC}=MAX. V_{IN}=V_{SS} to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}$=V_{IH}, $V_{I/O}$=V_{SS} to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA, min. cycle	–	60	120	mA
Standby V_{CC} Current	I_{SB}	$\overline{CS}$=V_{IH}, min. cycle	–	15	30	mA
Standby V_{CC} Current 1	I_{SB1}*2	$\overline{CS}$ ≧ V_{CC} −0.2V	–	0.02	2.0	mA
	I_{SB1}*3	0V ≦ V_{IN} ≦ 0.2V or V_{CC} −0.2V ≦ V_{IN}	–	0.02	0.1	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4.0mA	2.4	–	–	V

Notes: *1. Typical limits are at V_{CC}=5.0V, Ta=+25°C and specified loading.
*2. P version
*3. LP version

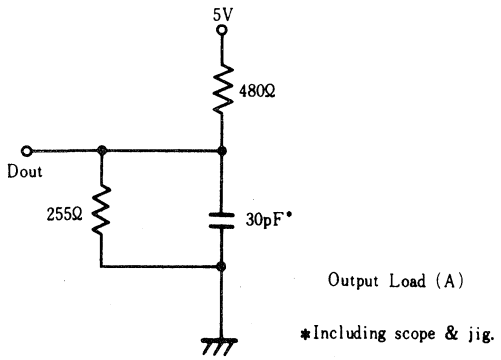
■CAPACITANCE (Ta=25°C, f=1.0MHz)

Parameter	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	8	pF

Note: This parameter is sampled and not 100% tested

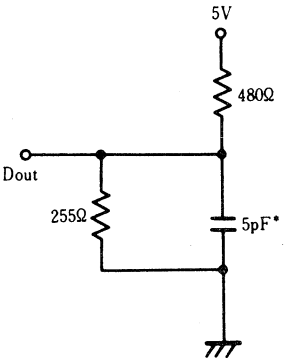
AC CHARACTERISTICS

- AC Test Conditions
  Input pulse levels: 0V to 3.0V
  Input rise and fall times: 5ns
  Input and Output timing reference levels: 1.5V
  Output load: See Figure



Output Load (A)

*Including scope & jig.



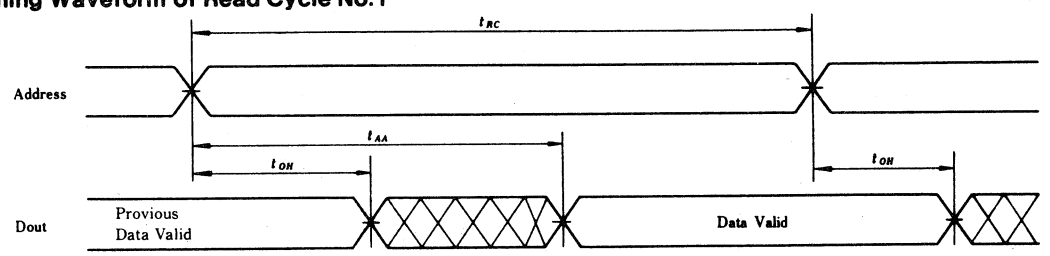
Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

READ CYCLE

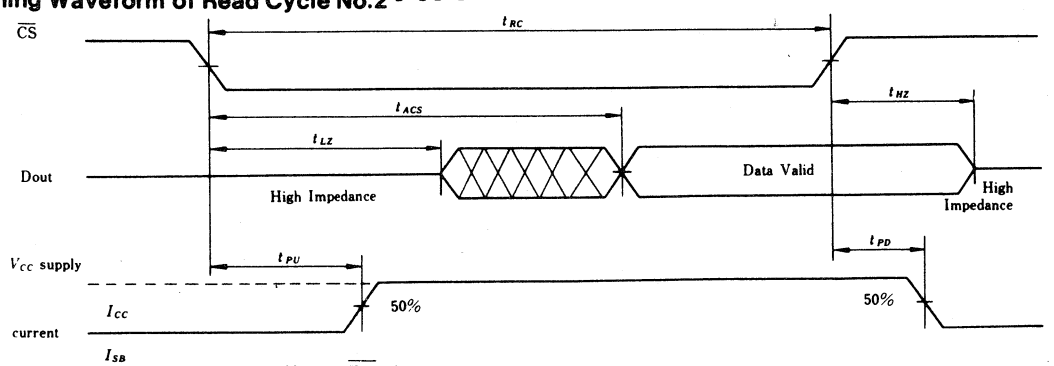
Parameter	Symbol	HM6288-25		HM6288-35		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	25	–	35	–	ns
Address Access Time	t_{AA}	–	25	–	35	ns
Chip Select Access Time	t_{ACS}	–	25	–	35	ns
Output Hold from Address Change	t_{OH}	3	–	5	–	ns
Chip Selection to Output in Low Z	t_{LZ}*	5	–	5	–	ns
Chip Deselection to Output in High Z	t_{HZ}*	0	12	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns
Chip Seselection to Power Down Time	t_{PD}	–	25	–	30	ns

* Transition is measured ±200mV from steady state voltage with Load(B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Read Cycle No.1 [1] [2]



● Timing Waveform of Read Cycle No.2 [1] [3]



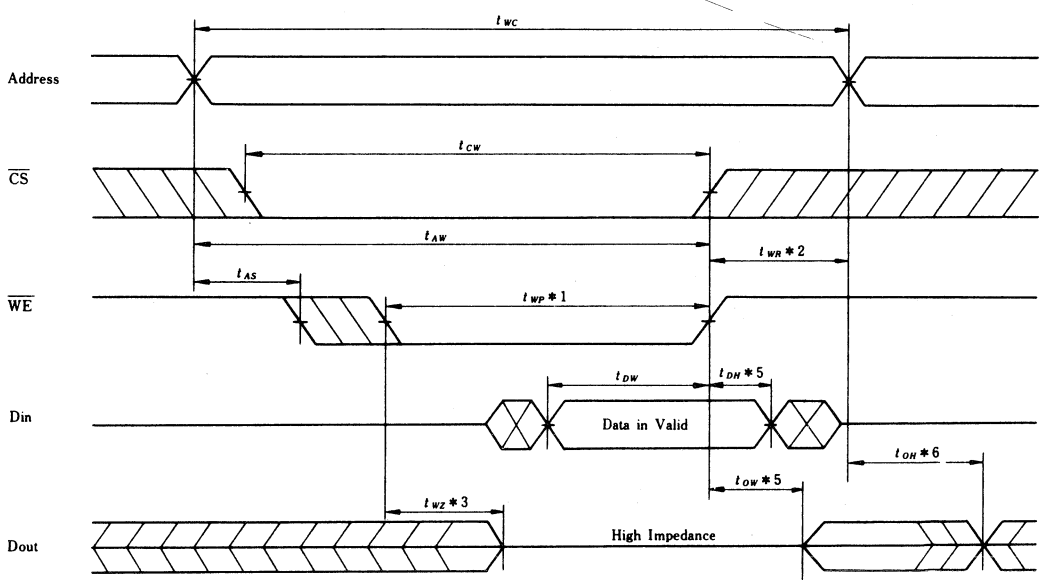
Notes: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

■ WRITE CYCLE

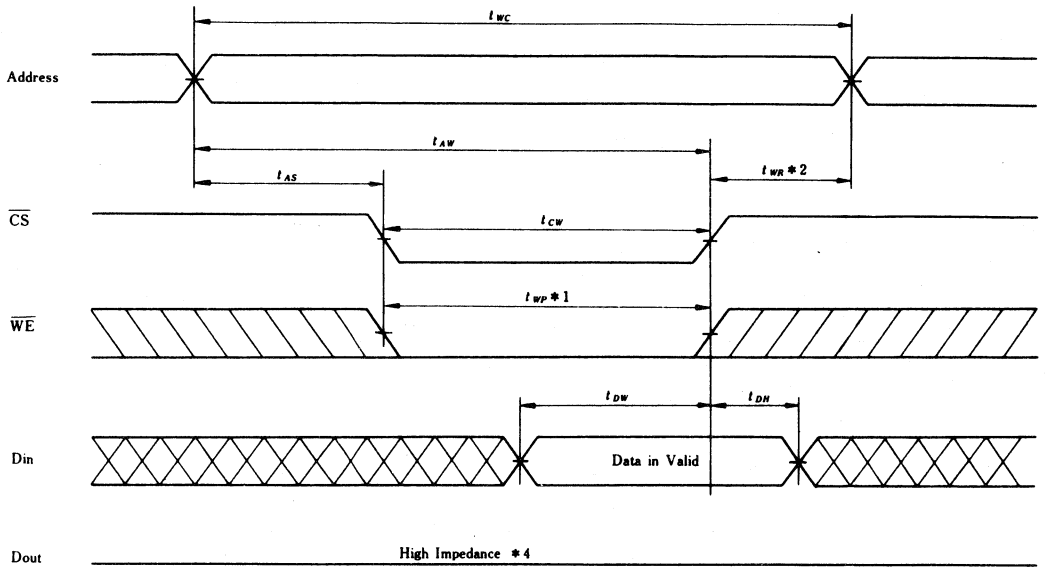
Parameter	Symbol	HM6288-25		HM6288-35		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	25	–	35	–	ns
Chip Selection to End of Write	t_{CW}	20	–	30	–	ns
Address Valid to End of Write	t_{AW}	20	–	30	–	ns
Address Setup Time	t_{AS}	0	–	0	–	ns
Write Pulse Width	t_{WP}	20	–	30	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	ns
Date Valid to End of Write	t_{DW}	12	–	20	–	ns
Data Hold Time	t_{DH}	0	–	0	–	ns
Write Enabled to Output in High Z	t_{WZ}*	0	8	0	10	ns
Output Active from End of Write	t_{OW}*	5	–	5	–	ns

* Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Write Cycle No.1 ($\overline{WE}$ Controlled)



● Timing Waveform of Write Cycle No.2 ($\overline{CS}$ Controlled)



Notes) 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state after tow. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

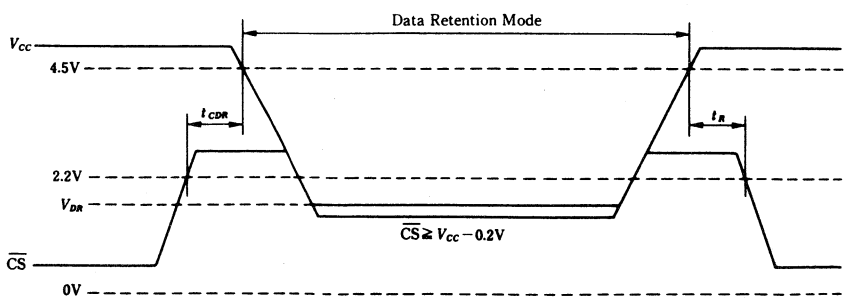
● Low *Vcc* Data Retention Characteristics (Ta=0 to +70°C)

(This Characteristics is guaranteed only for L-version.)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for data retention	V_{DR}	2.0	–	–	V	$\overline{CS} \geqq V_{CC}-0.2V$
Data retention current	I_{CCDR}	–	–	50[2] 35[3]	μA	$V_{in} \geqq V_{CC}-0.2V$ or $0V \leqq V_{in} \leqq 0.2V$
Chip deselect to data retention time	t_{CDR}	0	–	–	ns	See retention waveform
Operation recovery time	t_R	t_{RC}[1]	–	–	ns	

NOTE : 1. t_{RC} = Read cycle time
2. V_{CC} = 3.0V
3. V_{CC} = 2.0V

Low *Vcc* Data Retention Waveform



HM6788HA Series

16384-word × 4-bit High Speed Hi-BiCMOS Static RAM

Features

- 16384-word × 4 bit organization
- 1.3 µm Hi-BiCMOS process
- Super fast
  Access time: 12/15 ns (max)
- Low power dissipation
  (DC) operating: 300 mW (type)
- +5 V single supply
- Completely static memory no clock or timing strobe required
- Fully TTL compatible input and output

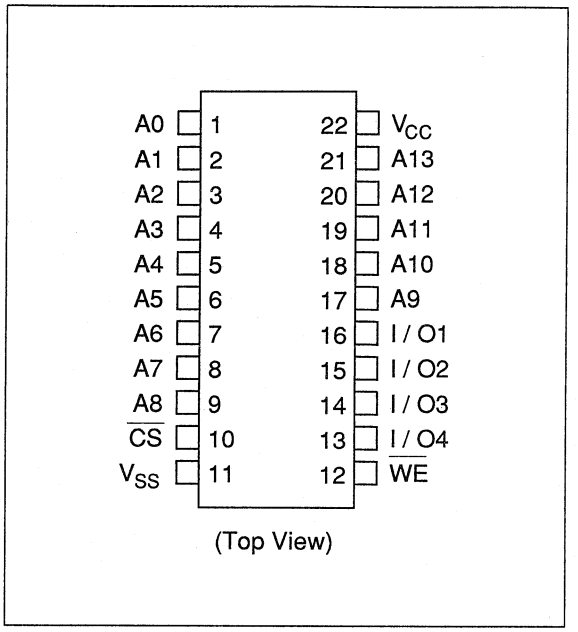
Ordering Information

Type No.	Cycle time	Package
HM6788HAP-12	12 ns	300-mil 22-pin plastic DIP (DP-22NB)
HM6788HAP-15	15 ns	

Pin Description

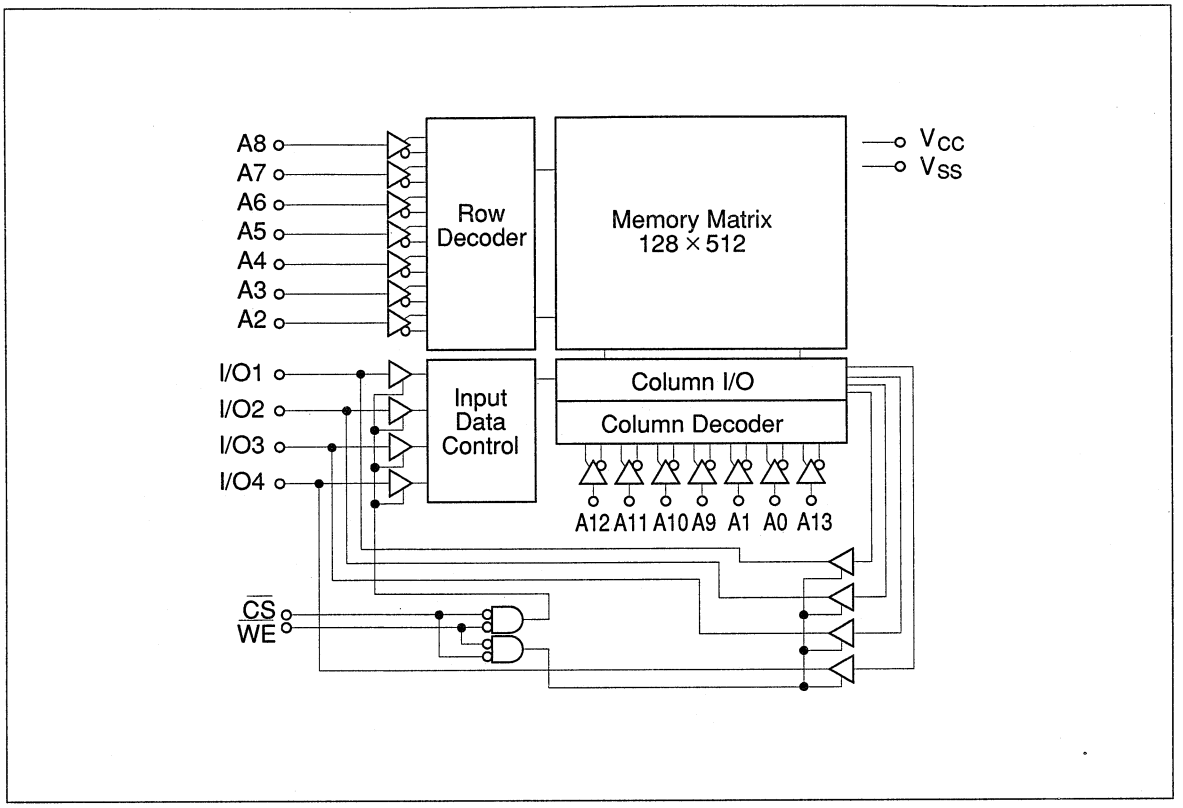
Pin name	Function
A0 – A13	Address input
I/O1 – I/O4	Data input/output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{SS}	Ground
V_{CC}	Supply voltage

Pin Arrangement



(Top View)

Block Diagram



Truth Table

Input

$\overline{CS}$	$\overline{WE}$	Output	Mode	V_{CC} current	Ref. cycle
H	X	High-Z	Not selected	I_{SB}, I_{SB1}	—
L	H	Dout	Read	I_{CC}, I_{CC1}	Read cycle (1), (2)
L	L	High-Z	Write	I_{CC}, I_{CC1}	Write cycle (1), (2)

Absolute Maximum Rating

Item	Symbol	Rating	Unit
Terminal voltage to V_{SS} pin	V_T	–0.5 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range (with bias)	Tstg (Bias)	–10 to +85	°C
Storage temperature range	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (0°C ≤ Ta ≤ 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input high voltage	V_{IH}	2.2	—	6.0	V
Input low voltage	V_{IL}	–3.0*1	—	0.8	V

Note: 1. Pulse width 10 ns, DC: –0.5 V

DC Characteristics (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	V_{CC} = 5.5 V, Vin = 0 V to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	10	µA	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = 0 V to V_{CC}
Operating power supply current	I_{CC}	—	—	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA
Average operating current	I_{CC1}	—	—	120	mA	min. cycle, Duty: 100%, $I_{I/O}$ = 0 mA
Standby power supply current	I_{SB}	—	—	30	mA	$\overline{CS}$ = V_{IH}, Vin = V_{IH} or V_{IL}
	I_{SB1}	—	—	10	mA	$\overline{CS}$ ≥ V_{CC} –0.2 V Vin ≤ 0.2 V or Vin ≥ V_{CC} –0.2V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4 mA

Capacitance (Ta = 25°C, f = 1 MHz)

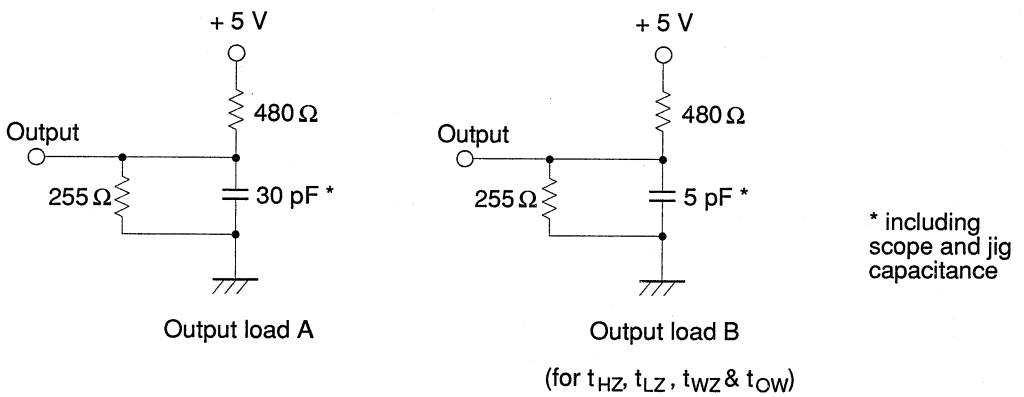
Item	Symbol	Max	Unit	Test condition
Input capacitance	C_{in}*1	6	pF	Vin = 0 V
Output capacitance	$C_{I/O}$*1	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC} = 5 V ±10%, Ta = 0°C to +70°C, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5 V
- Output load: See figures
- Input rise and fall times: 4 ns
- Output reference levels: 1.5 V



Read Cycle

Item	Symbol	HM6788HA-12 Min	HM6788HA-12 Max	HM6788HA-15 Min	HM6788HA-15 Max	Unit
Read cycle time	t_{RC}	12	—	15	—	ns
Address access time	t_{AA}	—	12	—	15	ns
Chip select access time	t_{ACS}	—	12	—	15	ns
Chip selection to output in low-Z	t_{LZ} *1, *2	3	—	5	—	ns
Chip deselection to output in high-Z	t_{HZ} *1, *2	0	6	0	6	ns
Output hold from address change	t_{OH}	4	—	4	—	ns

Notes: 1. This parameter is sampled and not 100% tested.
2. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).

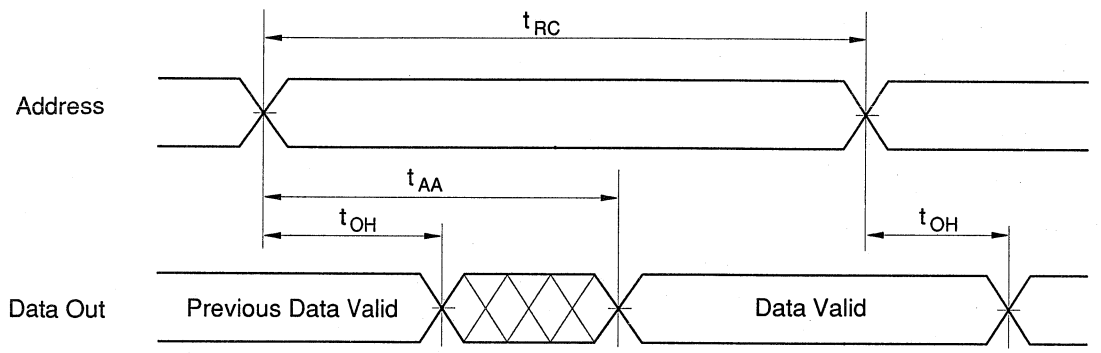
Write Cycle

Item	Symbol	HM6788HA-12 Min	HM6788HA-12 Max	HM6788HA-15 Min	HM6788HA-15 Max	Unit
Write cycle time	t_{WC} *1	12	—	15	—	ns
Chip selection to end of write	t_{CW}	8	—	10	—	ns
Address valid to end of write	t_{AW}	8	—	10	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	8	—	10	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0.5	—	0.5	—	ns
Write recovery time ($\overline{CS}$)	t_{WR1}	1	—	1	—	ns
Data valid to end of write	t_{DW}	6	—	7	—	ns
Data hold time	t_{DH}	0	—	0	—	ns
Write enable to output in high-Z	t_{WZ} *2, *3	0	6	0	6	ns
Output active from end of write	t_{OW} *2, *3	3	—	3	—	ns

Notes: 1. All write cycle timings are referenced from the last valid address to the first transitioning address.
2. This parameter is sampled and not 100% tested.
3. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).
4. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

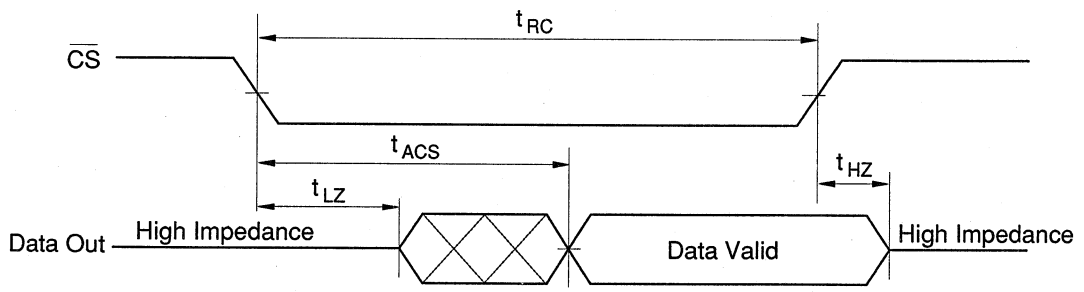
Timing Waveforms

Read Cycle (–1) *1, *2



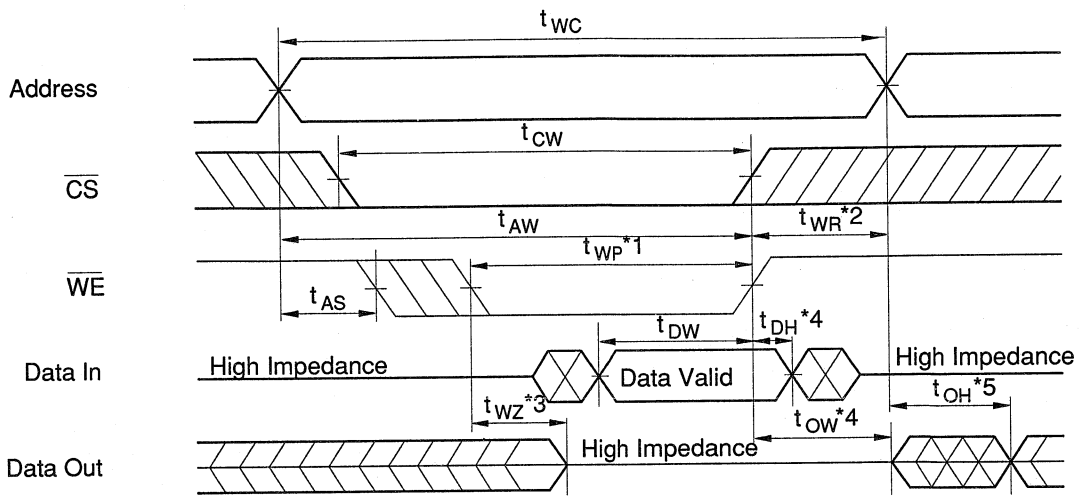
Notes : 1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.

Read Cycle (–2) *1, *2



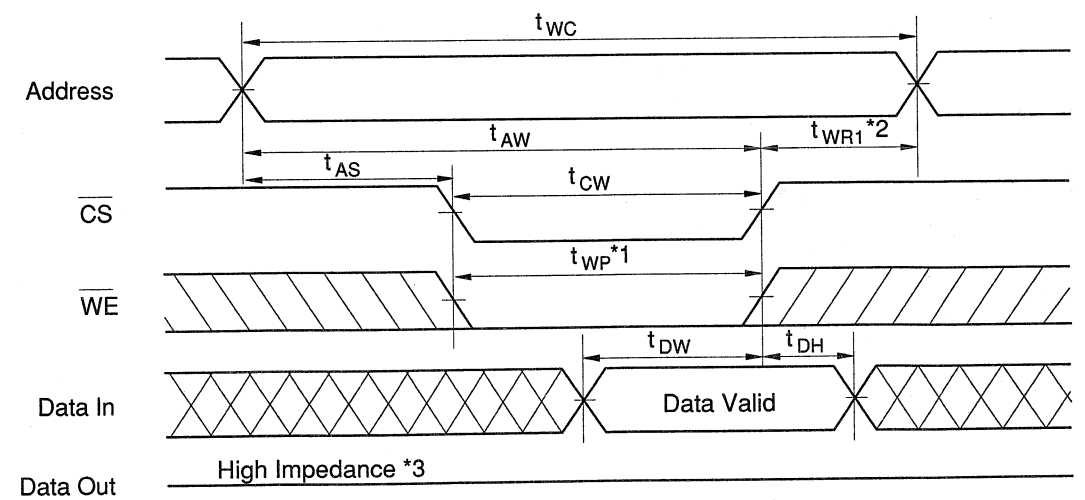
Note : 1. $\overline{WE}$ is high and $\overline{CS}$ is low for read cycle.
2. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle (–1) *1, *2, *3, *4, *5 ($\overline{WE}$ Controlled)



Notes : 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I / O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If $\overline{CS}$ is low during this period, I / O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
5. Output data is the same phase of write data of this write cycle.

Write Cycle (–2) *1, *2, *3 ($\overline{CS}$ Controlled)



Notes : 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR1} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high inpedance state.

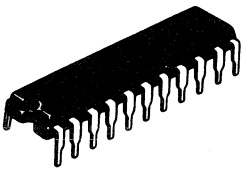
HM6287, HM6287H Series

65536-Word × 1-Bit High Speed CMOS Static RAM

The Hitachi HM6287H is a high speed 64K static RAM organized as 64-kword × 1-bit. It realizes high speed access time (25/35 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU. The HM6287H packaged in a 300-mil plastic DIP and SOJ, is available for high density mounting.

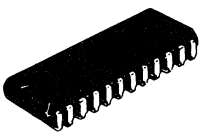
Low power version retains the data with battery back up.

HM6287P/HP Series



(DP-22N/DP-22NB)

HM6287HJP Series



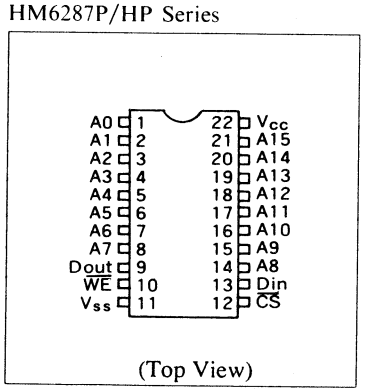
(CP-24D)

Features

- Single 5 V supply and high density 22-pin DIP and 24-pin SOJ
- High speed: Fast access time 25/35/45/55/70 ns (max)
- Low power
  - Operation: 300 mW (typ)
  - Standby: 100 µW (typ) /10 µW (typ) (L-version)
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation (L-version)

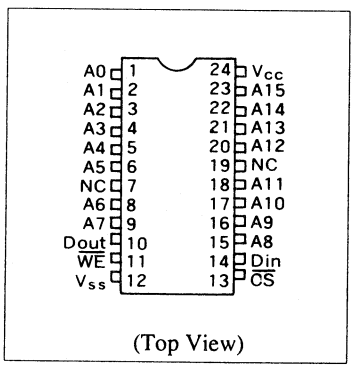
Pin Arrangement

HM6287P/HP Series



(Top View)

HM6287HJP Series



(Top View)

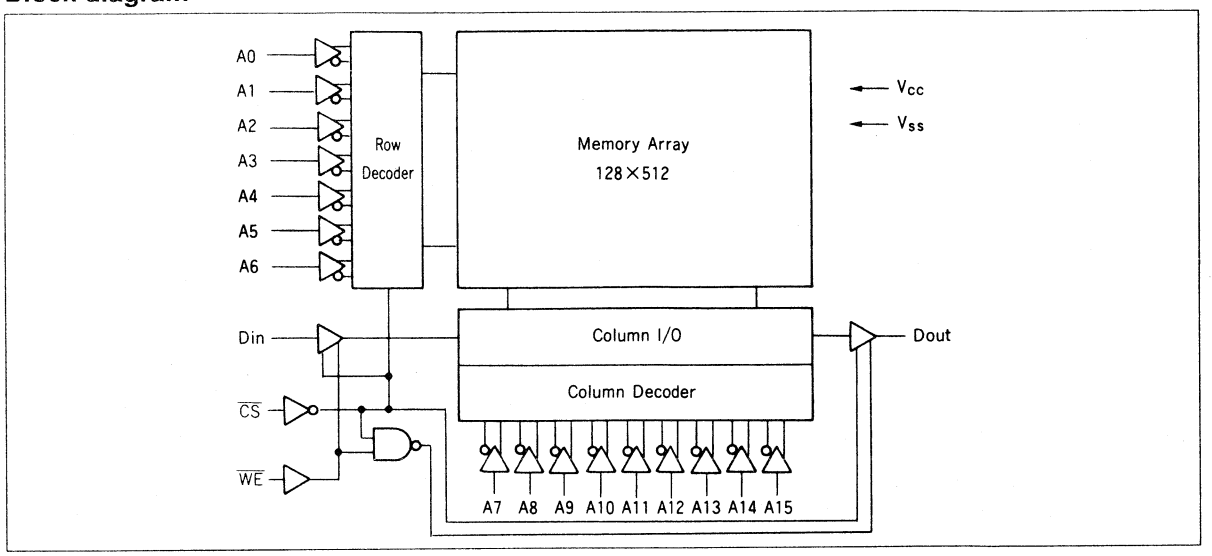
Pin Description

Pin Name	Function
A0 – A15	Address
Din	Input
Dout	Output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Ordering Information

Type No.	Access Time	Package
HM6287P-45	45 ns	300-mil 22-pin Plastic DIP (DP-22N)
HM6287P-55	55 ns	
HM6287P-70	70 ns	
HM6287LP-45	45 ns	
HM6287LP-55	55 ns	
HM6287LP-70	70 ns	
HM6287HP-25	25 ns	300-mil 22-pin Plastic DIP (DP-22NB)
HM6287HP-35	35 ns	
HM6287HLP-25	25 ns	
HM6287HLP-35	35 ns	
HM6287HJP-25	25 ns	300-mil 24-pin SOJ (CP-24D)
HM6287HJP-35	35 ns	
HM6287HLJP-25	25 ns	
HM6287HLJP-35	35 ns	

Block diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	Vcc Current	Dout Pin	Ref. Cycle
H	×	Standby	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	Icc	Dout	Read cycle 1, 2
L	L	Write	Icc	High-Z	Write cycle 1, 2

Note: ×: H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_T	–0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Note: *1. V_T min = –3.5 V for pulse width ≦ 20 ns (HM6287 Series)
V_T min = –2.0 V for pulse width ≦ 10 ns (HM6287H Series)

Recommended DC Operating Conditions (Ta = 0 to + 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
	Vss	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: *1. V_{IL} min = –3.0 V for pulse width ≦ 20 ns (HM6287 Series)
V_{IL} min = –2.0 V for pulse width ≦ 10 ns (HM6287H Series)

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	HM6287			HM6287H			Unit	Test Conditions
		Min	Typ*1	Max	Min	Typ*1	Max		
Input leakage current	$\|I_{LI}\|$	—	—	2.0	—	—	2.0	µA	V_{CC} = Max Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	2.0	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating V_{CC} current	I_{CC}	—	60	100	—	60	120	mA	$\overline{CS}$ = V_{IL} Iout = 0mA, min cycle
Standby V_{CC} current	I_{SB}	—	10	30	—	15	30	mA	$\overline{CS}$ = V_{IH}, min cycle
Standby V_{CC} current (1)	I_{SB1}	—	0.02	2.0	—	0.02	2.0	mA	$\overline{CS} \geqq V_{CC}$-0.2V 0V ≦ Vin ≦ 0.2V or V_{CC}-0.2V ≦ Vin
		—	0.02*2	0.1*2	—	0.02*2	0.1*2	mA	
Output low voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH} = -4.0 mA

Notes: *1. Typical limits are at V_{CC} = 5.0 V, Ta = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

Capacitance (Ta = 25°C, f = 1.0 MHz)*1

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	—	8	pF	Vout = 0 V

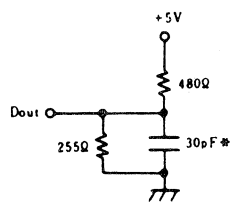
Note: *1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

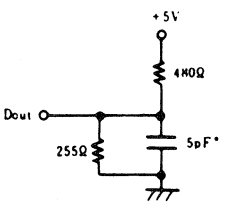
Test Conditions

- Input pulse levels: Vss to 3.0 V
- Input rise and fall times: 5 ns
- Input and Output timing reference levels: 1.5 V
- Output load: See figures

Output Load (A)



Output Load (B) (for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

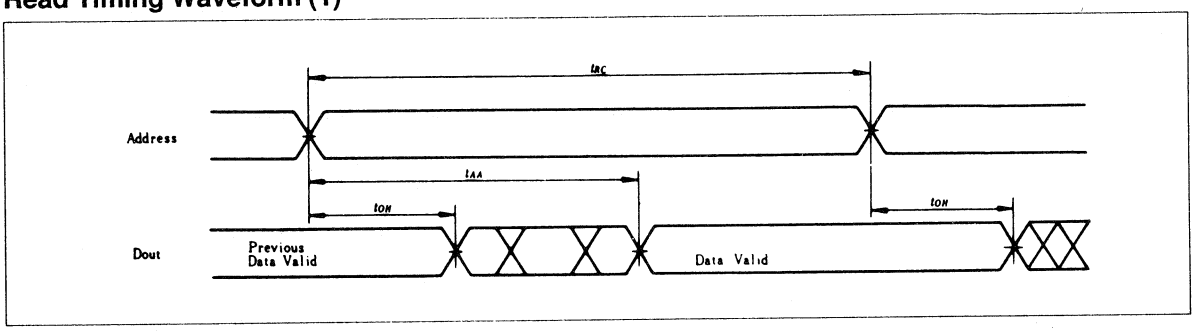


Note: Including scope & jig

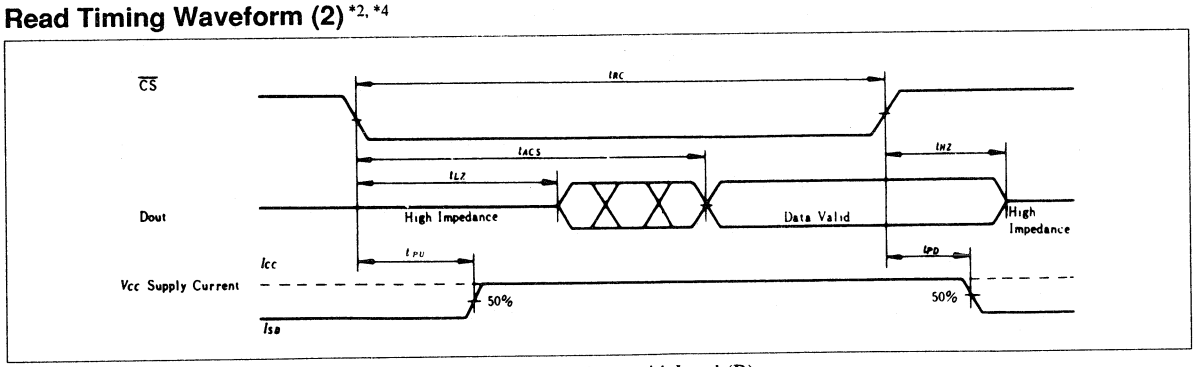
Read Cycle

Item	Symbol	HM6287H-25		HM6287H-35		HM6287-45		HM6287-55		HM6287-70		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	tRC	25	—	35	—	45	—	55	—	70	—	ns	5
Address access time	tAA	—	25	—	35	—	45	—	55	—	70	ns	
Chip select access time	tACS	—	25	—	35	—	45	—	55	—	70	ns	
Output hold from address change	tOH	3	—	5	—	5	—	5	—	5	—	ns	
Chip selection to output in low-Z	tLZ*1	5	—	5	—	5	—	5	—	5	—	ns	1,6,7
Chip deselection to output in high-Z	tHZ*1	0	12	0	20	0	30	0	30	0	30	ns	1,6,7
Chip selection to power up time	tPU	0	—	0	—	0	—	0	—	0	—	ns	7
Chip deselection to power down time	tPD	—	25	—	30	—	40	—	40	—	40	ns	7

Read Timing Waveform (1) *2, *3, *5



Read Timing Waveform (2) *2, *4

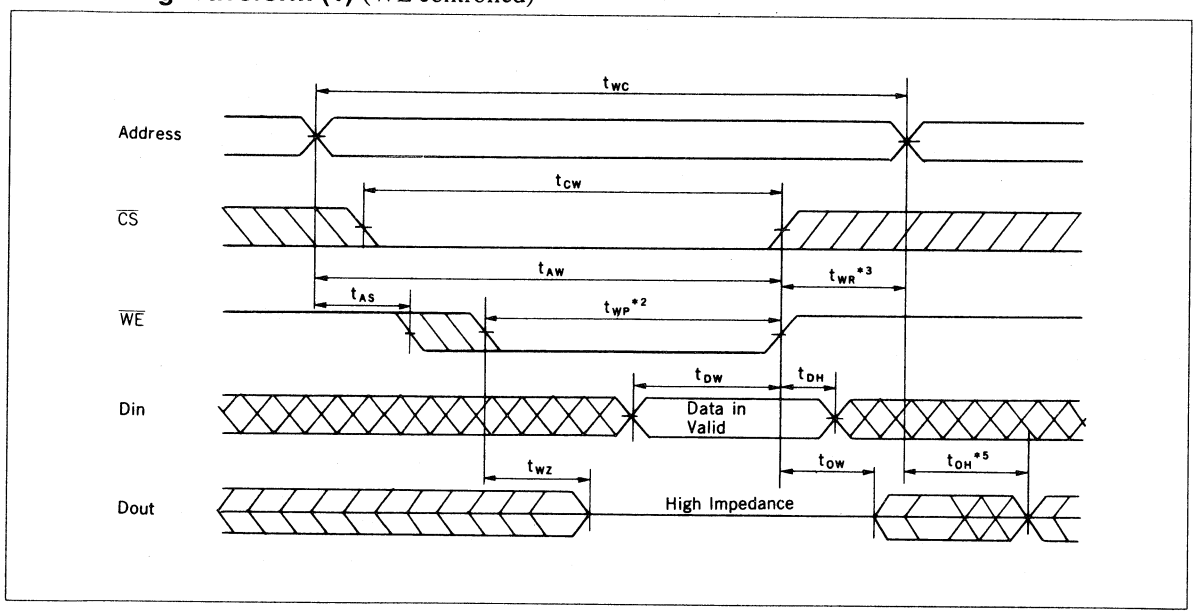


Notes: *1. Transition is measured ±200 mV from steady state voltage with Load (B).
*2. $\overline{WE}$ is high for read cycle.
*3. Device is continuously selected, $\overline{CS}$ = VIL.
*4. Address valid prior to or coincident with $\overline{CS}$ transition low.
*5. All read cycle timing are referenced from last valid address to the first transitioning address.
*6. At any given temperature and voltage condition, tHZ max. is less than tLZ min. both for a given device and from device to device.
*7. This parameter is sampled and not 100% tested.

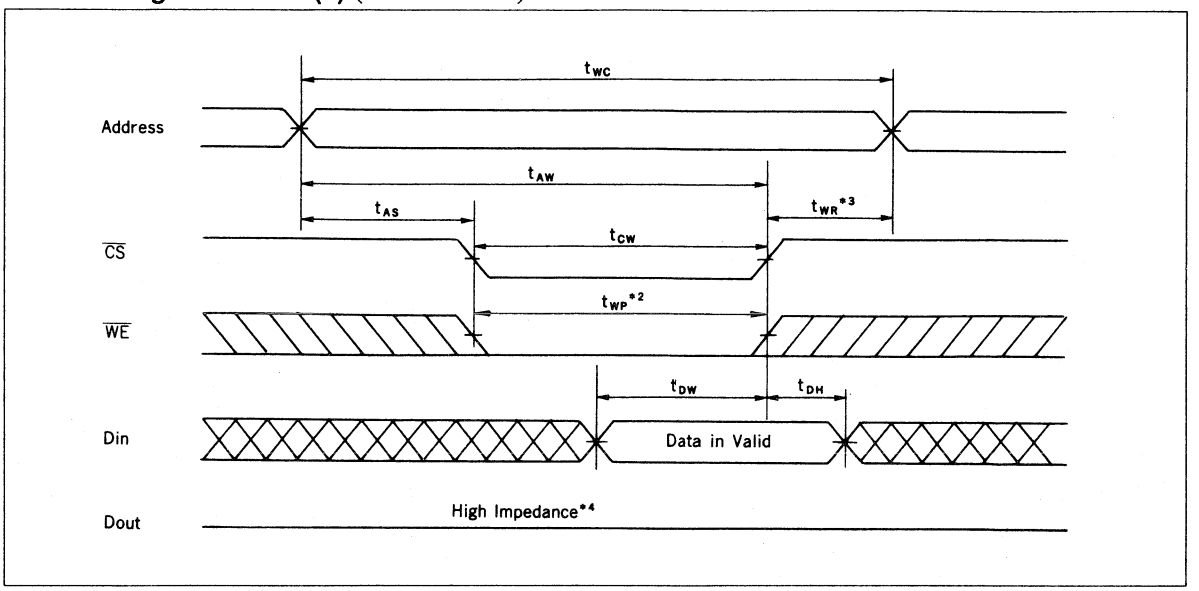
Write Cycle

Item	Symbol	HM6287H-25		HM6287H-35		HM6287-45		HM6287-55		HM6287-70		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	25	—	35	—	45	—	55	—	70	—	ns	6
Chip selection to end of write	t_{CW}	20	—	30	—	40	—	50	—	55	—	ns	
Address valid to end of write	t_{AW}	20	—	30	—	40	—	50	—	55	—	ns	
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Write pulse width	t_{WP}	20	—	30	—	25	—	35	—	40	—	ns	
Write recovery time	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	
Data valid to end of write	t_{DW}	15	—	20	—	25	—	25	—	30	—	ns	
Data hold time	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write enabled to output in high-Z	t_{WZ} *1	0	8	0	10	0	25	0	25	0	30	ns	1
Output active from end of write	t_{OW} *1	5	—	5	—	0	—	0	—	0	—	ns	1

Write Timing Waveform (1) (WE controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes: *1. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
*2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
*3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
*5. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.
*6. All write cycle timings are referenced from the last valid address to first transitioning address.

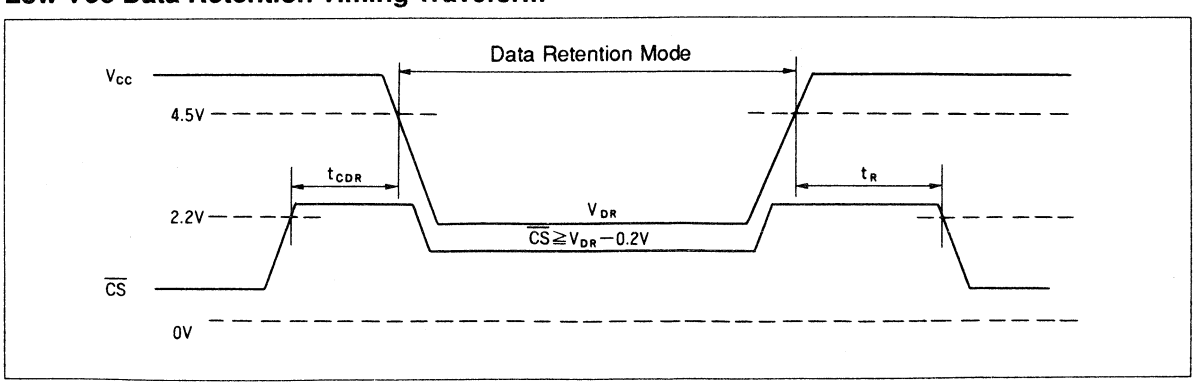
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

(This specification is guaranteed only for L-version.)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V
Data retention current	I_{CCDR}	—	—	50*2	µA	Vin ≥ Vcc – 0.2 V or
				35*3		0 V ≤ Vin ≤ 0.2 V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*1	—	—	ns	

Notes: *1. t_{RC} = Read cycle time
*2. V_{CC} = 3.0 V
*3. V_{CC} = 2.0 V

Low V_{CC} Data Retention Timing Waveform



HM6787HA Series

65536-word × 1-bit High Speed Static Random Access Memory

Features

- 65536-word × 1-bit organization
- 1.3 µm Hi-BiCMOS process
- Super fast
  Access time: 12/15 ns (max)
- Low power dissipation
  (DC) operating: 300 mW (typ)
- +5 V single supply
- Completely static memory no clock or timing strobe required
- Fully TTL compatible input and output

Ordering Information

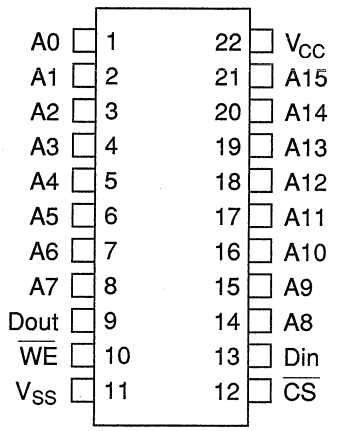
Type No.	Cycle time	Package
HM6787HAP-12	12 ns	300-mil 22-pin plastic DIP (DP-22NB)
HM6787HAP-15	15 ns	
HM6787HAJP-12	12 ns	300-mil 24-pin plastic SOJ (CP-24D)
HM6787HAJP-15	15 ns	

Pin Description

Pin name	Function
A0 – A15	Address input
Din	Data input
Dout	Data output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{SS}	Ground
V_{CC}	Supply voltage

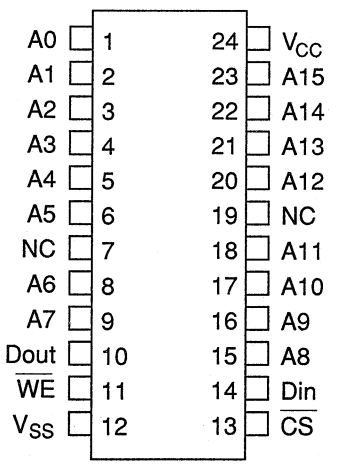
Pin Arrangement

HM6787HAP Series



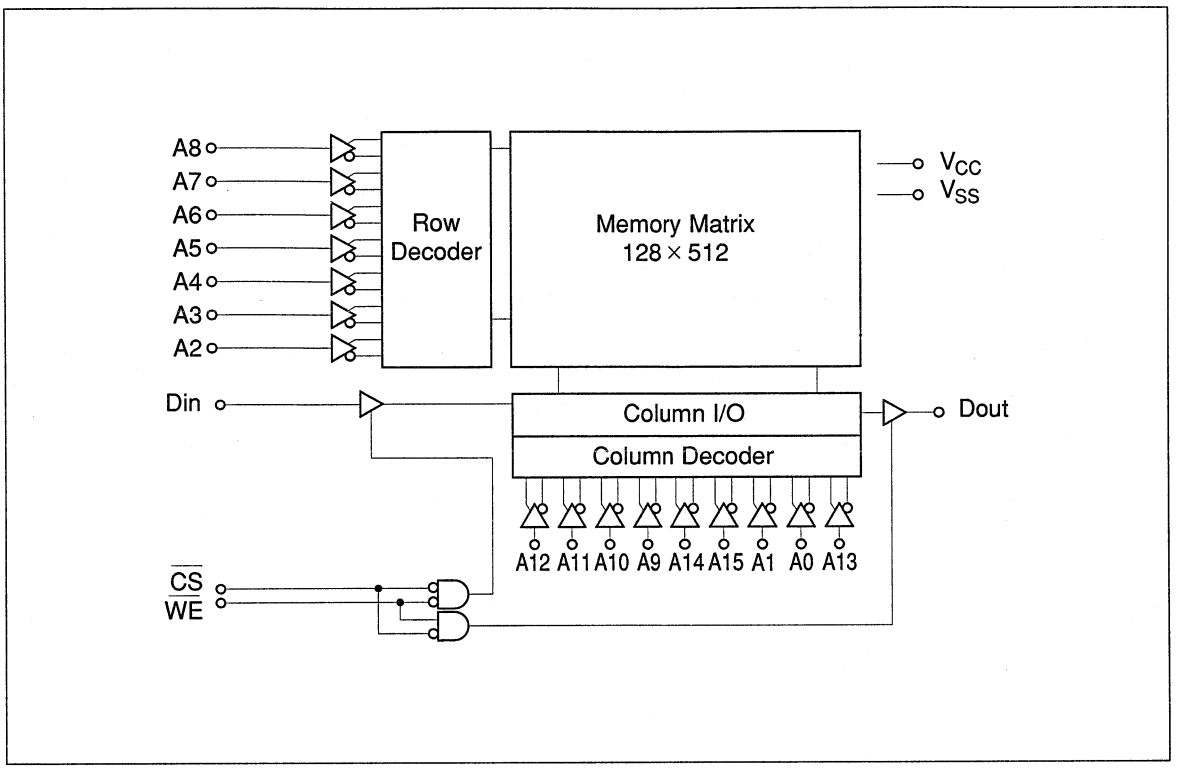
(Top View)

HM6787HAJP Series



(Top View)

Block Diagram



Truth Table

Input				
$\overline{CS}$	$\overline{WE}$	Output	Mode	V_{CC} current
H	X	High-Z	Not selected	I_{SB}, I_{SB1}
L	H	Dout	Read	I_{CC}, I_{CC1}
L	L	High-Z	Write	I_{CC}, I_{CC1}

Absolute Maximum Rating

Item	Symbol	Rating	Unit
Terminal voltage to V_{SS} pin	V_T	–0.5 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range (with bias)	Tstg (Bias)	–10 to +85	°C
Storage temperature range	Tstg	–55 to +125	°C

Recommended DC Operating Conditions ($0°C \leq Ta \leq 70°C$)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input high voltage	V_{IH}	2.2	—	6.0	V
Input low voltage	V_{IL}	–3.0*1	—	0.8	V

Note: 1. Pulse width 10 ns, DC: –0.5 V

DC Characteristics ($V_{CC} = 5.0\ V \pm 10\%$, $V_{SS} = 0\ V$, $Ta = 0$ to $+70°C$)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	V_{CC} = 5.5 V, Vin = 0 V to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	10	µA	$\overline{CS}$ = V_{IH}, Vout = 0 V to V_{CC}
Operating power supply current	I_{CC}	—	—	100	mA	$\overline{CS}$ = V_{IL}, Iout = 0 mA
Average operating current	I_{CC1}	—	—	120	mA	min. cycle, Duty: 100%, Iout = 0 mA
Standby power supply current	I_{SB}	—	—	30	mA	$\overline{CS}$ = V_{IH}, Vin = V_{IH} or V_{IL}
	I_{SB1}	—	—	10	mA	$\overline{CS} \geq V_{CC} - 0.2$ V Vin ≤ 0.2 V or Vin ≥ V_{CC} –0.2V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4 mA

Capacitance ($Ta = 25°C$, $f = 1$ MHz)

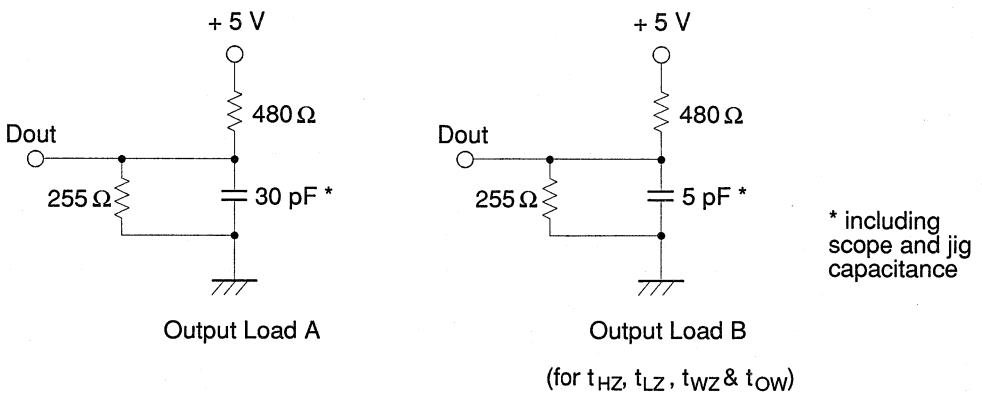
Item	Symbol	Max	Unit	Test condition
Input capacitance	C_{IN}*1	6	pF	Vin = 0 V
Output capacitance	C_{OUT}*1	10	pF	Vout = 0 V

Note : 1. This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC} = 5 V ± 10%, Ta = 0°C to +70°C, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5 V
- Output load: See figures
- Input rise and fall times: 4 ns
- Output reference levels: 1.5 V



Read Cycle

Item	Symbol	HM6787HA-12 Min	HM6787HA-12 Max	HM6787HA-15 Min	HM6787HA-15 Max	Unit
Read cycle time	t_{RC}	12	—	15	—	ns
Address access time	t_{AA}	—	12	—	15	ns
Chip select access time	t_{ACS}	—	12	—	15	ns
Output hold from address change	t_{OH}	4	—	4	—	ns
Chip selection to output in low-Z	t_{LZ}*1, *2	3	—	5	—	ns
Chip deselection to output in high-Z	t_{HZ}*1, *2	0	6	0	6	ns

Notes: 1. This parameter is sampled and not 100% tested.
2. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).

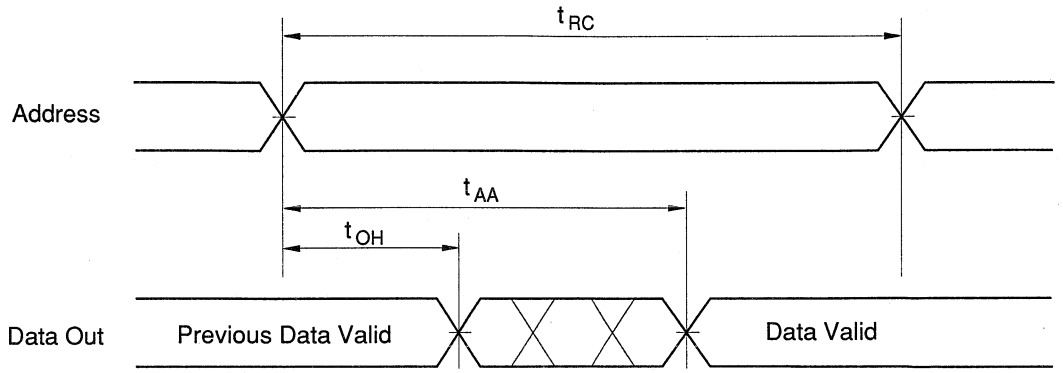
Write Cycle

Item	Symbol	HM6787HA-12 Min	HM6787HA-12 Max	HM6787HA-15 Min	HM6787HA-15 Max	Unit
Write cycle time	t_{WC} *1	12	—	15	—	ns
Chip selection to end of write	t_{CW}	8	—	10	—	ns
Address valid to end of write	t_{AW}	8	—	10	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	8	—	10	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0.5	—	0.5	—	ns
Write recovery time ($\overline{CS}$)	t_{WR1}	1	—	1	—	ns
Data valid to end of write	t_{DW}	7	—	8	—	ns
Data hold time	t_{DH}	0	—	0	—	ns
Write enable to output in high-Z	t_{WZ} *2, *3	0	6	0	6	ns
Output active from end of write	t_{OW} *2, *3	3	—	3	—	ns

Notes: 1. All write cycle timings are referenced form the last valid address to the first transitioning address.
2. This parameter is sampled and not 100% tested.
3. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).
4. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

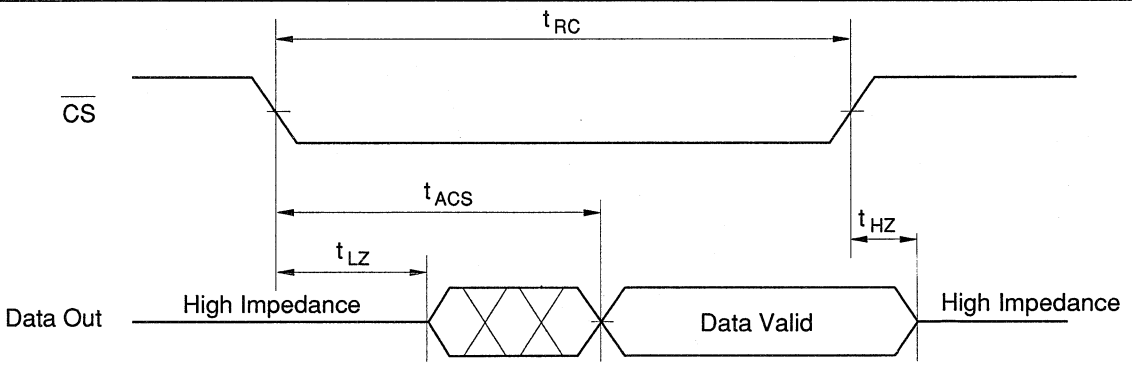
Timing Waveforms

Read Cycle (–1)*1, *2



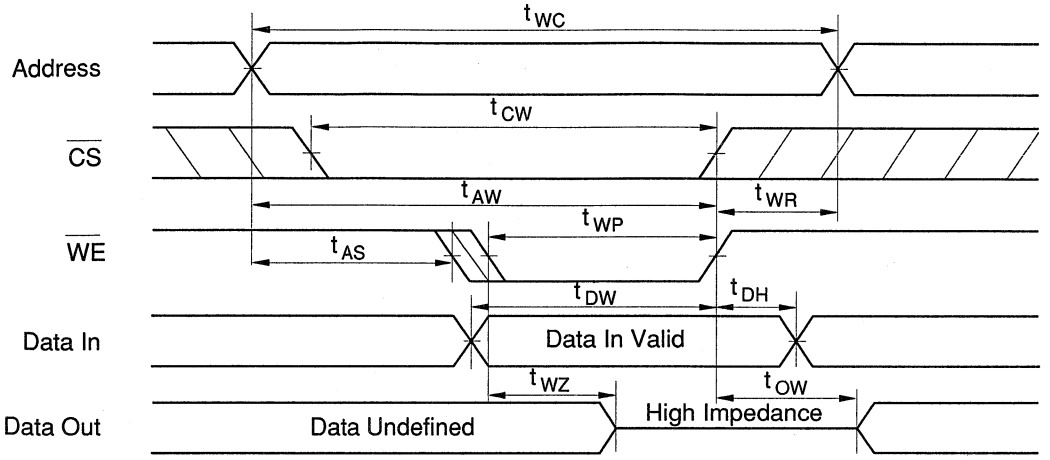
Notes : 1. $\overline{WE}$ is high and $\overline{CS}$ is low for read cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.

Read Cycle (–2)*1, *2, *3



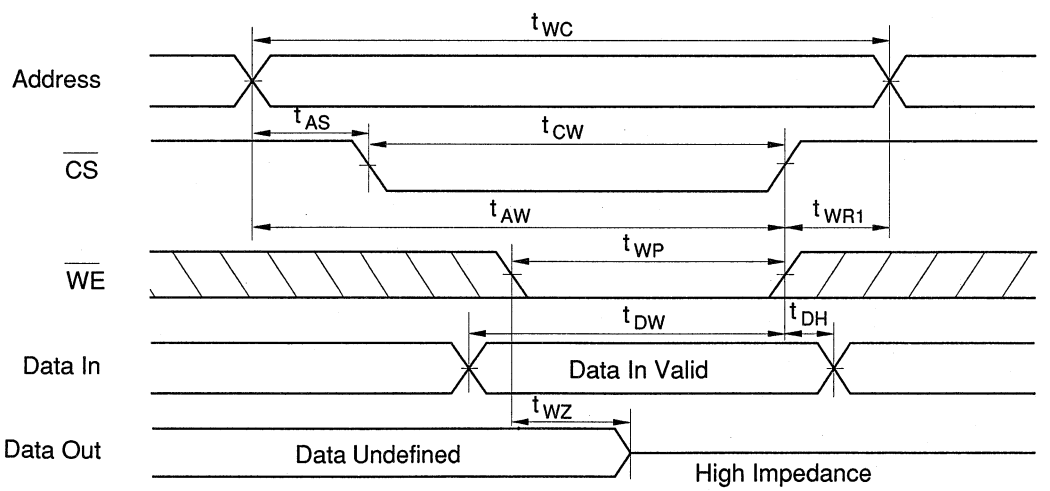
Notes : 1. $\overline{WE}$ is high and $\overline{CS}$ is low for read cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is meaured ± 200 mV from steady state voltage with specified loading in Load(B).

Write Cycle (–1)[*1] ($\overline{WE}$ Controlled)



Note : 1. Transition is measured ± 200 mV from steady state voltage with specified loading in Load(B).

Write Cycle (–2)[*1] ($\overline{CS}$ Controlled)



Note : 1. Transition is measured ± 200 mV from steady state voltage with specified loading in Load(B).

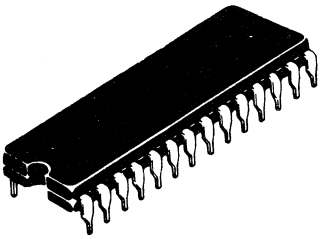
HM62256 Series

32768-word x 8-bit High Speed CMOS Static RAM

■ FEATURES

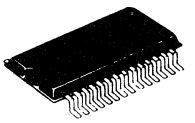
- High Speed: Fast Access Time 85/100/120/150ns (max.)
- Low Power Standby and Low Power Operation;
  Standby: 200μW (typ)/10μW (typ) (L-/L-SL version),
  Operation: 40mW (typ.) (f = 1MHz)
- Single 5V Supply
- Completely Static RAM: No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three-state Output
- Directly TTL Compatible: All Input and Output
- Capability of Battery Back Up Operation (L-/L-SL version)

HM62256P Series



(DP-28)

HM62256FP Series

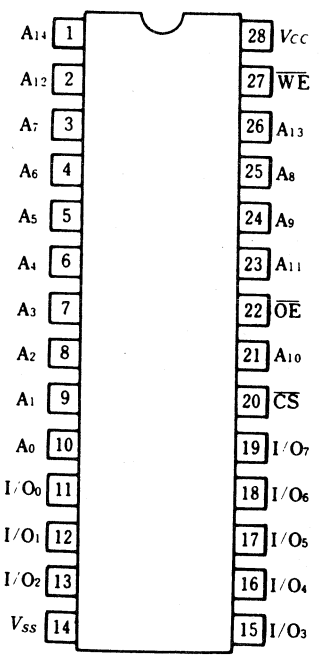


(FP-28DA)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM62256P-8	85ns	600 mil 28 pin Plastic DIP
HM62256P-10	100ns	
HM62256P-12	120ns	
HM62256P-15	150ns	
HM62256LP-8	85ns	
HM62256LP-10	100ns	
HM62256LP-12	120ns	
HM62256LP-15	150ns	
HM62256LP-10SL	100ns	
HM62256LP-12SL	120ns	
HM62256LP-15SL	150ns	
HM62256FP-8T	85ns	28 pin Plastic SOP
HM62256FP-10T	100ns	
HM62256FP-12T	120ns	
HM62256FP-15T	150ns	
HM62256LFP-8T	85ns	
HM62256LFP-10T	100ns	
HM62256LFP-12T	120ns	
HM62256LFP-15T	150ns	
HM62256LFP-10SLT	100ns	
HM62256LFP-12SLT	120ns	
HM62256LFP-15SLT	150ns	

■ PIN ARRANGEMENT



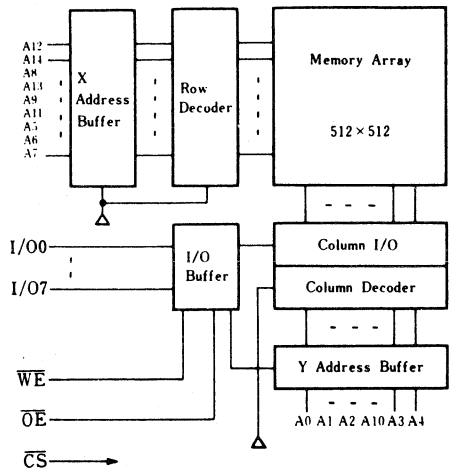
(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on any pin with relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

Note) *1. −3.0V for pulse width ≦ 50ns

■ BLOCK DIAGRAM



■ TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	X	X	Not Selected	I_{SB}, I_{SB1}	High Z	–
L	L	H	Read	I_{CC}	Dout	Read Cycle No. 1~3
L	H	L	Write	I_{CC}	Din	Write Cycle No. 1
L	L	L	Write	I_{CC}	Din	Write Cycle No. 2

X means H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 50ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item		Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current		$\|I_{LI}\|$	$V_{IN} = V_{SS}$ to V_{CC}	–	–	2	μA
Output Leakage Current		$\|I_{LO}\|$	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, $V_{I/O}=V_{SS}$ to V_{CC}	–	–	2	μA
Operating Power Supply Current		I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA	–	8	15	mA
Average Operating Power Supply Current	HM62256-8	I_{CC1}	Min. Cycle, duty=100%, $\overline{CS}=V_{IL}$, $I_{I/O}$=0mA	–	50	70	mA
	HM62256-10			–	40	70	
	HM62256-12			–	35	70	
	HM62256-15			–	33	70	
		I_{CC2}	$\overline{CS}=V_{IL}$, $V_{IH}=V_{CC}$, V_{IL}=0V, $I_{I/O}$=0mA, f=1MHZ	–	8	15	mA
Standby Power Supply Current		I_{SB}	$\overline{CS}=V_{IH}$	–	0.5	3	mA
		I_{SB1}	$\overline{CS} \geqq V_{CC}-0.2V$, $0V \leqq V_{IN}$	–	0.04	2	mA
				–	2*2	100*2	μA
				–	2*3	50*3	
Output Voltage		V_{OL}	I_{OL}=2.1mA	–	–	0.4	V
		V_{OH}	I_{OH}=−1.0mA	2.4	–	–	V

Notes) *1. Typical values are at V_{CC}=5.0V, T_a= 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.
*3. This characteristics is guaranteed only for L-SL version.

■ CAPACITANCE (T_a=25°C, f=1MHz)

Item	Symbol	Test Condition	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	8	pF

Note) This parameter is sampled and not 100% tested.

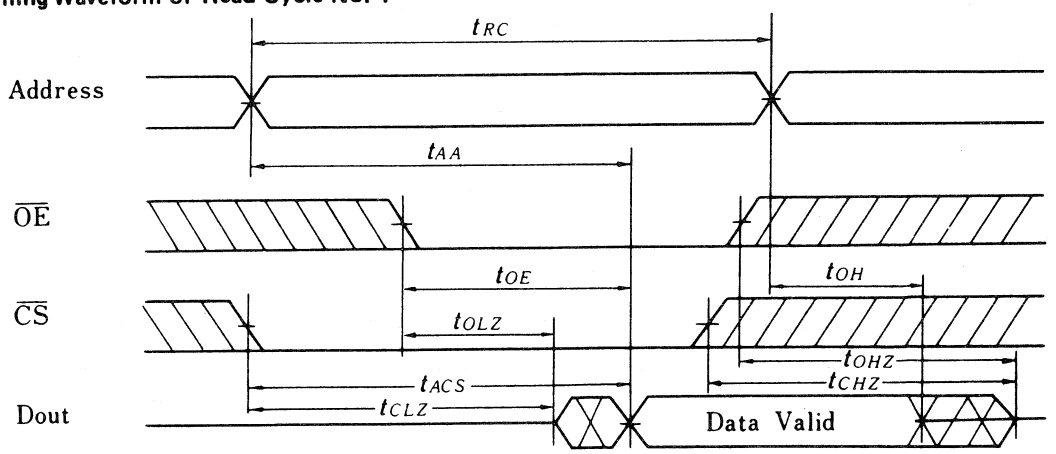
■ AC CHARACTERISTICS (V_{CC}=5V± 10%, T_a=0 to +70°C unless otherwise noted)

- **AC Test Conditions**
  - ○ Input pulse levels: 0.8V to 2.4V
  - ○ Input rise and fall times: 5ns
  - ○ Input and Output timing reference levels: 1.5V
  - ○ Output load: 1TTL Gate and C_L (100pF) (Including scope and jig)

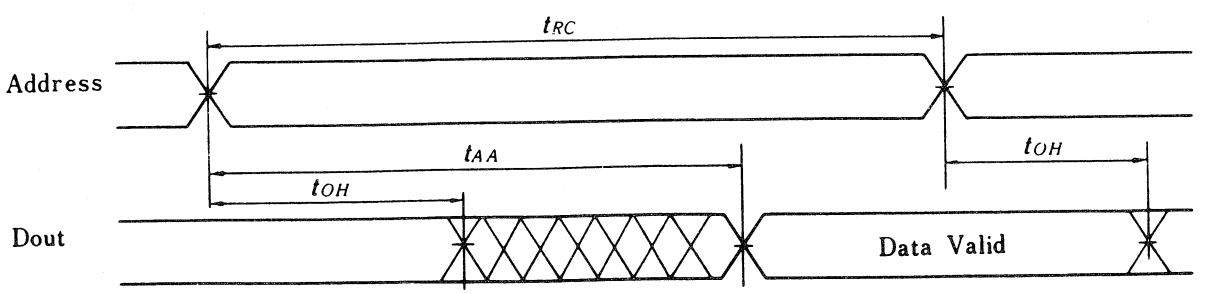
- **Read Cycle**

Item	Symbol	HM62256-8		HM62256-10		HM62256-12		HM62256-15		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	85	–	100	–	120	–	150	–	ns
Address Access Time	t_{AA}	–	85	–	100	–	120	–	150	ns
Chip Select Access Time	t_{ACS}	–	85	–	100	–	120	–	150	ns
Output Enable to Output Valid	t_{OE}	–	45	–	50	–	60	–	70	ns
Output Hold from Address Change	t_{OH}	5	–	10	–	10	–	10	–	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	–	10	–	10	–	10	–	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	30	0	35	0	40	0	50	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns

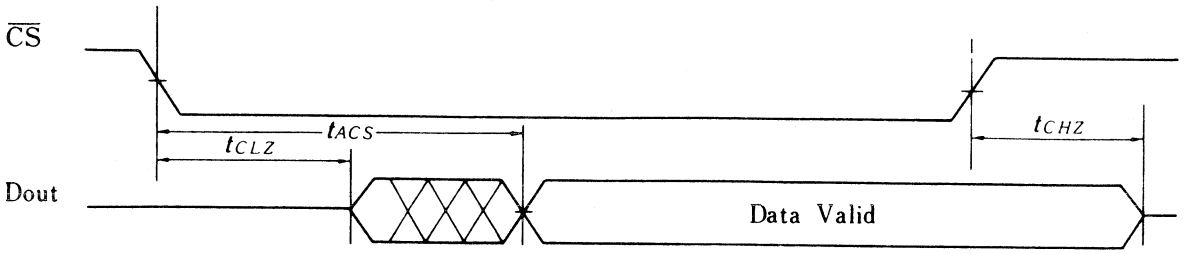
- **Timing Waveform of Read Cycle No. 1[1]**



- **Timing Waveform of Read Cycle No. 2[1][2][4]**



- **Timing Waveform of Read Cycle No. 3[1][3][4]**

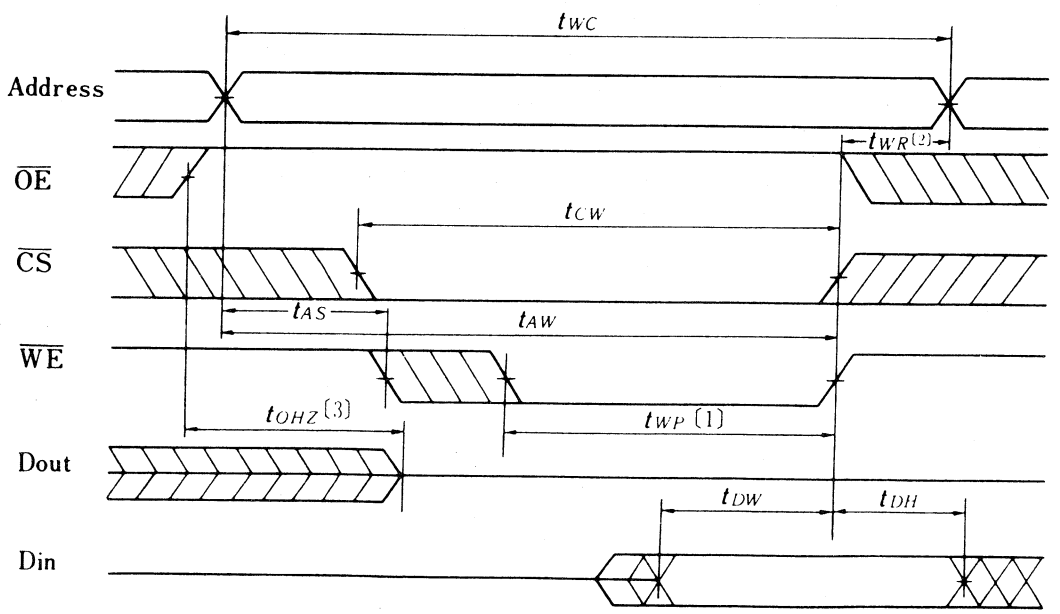


Notes) 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE} = V_{IL}$.

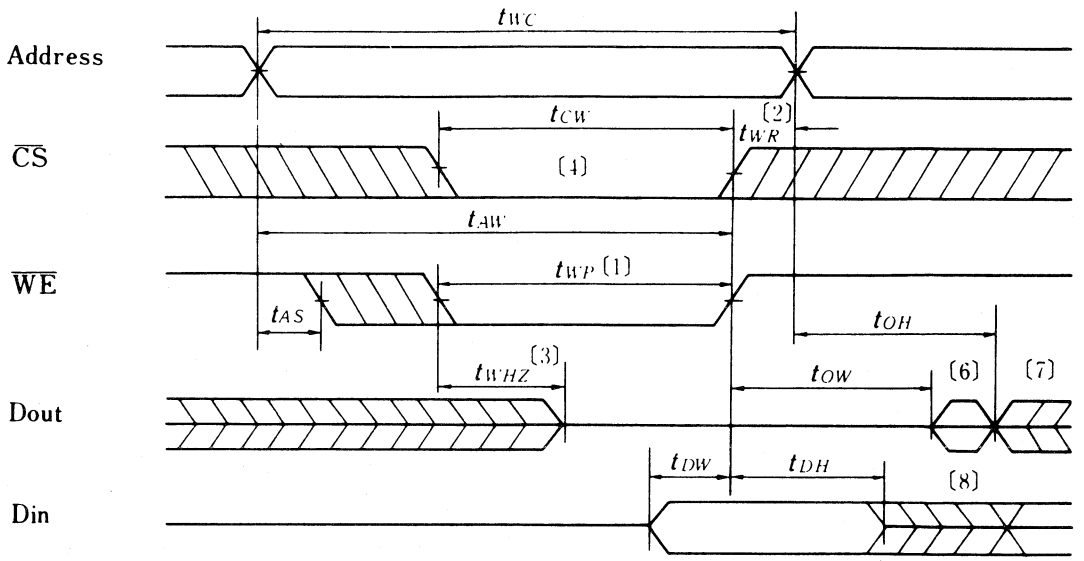
- **Write Cycle**

Item	Symbol	HM62256-8		HM62256-10		HM62256-12		HM62256-15		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Write Cycle Time	t_{WC}	85	–	100	–	120	–	150	–	ns
Chip Selection to End of Write	t_{CW}	75	–	80	–	85	–	100	–	ns
Address Valid to End of Write	t_{AW}	75	–	80	–	85	–	100	–	ns
Address Set Up Time	t_{AS}	0	–	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	60	–	60	–	70	–	90	–	ns
Write Recovery Time	t_{WR}	10	–	0	–	0	–	0	–	ns
Write to Output in High Z	t_{WHZ}	0	30	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	–	40	–	50	–	60	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	0	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	5	–	ns

- **Timing Waveform of Write Cycle No. 1 ($\overline{OE}$ Clock)**



- **Timing Waveform of Write Cycle No. 2[5] ($\overline{OE}$ Low Fixed)**



Notes: 1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state. The input signals out of phase must not be applied
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. Dout is in the same phase of written data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The input signals out of phase must not be applied to I/O Pins.

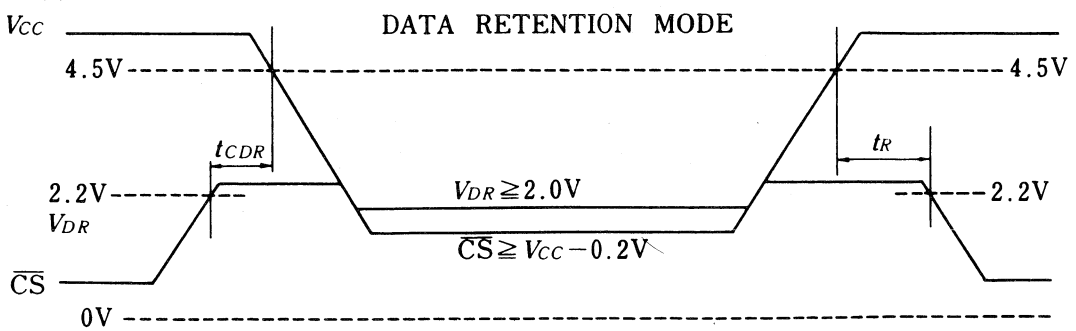
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

(This characteristics is guaranteed only for L-and L-SL version)

Item	Symbol	Test Conditions	min.	typ.	max.	Unit
V_{CC} for Date Retention	V_{DR}	$\overline{CS} \geqq V_{CC}$ –0.2V	2.0	–	–	V
Data Retention Current	I_{CCDR}	V_{CC} = 3.0V, $\overline{CS} \geqq$ 2.8V 0V ≦ V_{in}	–	–	50*2	μA
			–	–	10*3	
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}*1	–	–	ns

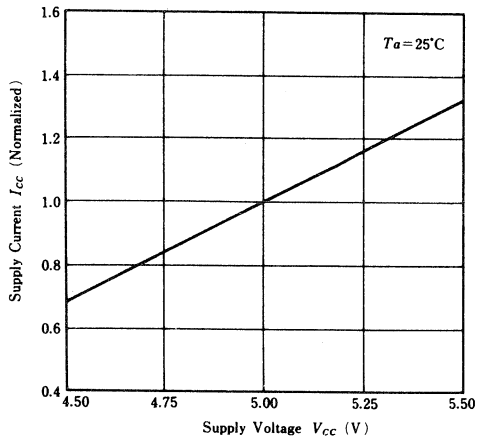
Note) *1. t_{RC} = Read Cycle Time
*2. This characteristic is guaranteed only for L-version, 20μA max. at T_a = 0 to 40°C.
*3. This characteristic is guaranteed only for L-SL version, 3μA max. at T_a = 0 to 40°C.

- **Low V_{CC} Data Retention Waveform**

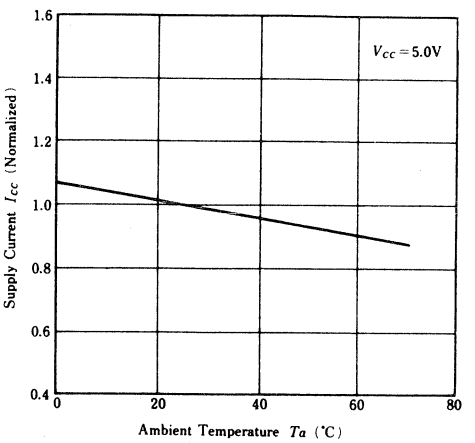


Note) In Data Retention Mode, $\overline{CS}$ controls the Address, $\overline{WE}$, $\overline{OE}$, and Din Buffers. *Vin* for these inputs can be in high impedance state in data retention mode.

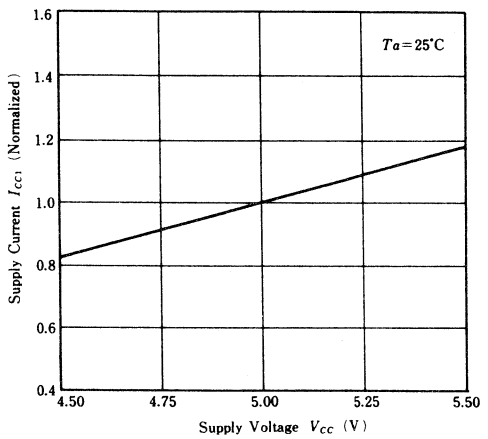
SUPPLY CURRENT vs. SUPPLY VOLTAGE (1)



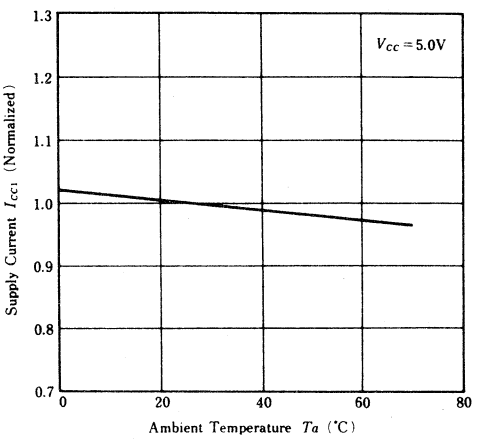
SUPPLY CURRENT vs. AMBIENT TEMPERATURE (1)



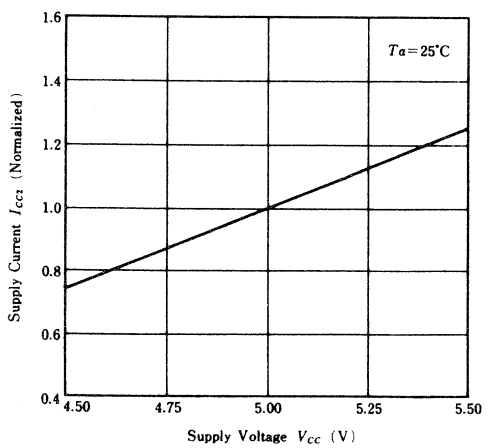
SUPPLY CURRENT vs. SUPPLY VOLTAGE (2)



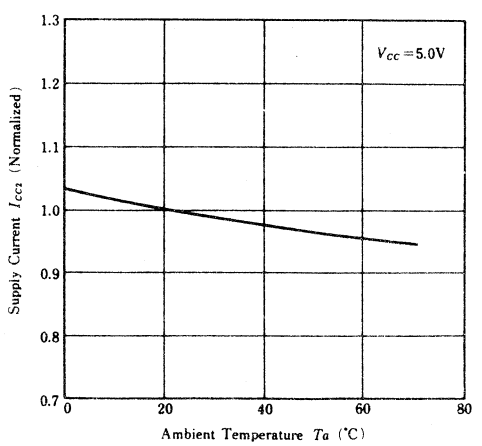
SUPPLY CURRENT vs. AMBIENT TEMPERATURE (2)



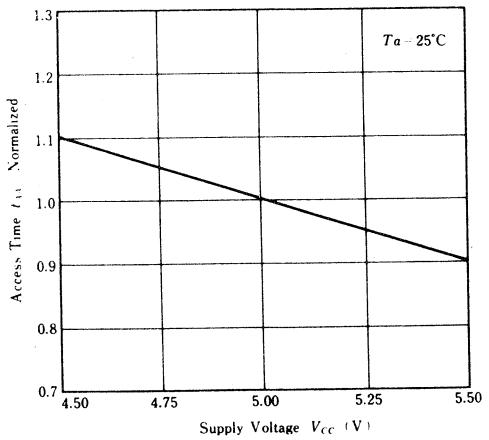
SUPPLY CURRENT vs. SUPPLY VOLTAGE (3)



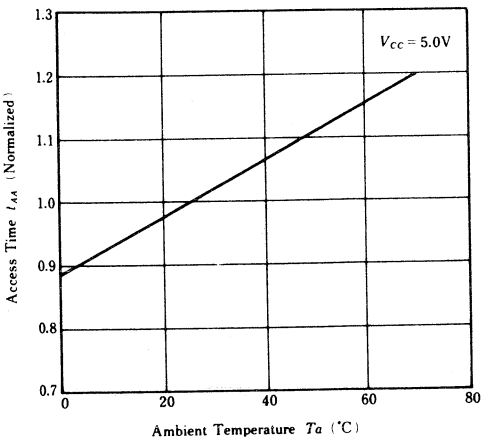
SUPPLY CURRENT vs. AMBIENT TEMPERATURE (3)



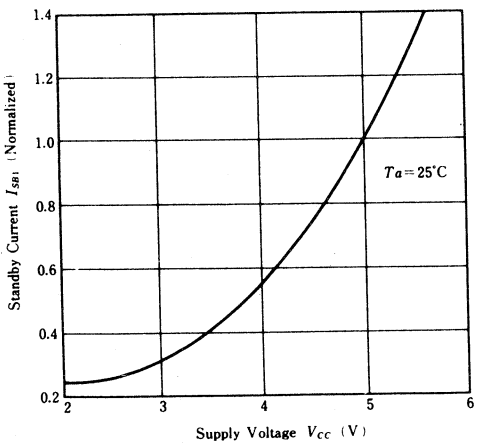
ACCESS TIME vs. SUPPLY VOLTAGE



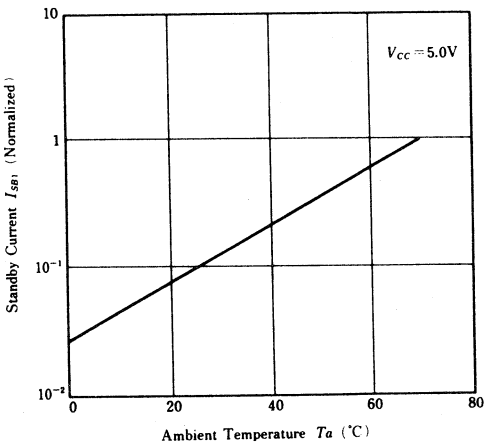
ACCESS TIME vs. AMBIENT TEMPERATURE



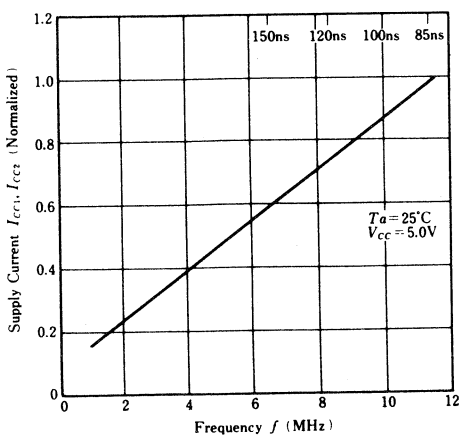
STANDBY CURRENT vs. SUPPLY VOLTAGE



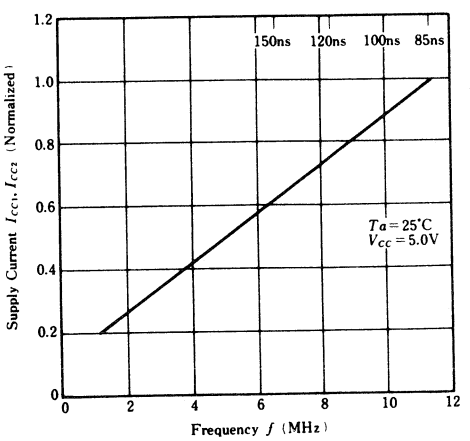
STANDBY CURRENT vs. AMBIENT TEMPERATURE



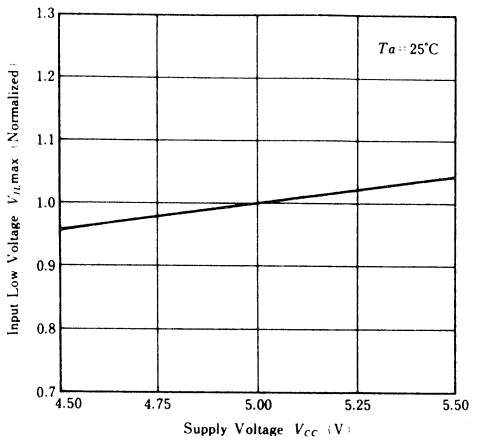
SUPPLY CURRENT vs. FREQUENCY (READ)



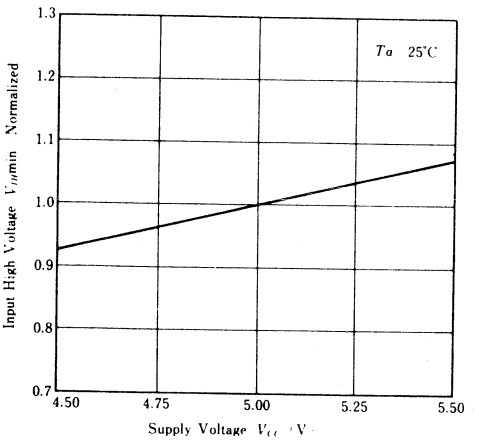
SUPPLY CURRENT vs. FREQUENCY (WRITE)



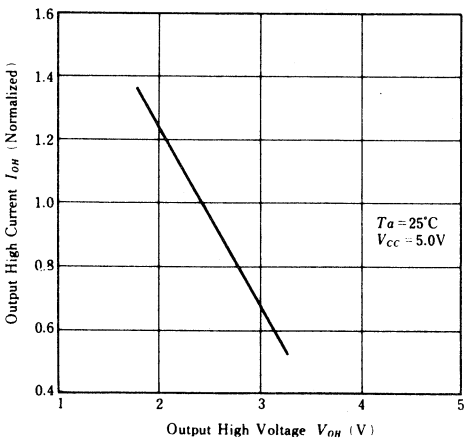
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



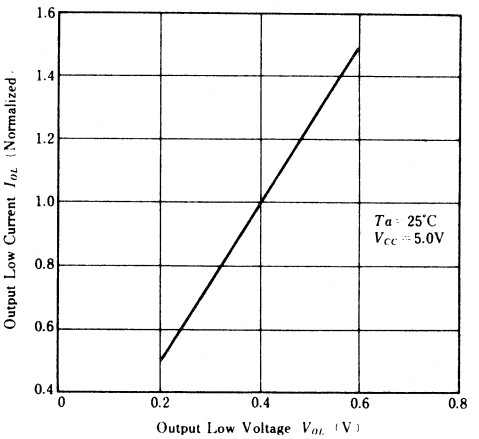
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



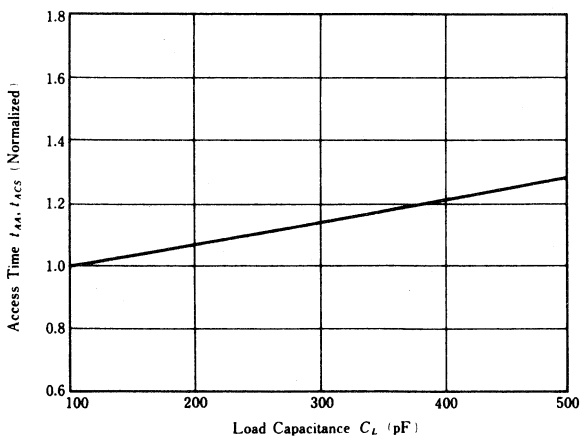
OUTPUT CURRENT vs. OUTPUT VOLTAGE



OUTPUT CURRENT vs. OUTPUT VOLTAGE



ACCESS TIME vs. LOAD CAPACITANCE



HM62256A Series

32,768-word × 8-bit High Speed CMOS Static RAM

The Hitachi HM62256A is a CMOS static RAM organized 32-kword × 8-bit. It realizes higher performance and low power consumption by employing 0.8 μm Hi-CMOS process technology. The device, packaged in a 8 × 14 mm TSOP with thickness of 1.2 mm, 450-mil SOP (foot print pitch width), 600-mil plastic DIP, or 300-mil plastic DIP, is available for high density mounting. TSOP package is suitable for cards, and reverse type TSOP is also provided. It offers low power standby power dissipation; therefore, it is suitable for battery back up system.

Features

- High speed: Fast Access time 85/100/120/150 ns (max)
- Low Power
  Standby: 5 μW (typ) (L/L-SL version)
  Operation: 40 mW (typ) (f = 1 MHz)
- Single 5 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation

Ordering Information

Type No.	Access time	Package
HM62256AP-8	85 ns	600-mil 28-pin plastic DIP (DP-28)
HM62256AP-10	100 ns	
HM62256AP-12	120 ns	
HM62256AP-15	150 ns	
HM62256ALP-8	85 ns	
HM62256ALP-10	100 ns	
HM62256ALP-12	120 ns	
HM62256ALP-15	150 ns	
HM62256ALP-8SL	85 ns	
HM62256ALP-10SL	100 ns	
HM62256ALP-12SL	120 ns	
HM62256ALP-15SL	150 ns	
HM62256ASP-8	85 ns	300-mil 28-pin plastic DIP (DP-28NA)
HM62256ASP-10	100 ns	
HM62256ASP-12	120 ns	
HM62256ASP-15	150 ns	
HM62256ALSP-8	85 ns	
HM62256ALSP-10	100 ns	
HM62256ALSP-12	120 ns	
HM62256ALSP-15	150 ns	
HM62256ALSP-8SL	85 ns	
HM62256ALSP-10SL	100 ns	
HM62256ALSP-12SL	120 ns	
HM62256ALSP-15SL	150 ns	
HM62256AFP-8T	85 ns	450-mil 28-pin plastic SOP (FP-28DA)
HM62256AFP-10T	100 ns	
HM62256AFP-12T	120 ns	
HM62256AFP-15T	150 ns	
HM62256ALFP-8T	85 ns	
HM62256ALFP-10T	100 ns	
HM62256ALFP-12T	120 ns	
HM62256ALFP-15T	150 ns	
HM62256ALFP-8SLT	85 ns	
HM62256ALFP-10SLT	100 ns	
HM62256ALFP-12SLT	120 ns	
HM62256ALFP-15SLT	150 ns	

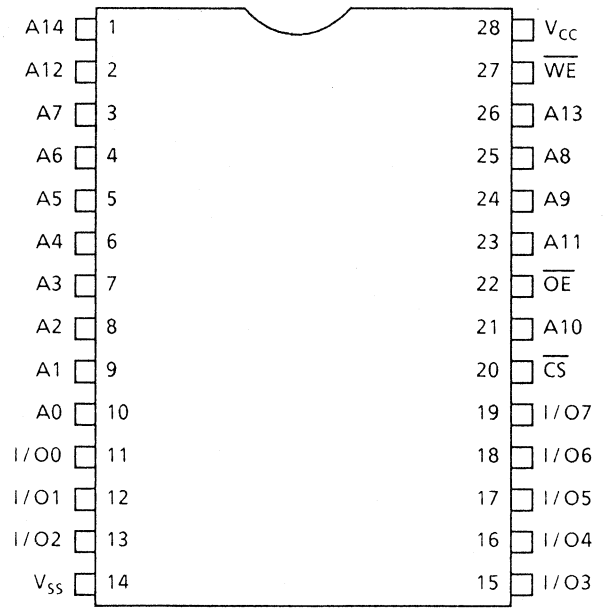
TSOP Series

Type No.	Access time	Package
HM62256ALT-8	85 ns	8 mm × 14 mm
HM62256ALT-10	100 ns	32-pin TSOP
HM62256ALT-12	120 ns	(normal type)
HM62256ALT-15	150 ns	(TFP-32DA)
HM62256ALT-8SL	85 ns	
HM62256ALT-10SL	100 ns	
HM62256ALT-12SL	120 ns	
HM62256ALT-15SL	150 ns	

Type No.	Access time	Package
HM62256ALR-8	85 ns	8 mm × 14 mm
HM62256ALR-10	100 ns	32-pin TSOP
HM62256ALR-12	120 ns	(reverse type)
HM62256ALR-15	150 ns	(TFP-32DAR)
HM62256ALR-8SL	85 ns	
HM62256ALR-10SL	100 ns	
HM62256ALR-12SL	120 ns	
HM62256ALR-15SL	150 ns	

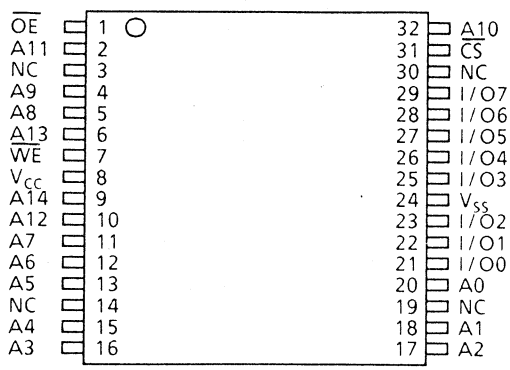
Pin Arrangement

HM62256AP/AFP/ASP Series



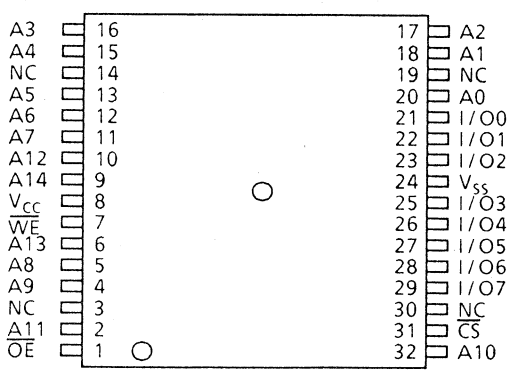
(Top View)

HM62256AT Series



(Top View)

HM62256AR Series

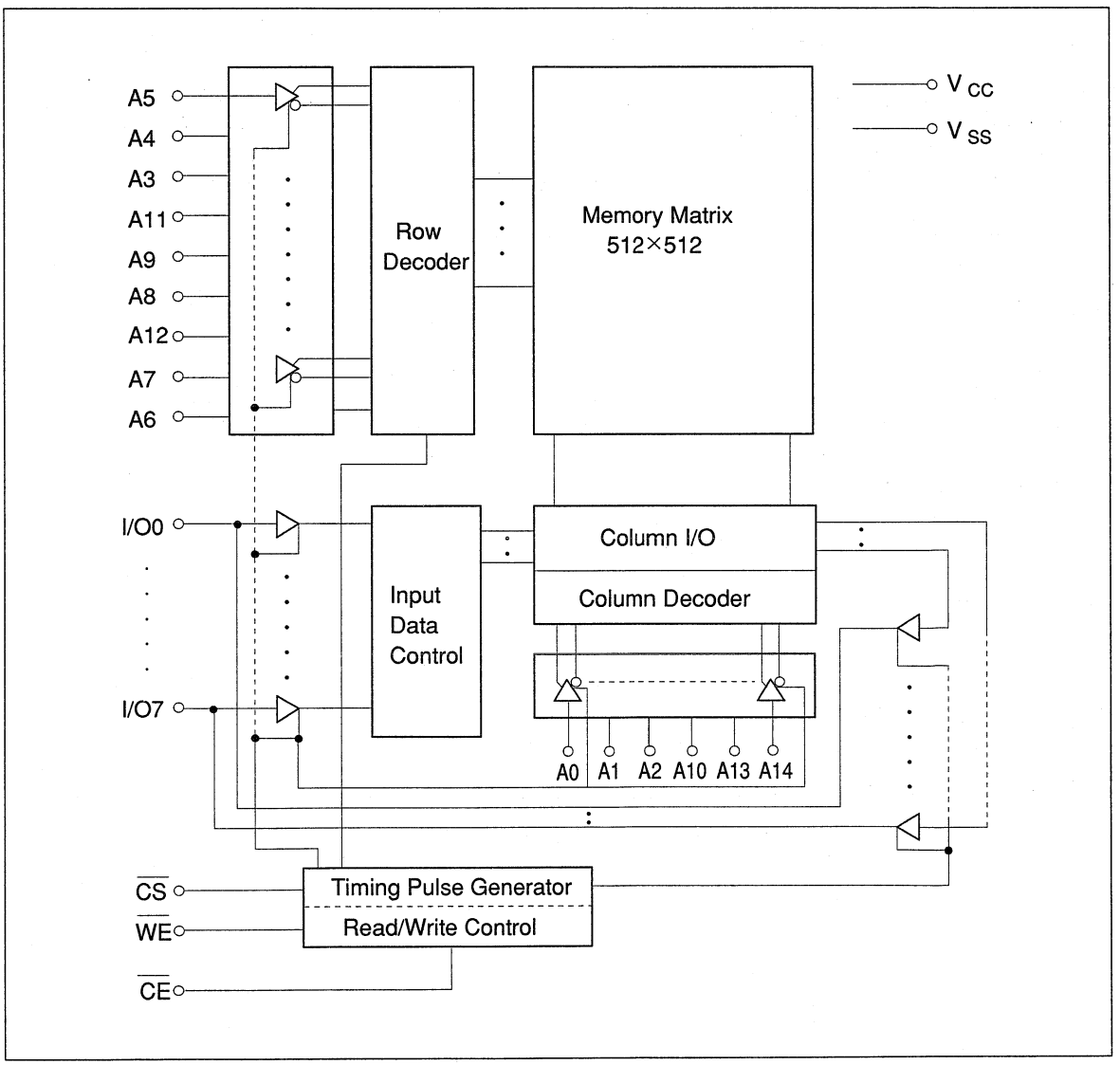


(Top View)

Pin Description

Symbol	Function	Symbol	Function
A0 – A14	Address	$\overline{OE}$	Output enable
I/O0 – I/O7	Input/output	NC	No connection
$\overline{CS}$	Chip select	V_{CC}	Power supply
$\overline{WE}$	Write enable	V_{SS}	Ground

Block Diagram



Function Table

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
X	H	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
H	L	H	Output disable	I_{CC}	High-Z	—
H	L	L	Read	I_{CC}	Dout	Read cycle (1)–(3)
L	L	H	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: X: H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5[*1] to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to + 70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Note: 1. V_T min = −3.0 V for pulse half-width ≤ 50 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	−0.5[*1]	—	0.8	V

Note: 1. V_{IL} min = −3.0 V for pulse half-width ≤ 50 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min	Typ*1	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	1	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating V_{CC} current	I_{CC}	—	8	15	mA	$\overline{CS}$ = V_{IL}, others = V_{IH}/V_{IL} Iout = 0 mA
	I_{CC1}	—	40	70	mA	min cycle, duty = 100%, $I_{I/O}$ = 0 mA $\overline{CS}$ = V_{IL}, others = V_{IH}/V_{IL}
	I_{CC2}	—	8	15	mA	Cycle time = 1µs, $I_{I/O}$ = 0 mA $\overline{CS}$ = V_{IL}, V_{IH} = V_{CC}, V_{IL} = 0
Standby V_{CC} current	I_{SB}	—	0.5	3	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}	—	0.02	2	mA	Vin ≥ 0 V $\overline{CS}$ ≥ V_{CC} –0.2 V
		—	1*2	100*2	µA	
		—	1*3	50*3	µA	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –1.0 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and not guaranteed.
2. This characteristics is guaranteed only for L-version.
3. This characteristics is guaranteed only for L-SL version.

Capacitance (Ta = 25°C, f = 1 MHz)*1

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	8	pF	$V_{I/O}$= 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

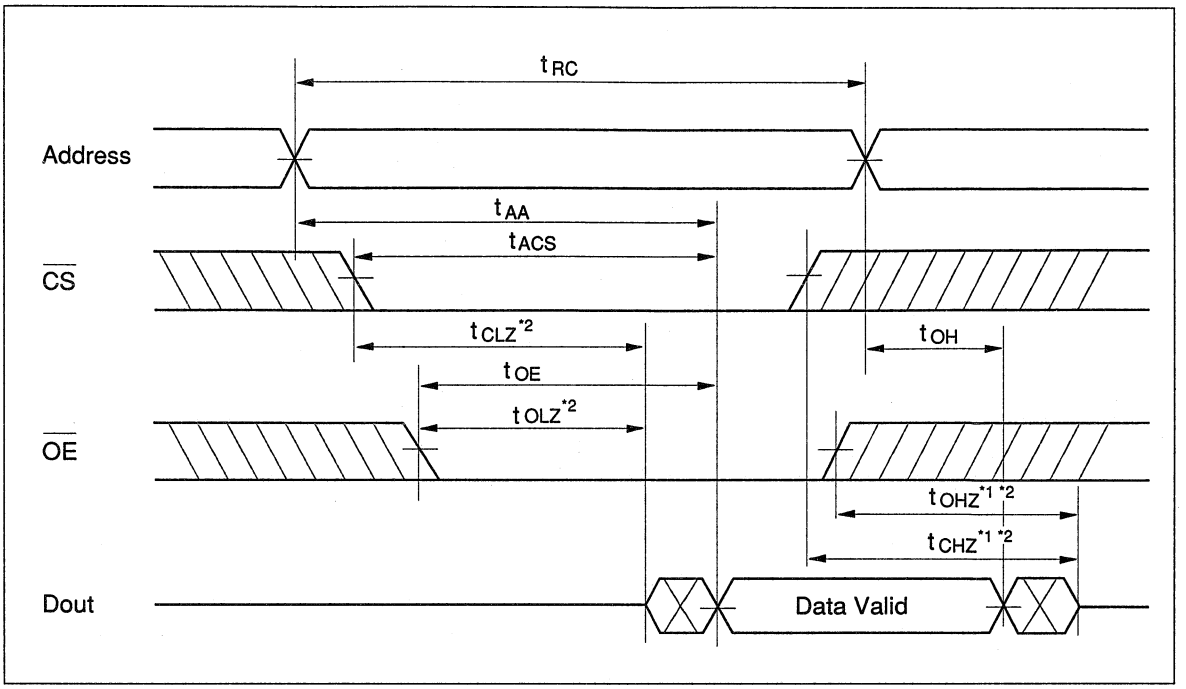
Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input and output timing refernce levels: 1.5 V
- Input rise and fall times: 5 ns
- Output load: 1 TTL Gate + C_L (100 pF) (Including scope & jig)

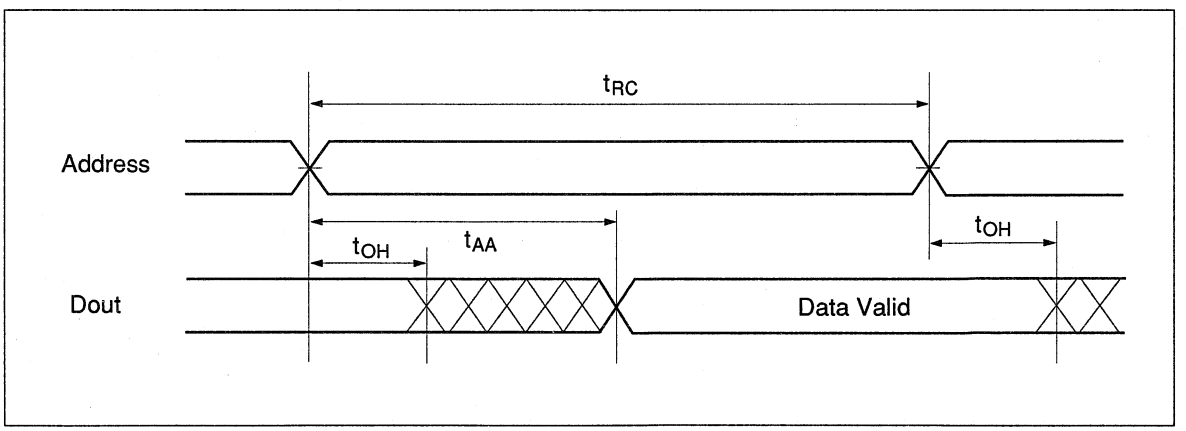
Read Cycle

		HM62256A-8		HM62256A-10		HM62256A-12		HM62256A-15			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	85	—	100	—	120	—	150	—	ns	
Address access time	t_{AA}	—	85	—	100	—	120	—	150	ns	
Chip select access time	t_{ACS}	—	85	—	100	—	120	—	150	ns	
Output enable to output valid	t_{OE}	—	45	—	50	—	60	—	70	ns	
Chip selection to output in low-Z	t_{CLZ}	10	—	10	—	10	—	10	—	ns	2
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	5	—	5	—	ns	2
Chip deselection to output in high-Z	t_{CHZ}	0	30	0	35	0	40	0	50	ns	1, 2
Output disable to output in high-Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns	1, 2
Output hold from address change	t_{OH}	5	—	10	—	10	—	10	—	ns	

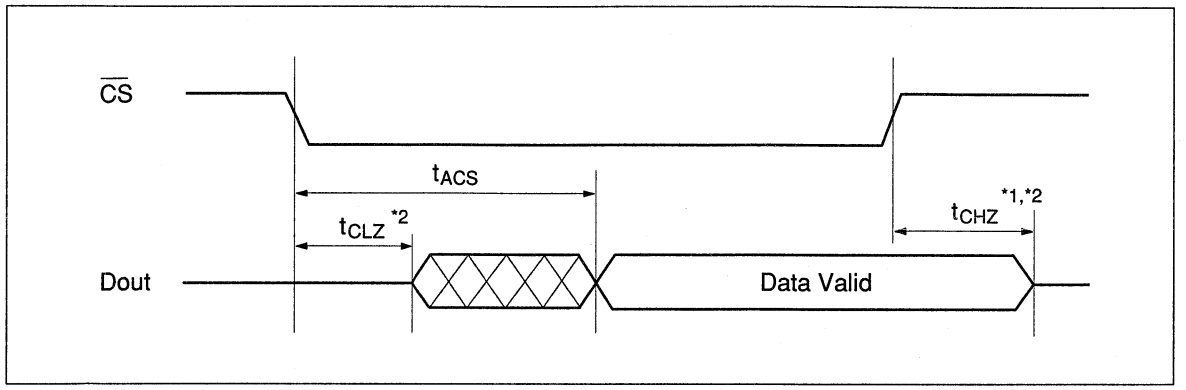
Read Timing Waveform (1) *3



Read Timing Waveform (2) *3 *4 *6



Read Timing Waveform (3) *3 *5 *6

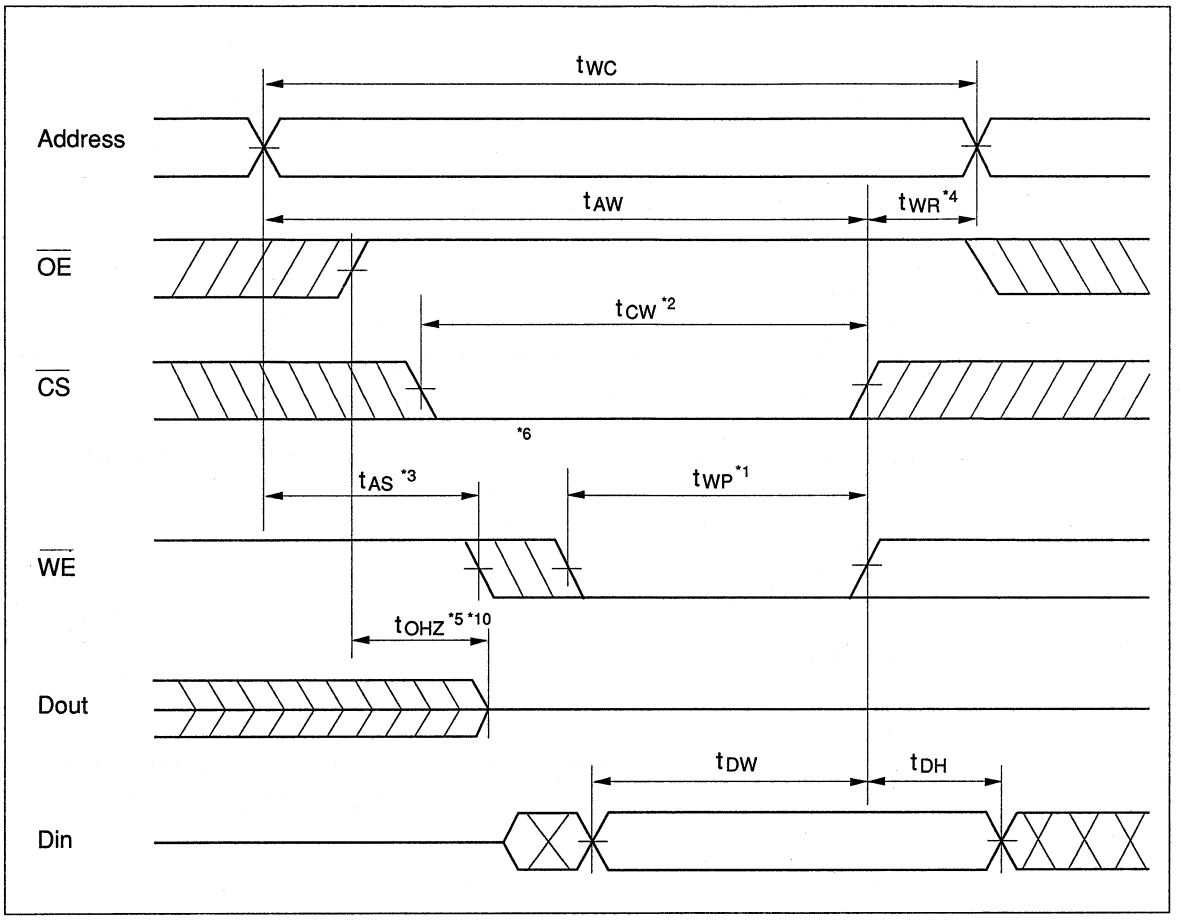


Notes:
1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. $\overline{WE}$ is high for read cycle.
4. Device is continuously selected, $\overline{CS} = V_{IL}$.
5. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
6. $\overline{OE} = V_{IL}$.

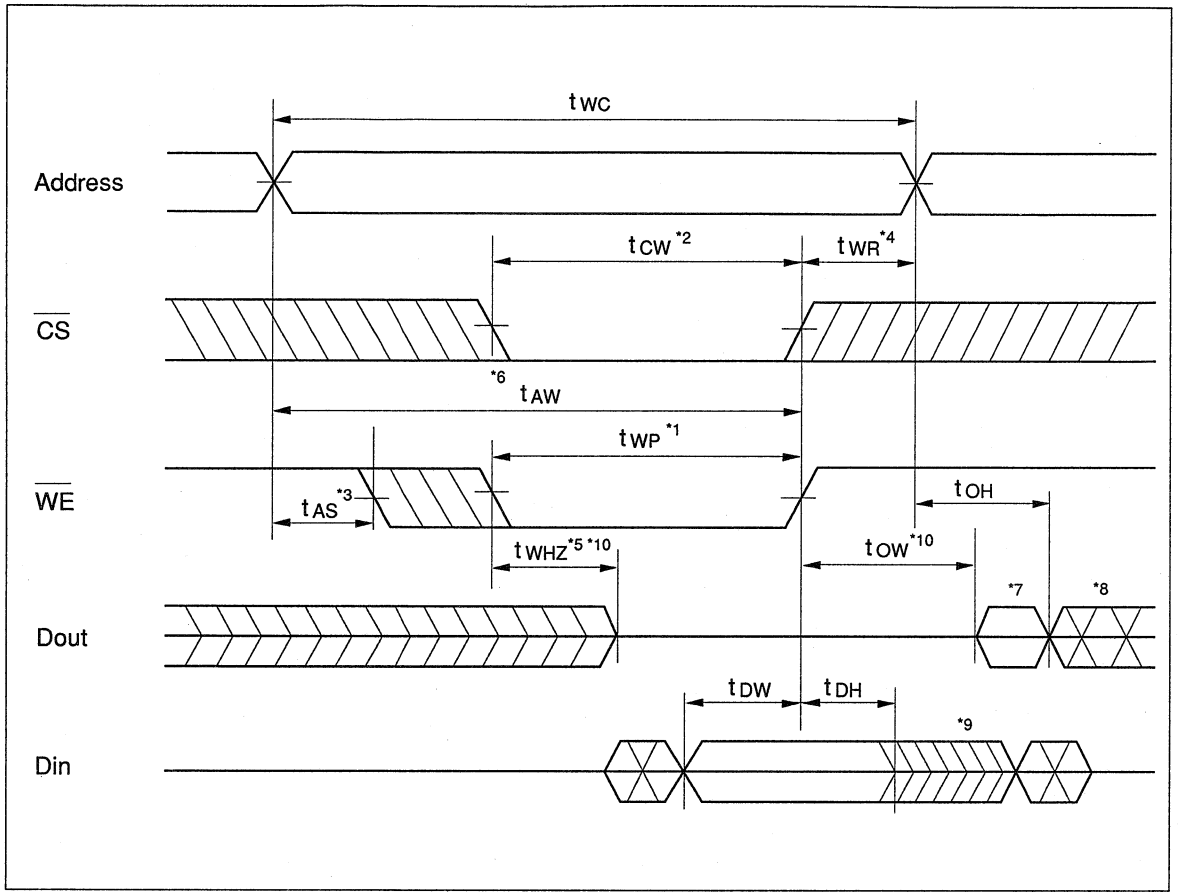
Write Cycle

		HM62256A-8		HM62256A-10		HM62256A-12		HM62256A-15			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Write cycle time	t_{WC}	85	—	100	—	120	—	150	—	ns	
Chip selection to end of write	t_{CW}	75	—	80	—	85	—	100	—	ns	2
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns	3
Address valid to end of write	t_{AW}	75	—	80	—	85	—	100	—	ns	
Write pulse width	t_{WP}	55	—	60	—	70	—	90	—	ns	1
Write recovery time	t_{WR}	0	—	0	—	0	—	0	—	ns	4
$\overline{WE}$ to output in high-Z	t_{WHZ}	0	30	0	35	0	40	0	50	ns	10
Data to write time overlap	t_{DW}	40	—	40	—	50	—	60	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	5	—	5	—	ns	10
Output disable to output in high-Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns	10, 11

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Write Timing Waveform (2) ($\overline{OE}$ Low Fixed)



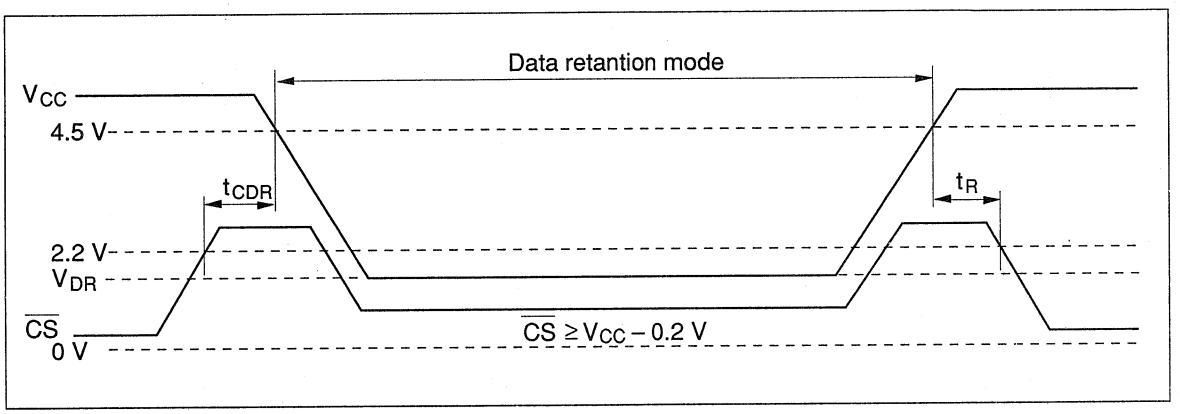
Notes:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CS}$ going low or $\overline{WE}$ going low. A write ends at the earlier transition of $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earlier of $\overline{WE}$ or $\overline{CS}$ going high to the end of write cycle.
5. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
6. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output remain in a high impedance state.
7. Dout is the same phase of the write data of this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the output must not be applied to them.
10. This parameter is sampled and not 100% tested.
11. t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L/L-SL version.

Item	Symbol	Min	Typ*1	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC}$ –0.2 V, Vin ≥ 0 V
Data retention current	I_{CCDR}	—	0.5	30*2	µA	V_{CC} = 3.0 V, Vin ≥ 0 V
		—	0.5	10*3	µA	$\overline{CS} \geq V_{CC}$ –0.2 V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*4	—	—	ns	

Low V_{CC} Data Retention Timing Waveform



Notes: 1. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and not guaranteed.
2. 20 µA max at Ta = 0 to +40°C. (only for L-version)
3. 3 µA max at Ta = 0 to +40°C. (only for L-SL version)
4. t_{RC} = read cycle time. (The transient time from V_{DR} to operating voltage must be more than 5 ms.) When this transient time is less than 5 ms, t_R must be 5 ms or more.
5. $\overline{CS}$ controls address buffer, $\overline{WE}$ buffer, $\overline{OE}$ buffer, and Din buffer. If $\overline{CS}$ controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

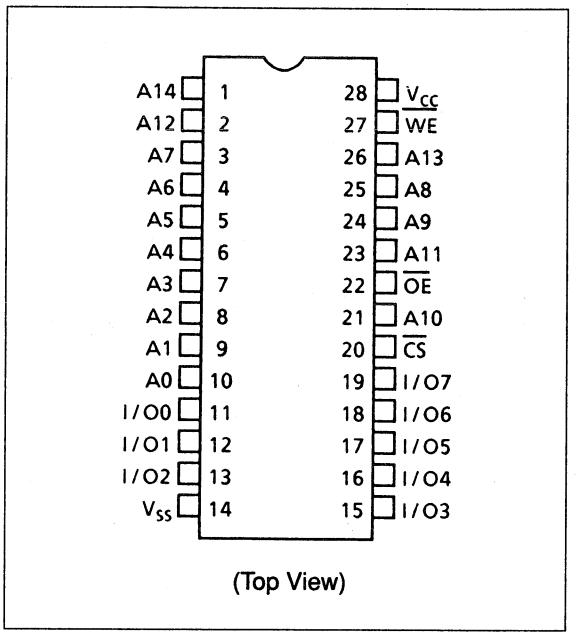
HM62832H Series

32768-Word × 8-Bit High Speed CMOS Static RAM

Features

- High speed: Fast access time 25/35/45 ns (max)
- Low power
  Active: 300 mW (typ)
  Standby: 10 µW (typ) (L-version)
- Single 5 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output – Three state output
- Directly TTL compatible – All inputs and outputs

Pin Arrangement



(Top View)

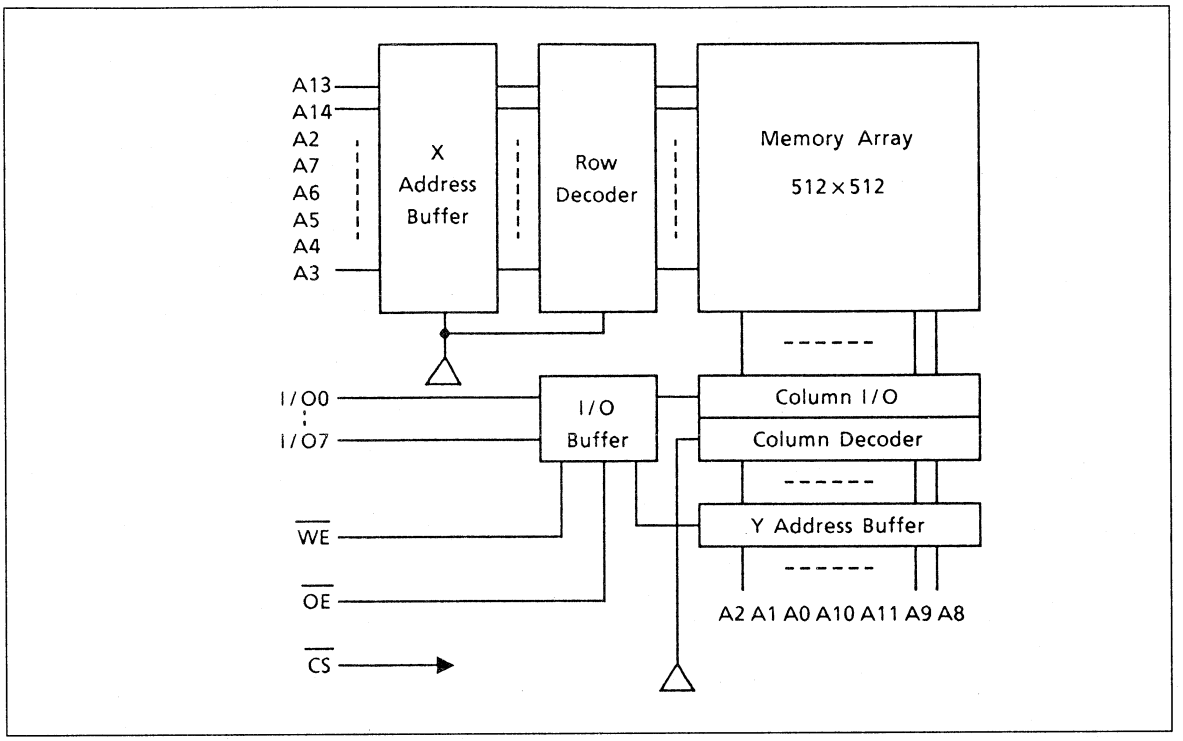
Ordering Information

Type No.	Access time	Package
HM62832HP–25	25 ns	300-mil 28-pin plastic DIP (DP-28NA)
HM62832HP–35	35 ns	
HM62832HP–45	45 ns	
HM62832HLP–25	25 ns	
HM62832HLP–35	35 ns	
HM62832HLP–45	45 ns	
HM62832HJP–25	25 ns	300-mil 28-pin plastic SOJ (CP-28DN)
HM62832HJP–35	35 ns	
HM62832HJP–45	45 ns	
HM62832HLJP–25	25 ns	
HM62832HLJP–35	35 ns	
HM62832HLJP–45	45 ns	

Pin Description

Pin name	Function
A0 – A14	Address
I/O0 – I/O7	Input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5 *1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Note: 1. −2.5 V for pulse width ≤ 10 ns

Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
H	X	X	Not selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read cycle (1) to (3)
L	H	L	Write	I_{CC}	Din	Write cycle (1)
L	L	L		I_{CC}	Din	Write cycle (2)

Note: 1. X: H or L

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	–0.5 *1	—	0.8	V

Note: 1. –2.0 V for pulse width ≤ 10 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions	Notes
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	Vin = V_{SS} to V_{CC}	
Output leakage current	$\|I_{LO}\|$	—	—	2	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	
Operating power supply current	I_{CC}	—	60	120	mA	Min cycle, duty = 100%, $\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA	
Standby power supply current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}	
Standby power supply current	I_{SB1}	—	0.02	2	mA	$\overline{CS}$ ≥ V_{CC} – 0.2 V, 0 V ≤ Vin ≤ 0.2 V or Vin ≥ V_{CC} – 0.2 V	
		—	0.002	0.1	mA		L-version
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA	
	V_{OH}	2.4	—	—	V	I_{OH} = –4 mA	

Note: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1.0 MHz)

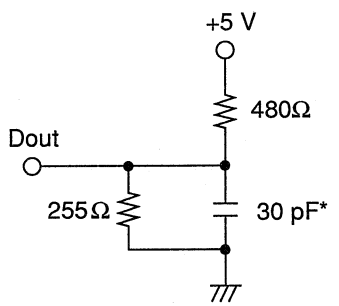
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

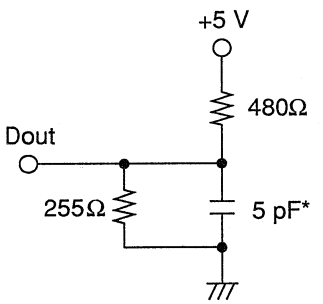
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.0 V to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures



Output load (A)



Output load (B)
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ} and t_{OW})

* Including scope and jig

Read Cycle

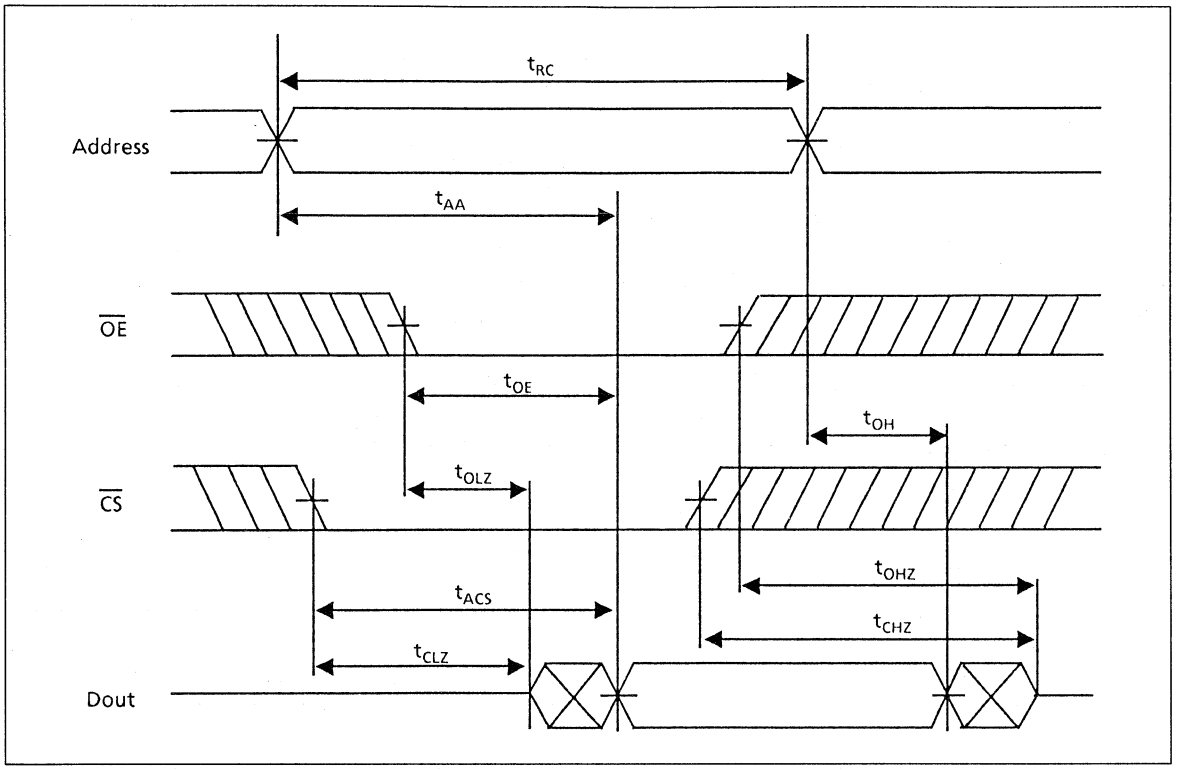
Parameter	Symbol	HM62832H–25		HM62832H–35		HM62832H–45		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	25	—	35	—	45	—	ns
Address access time	t_{AA}	—	25	—	35	—	45	ns
Chip select access time	t_{ACS}	—	25	—	35	—	45	ns
Output enable to output valid	t_{OE}	—	12	—	15	—	20	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip selection to output in low Z	t_{CLZ}	5	—	5	—	5	—	ns
Output enable to output in low Z	t_{OLZ}	0	—	0	—	0	—	ns
Chip deselection to output in high Z	t_{CHZ}	0	12	0	15	0	20	ns
Output enable to output in high Z	t_{OHZ}	0	12	0	15	0	20	ns

Write Cycle

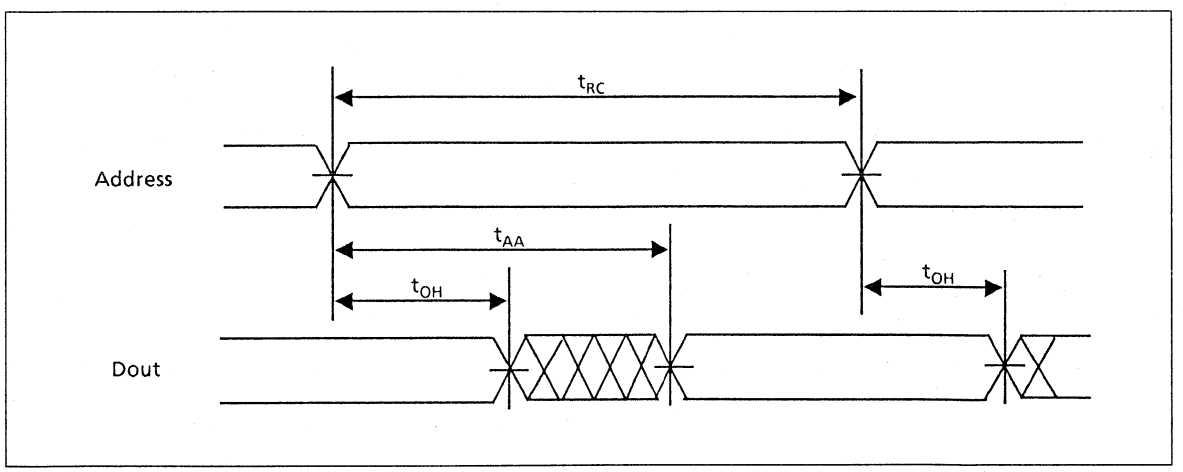
Parameter	Symbol	HM62832H–25		HM62832H–35		HM62832H–45		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	t_{WC}	25	—	35	—	45	—	ns
Chip selection to end of write	t_{CW}	15	—	20	—	25	—	ns
Address valid to end of write	t_{AW}	20	—	30	—	40	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	15	—	20	—	25	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Write to output in high Z	t_{WHZ}	0	12	0	15	0	20	ns
Data to write time overlap	t_{DW}	12	—	15	—	20	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Output disable to output in high Z	t_{OHZ}	0	12	0	15	0	20	ns
Output active from end of write	t_{OW}	5	—	5	—	5	—	ns

Timing Waveforms

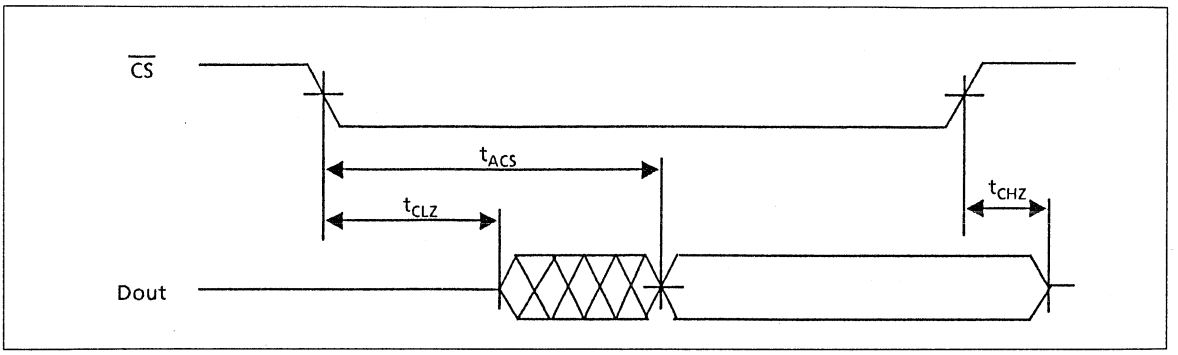
Read Cycle Timing–1*1, *2



Read Cycle Timing–2*2, *3, *5

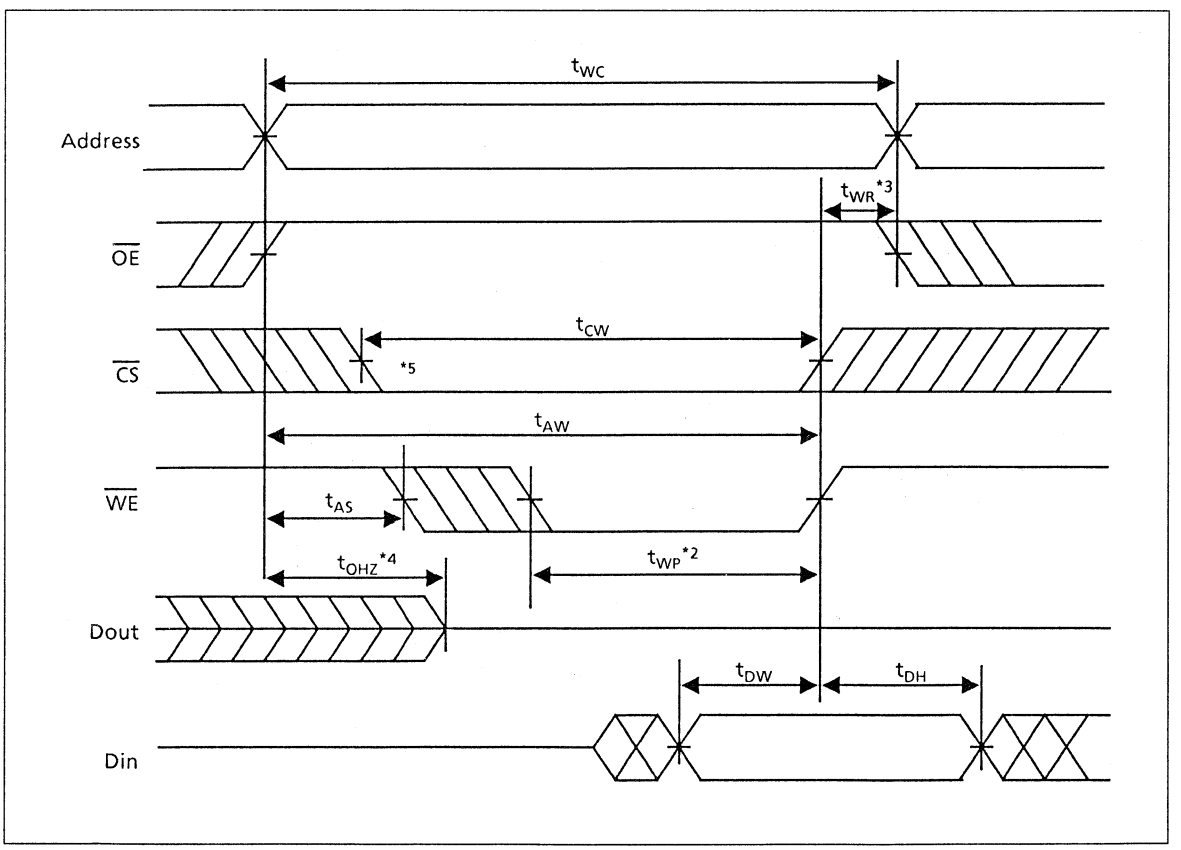


Read Cycle Timing–3*1, *2, *4, *5

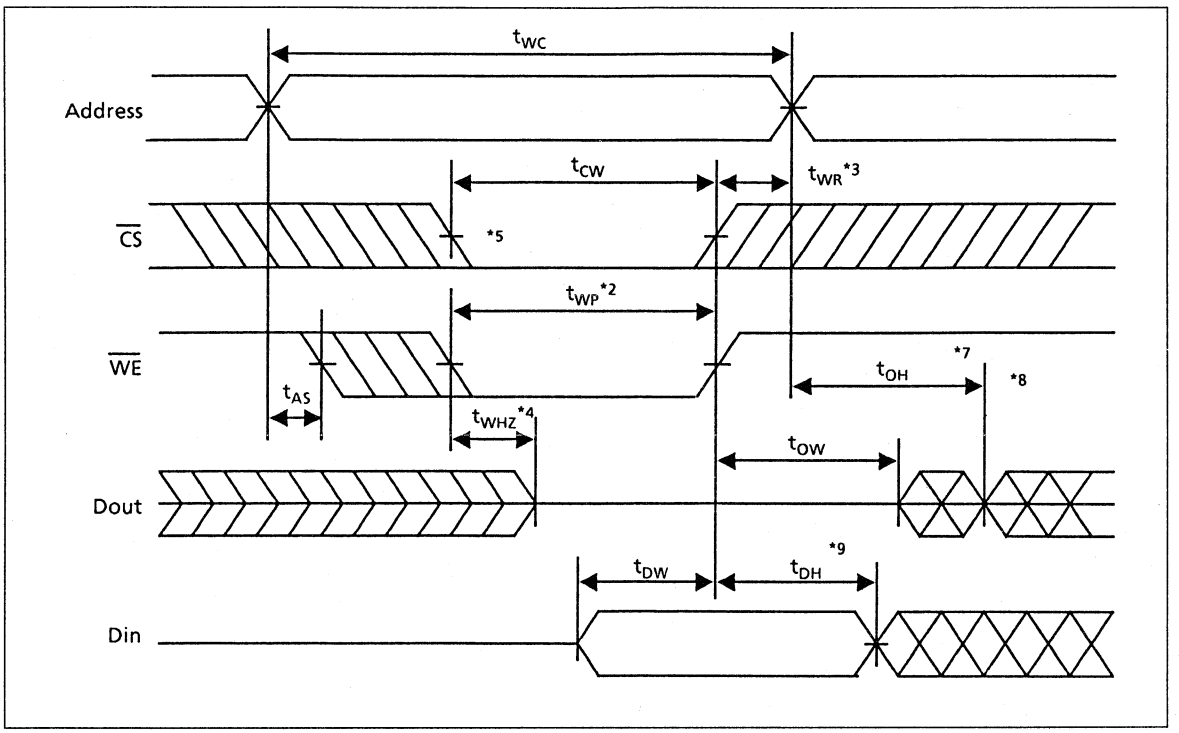


Notes: 1. Transition is measured ±200 mV from steady state voltage with load (B).
This parameter is sampled and not 100% tested.
2. $\overline{WE}$ is high for read cycle.
3. Device is continuously selected, $\overline{CS}$ = V_{IL}.
4. Address should be valid prior to or coincident with $\overline{CS}$ transition low.
5. $\overline{OE}$ = V_{IL}.

Write Cycle Timing–1*10



Write Cycle Timing–2*6, *10



Notes: 1. Transition is measured ±200 mV from high impedance voltage with load (B).
This parameter is sampled and not 100% tested.

2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the ealier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state. The input signals out of phase must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
7. Dout is in the same phase of written data of this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The input signals out of phase must not be applied to I/O pins.
10. $\overline{WE}$ must be high during all address transitions except when device is deselected with $\overline{CS}$.

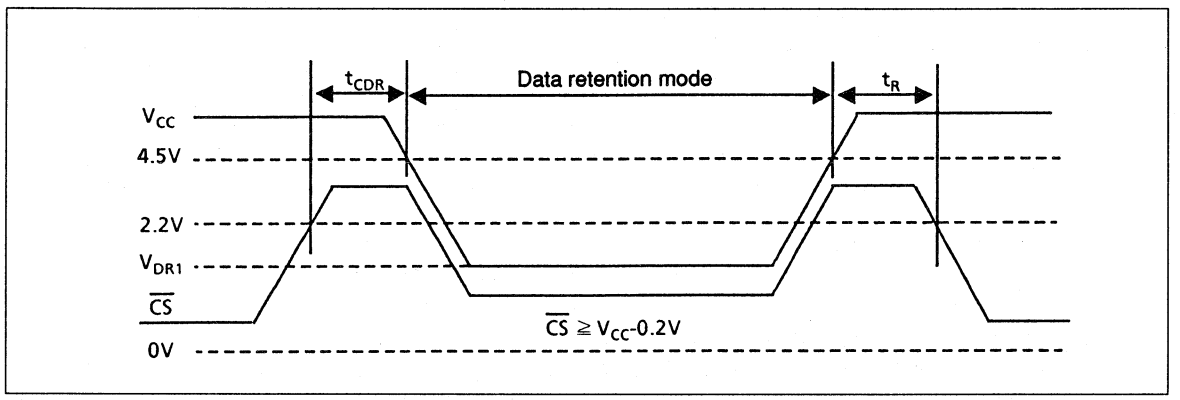
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

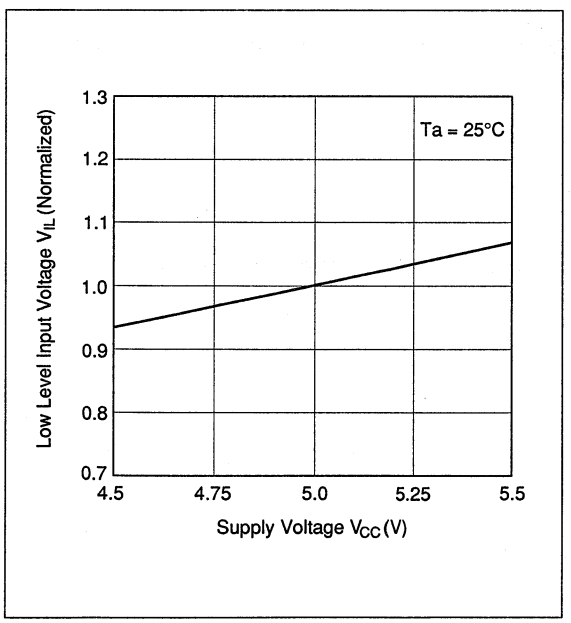
This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC}$ –0.2 V, Vin ≥ V_{CC} –0.2 V or 0 V ≤ Vin ≤ 0.2 V
Data retention current	I_{CCDR}	—	1	50*1	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

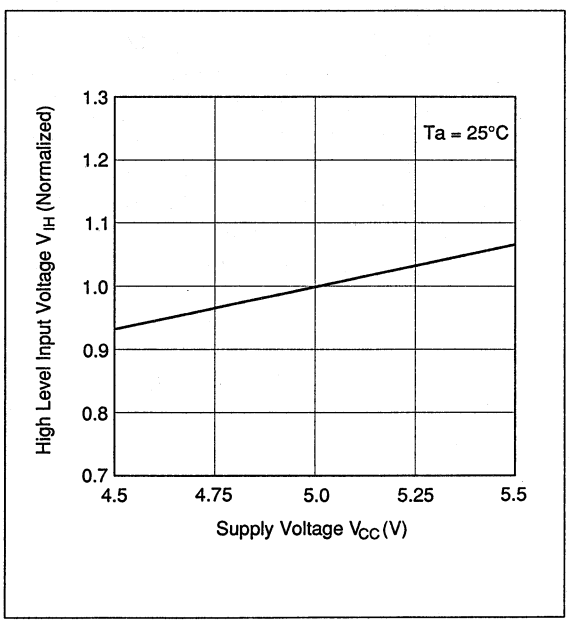
Note: 1. V_{CC} = 3.0 V

Low V_{CC} Data Retention Timing Waveform

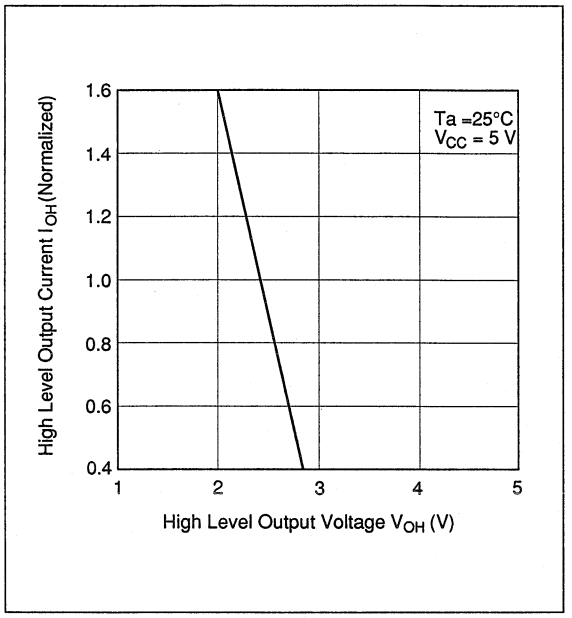




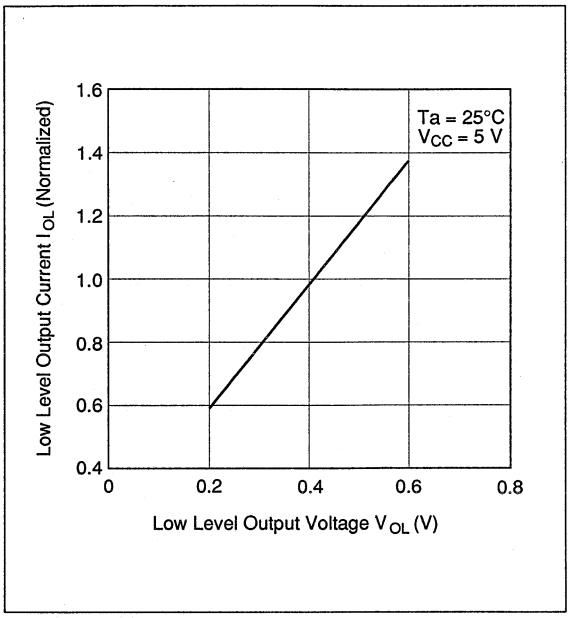
Low Level Input Voltage vs. Supply Voltage



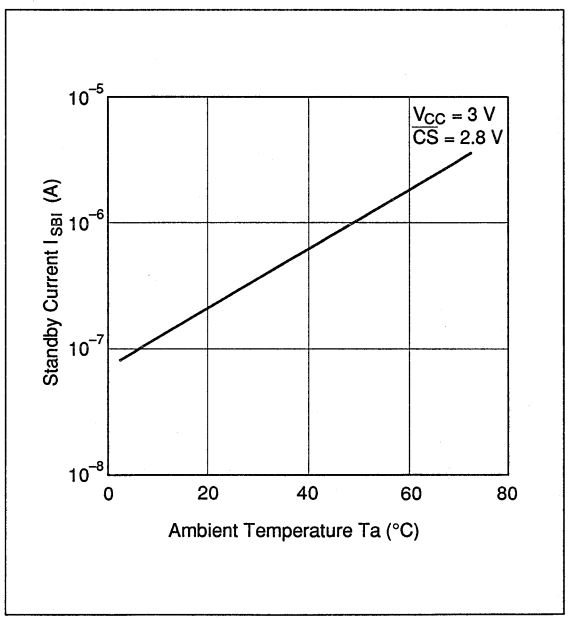
High Level Input Voltage vs. Supply Voltage



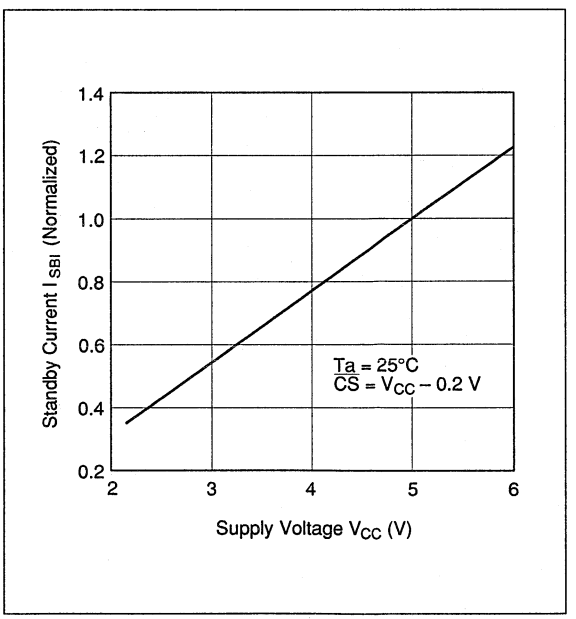
High Level Output Current vs. High Level Output Voltage



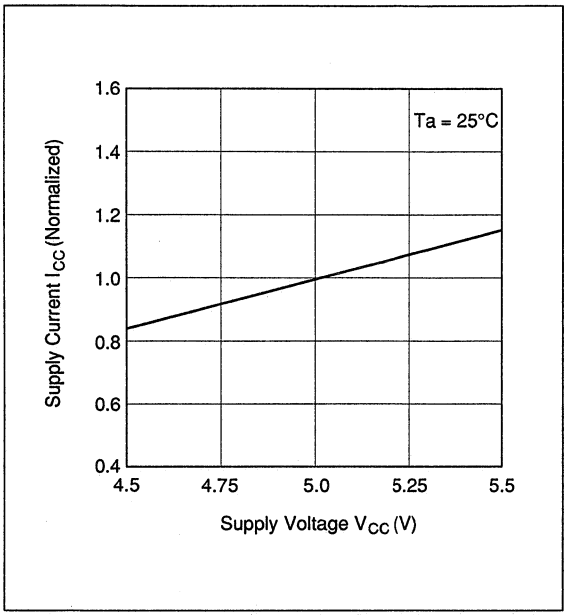
Low Level Output Current vs. Low Level Output Voltage



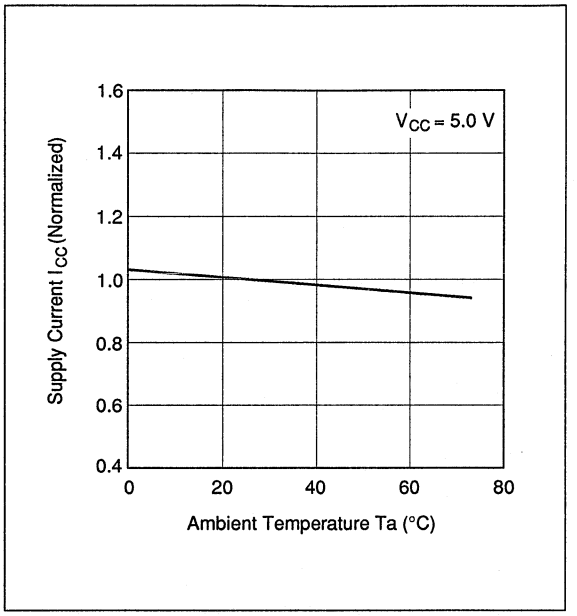
Standby Current vs. Ambient Temperature



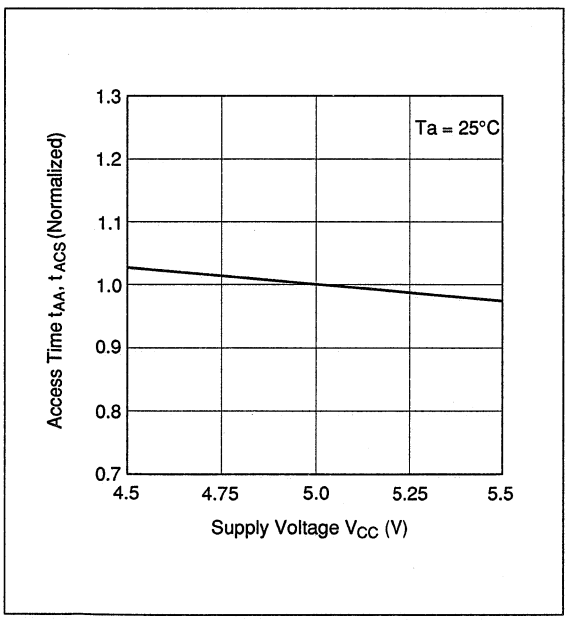
Standby Current vs. Supply Voltage



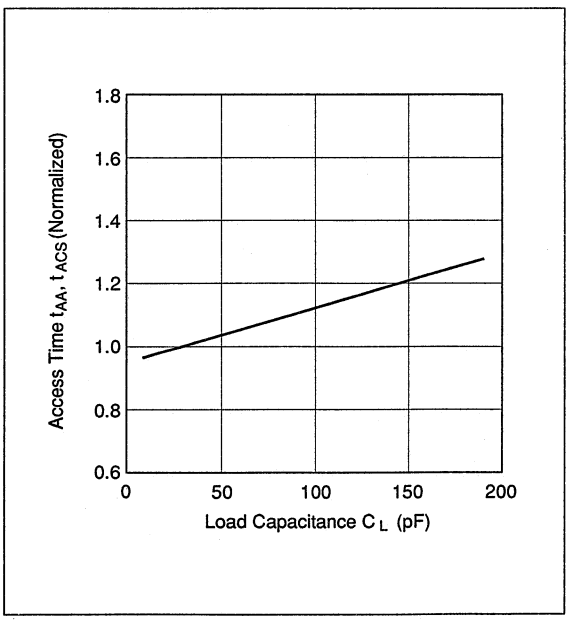
Supply Current vs. Supply Voltage



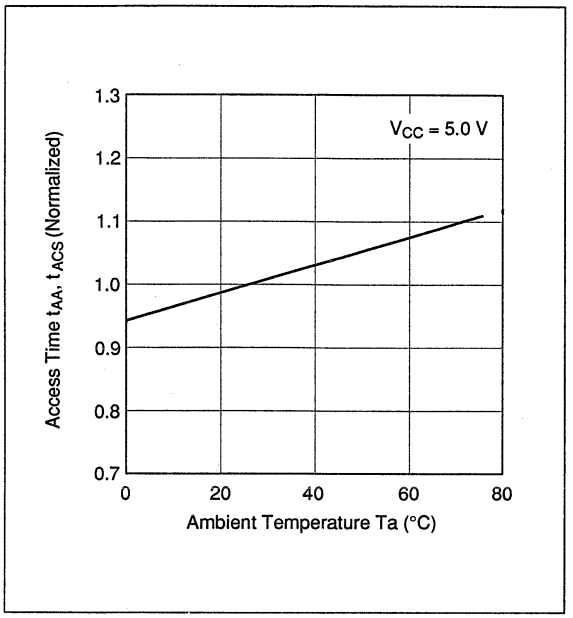
Supply Current vs. Ambient Temperature



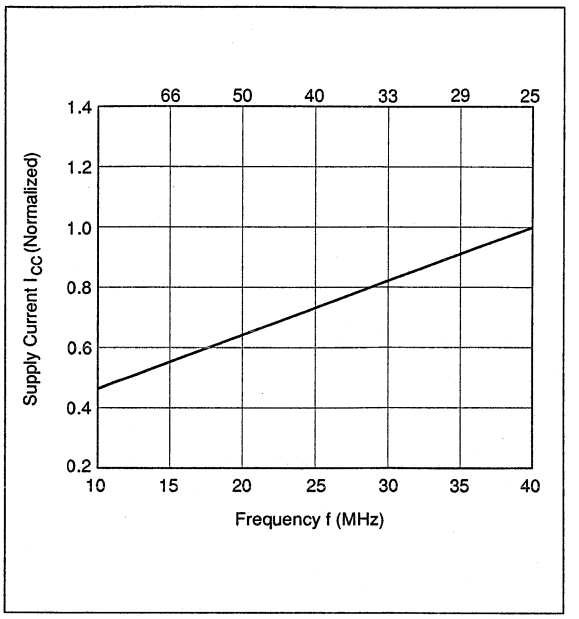
Access Time vs. Supply Voltage



Access Time vs. Load Capacitance



Access Time vs. Ambient Temperature



Supply Current vs. Frequency

HM62832UH Series

32768-word × 8-bit High Speed CMOS Static RAM

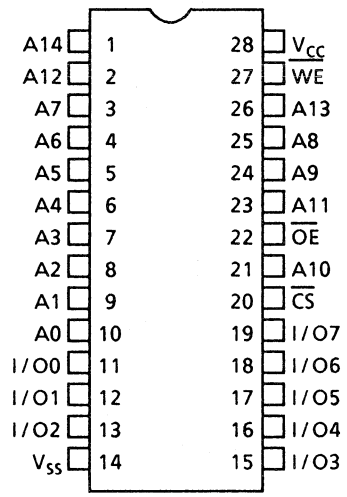
Features

- High speed: Fast access time 15/20 ns (max)
- Low Power
  Standby: 15 µW (typ) (L version)
  Operation: 675/600 mW (typ)
- Single 5 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs

Ordering Information

Type No.	Access time	Package
HM62832UHP-15	15 ns	300-mil 28-pin plastic DIP (DP-28NA)
HM62832UHP-20	20 ns	
HM62832UHLP-15	15 ns	
HM62832UHLP-20	20 ns	
HM62832UHJP-15	15 ns	300-mil 28-pin plastic SOJ (CP-28DN)
HM62832UHJP-20	20 ns	
HM62832UHLJP-15	15 ns	
HM62832UHLJP-20	20 ns	

Pin Arrangement

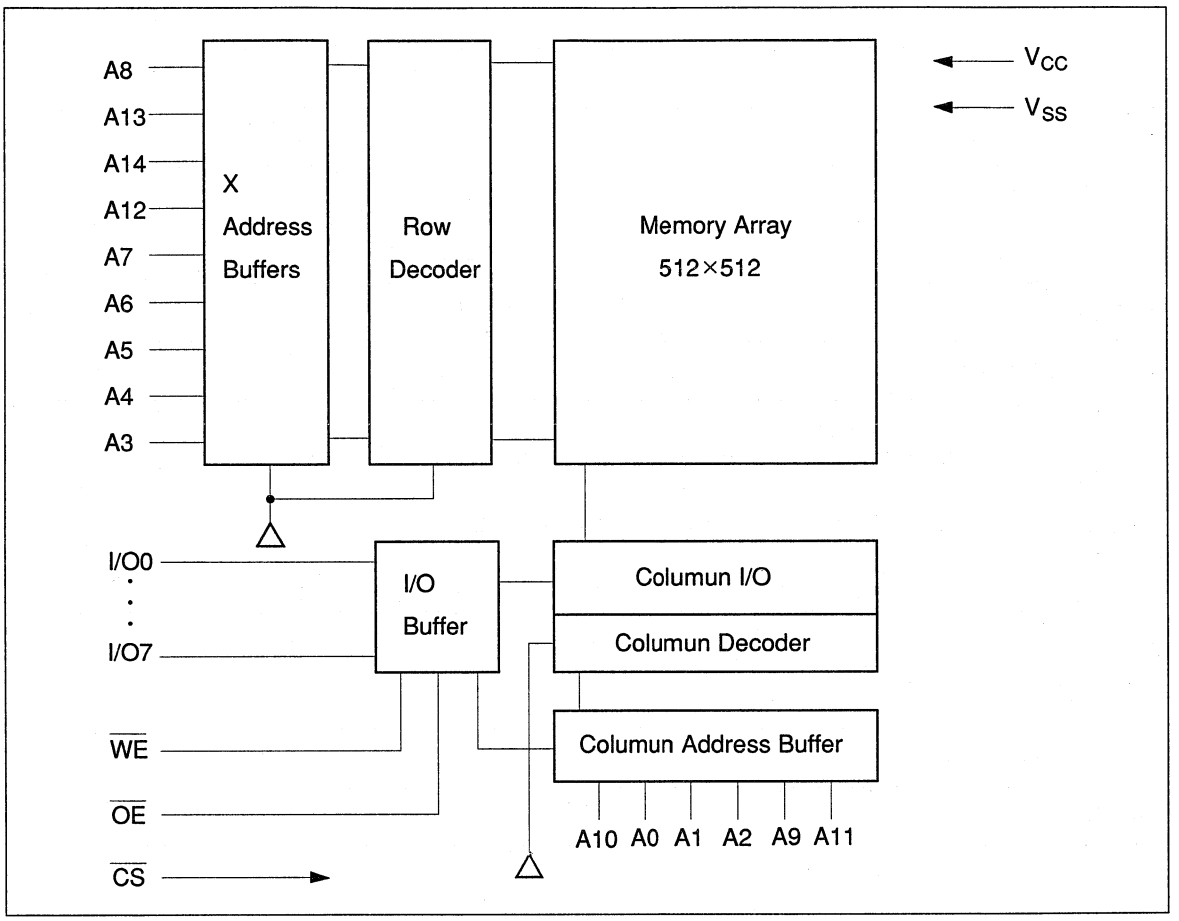


(Top View)

Pin Description

Symbol	Function
A0 – A14	Address
I/O0 – I/O7	Input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
H	X	X	Standby	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	I_{CC}	Dout	Read cycle 1, 2, 3
L	H	L	Write	I_{CC}	Din	Write cycle 1
L	L	L	Write	I_{CC}	Din	Write cycle 2

Note: X : H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply voltage*1	V_{CC}	−0.5*2 to +7.0	V
Voltage on any pin relative to V_{SS}*1	V_T	−0.5*2 to V_{CC} +0.5	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Notes: 1. With respect to V_{SS}
2. V_{CC} and V_T min = −2.5 V for pulse width ≤ 10 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	V_{CC} +0.5	V
Input low (logic 0) voltage	V_{IL}	−0.5*1	—	0.8	V

Note: 1. V_{IL} min = −2.0 V for pulse with ≤ 10 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min	Typ*1	Max	Unit	Test conditions	
Input leakage current	$\|I_{LI}\|$	—	—	2.0	µA	V_{CC} = 5.5 V Vin = V_{SS} to V_{CC}	
Output leakage current	$\|I_{LO}\|$	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}	
Operating V_{CC} current	I_{CC1} (–15) *3	—	135	170	mA	min cycle	*2
	I_{CC2} (–15)	—	100	120	mA	2x min cycle	
	I_{CC1} (–20)	—	120	150	mA	min cycle	
	I_{CC2} (–20)	—	90	110	mA	2x min cycle	
Standby V_{CC} current	I_{SB} (–15)	—	40	60	mA	$\overline{CS}$ = V_{IH}, min cycle	
	I_{SB} (–20)	—	30	50			
Standby V_{CC} current (1)	I_{SB1} (L-version)	—	0.02	2.0	mA	$\overline{CS}$ ≥ V_{CC} –0.2 V 0 V ≤ Vin ≤ 0.2 V or V_{CC} –0.2 V ≤ Vin	
		—	0.003	0.1			
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA	
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4.0 mA	

Notes: 1. Typical limits are at V_{CC} = 5.0 V, Ta = 25°C and specified loading.
2. $\overline{CS}$ = V_{IL}, Iout = 0 mA
3. Access time version

Capacitance (Ta = 25°C, f = 1.0 MHz)*1

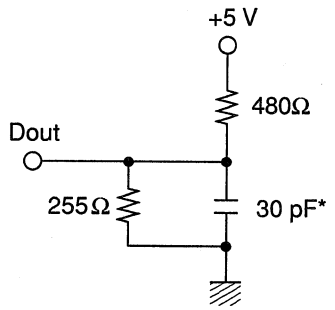
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

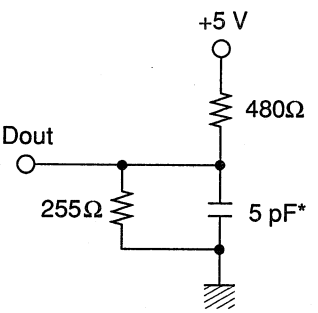
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 4 ns
- Input and Output timing reference levels: 1.5 V
- Output load: See figures



Output load (A)



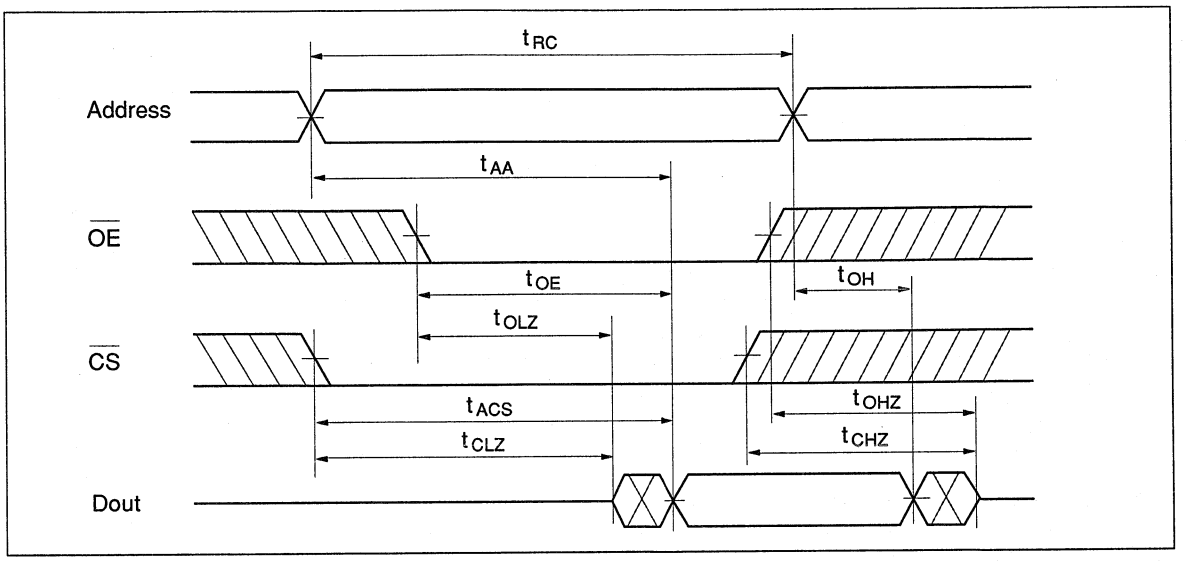
Output load (B)
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ} and t_{OW})

* Including scope and jig

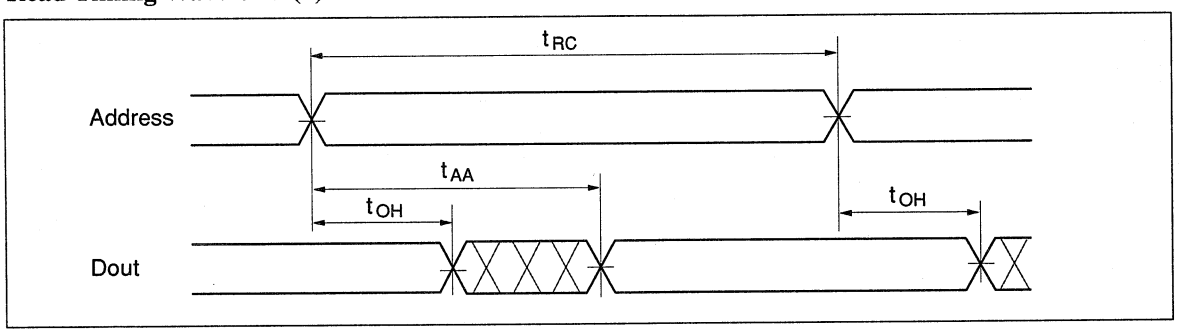
Read Cycle

Item	Symbol	HM62832UH-15 Min	HM62832UH-15 Max	HM62832UH-20 Min	HM62832UH-20 Max	Unit
Read cycle time	t_{RC}	15	—	20	—	ns
Address access time	t_{AA}	—	15	—	20	ns
Chip select access time	t_{ACS}	—	15	—	20	ns
Chip selection to output in low-Z	t_{CLZ}*1	3	—	3	—	ns
Output enable to output valid	t_{OE}	—	8	—	10	ns
Output enable to output in low-Z	t_{OLZ}*1	0	—	0	—	ns
Chip deselection to output in high-Z	t_{CHZ}*1	0	7	0	10	ns
Chip disable to output in high-Z	t_{OHZ}*1	0	7	0	10	ns
Output hold from address change	t_{OH}	3	—	3	—	ns
Chip selection to power up time	t_{PU}	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	15	—	20	ns

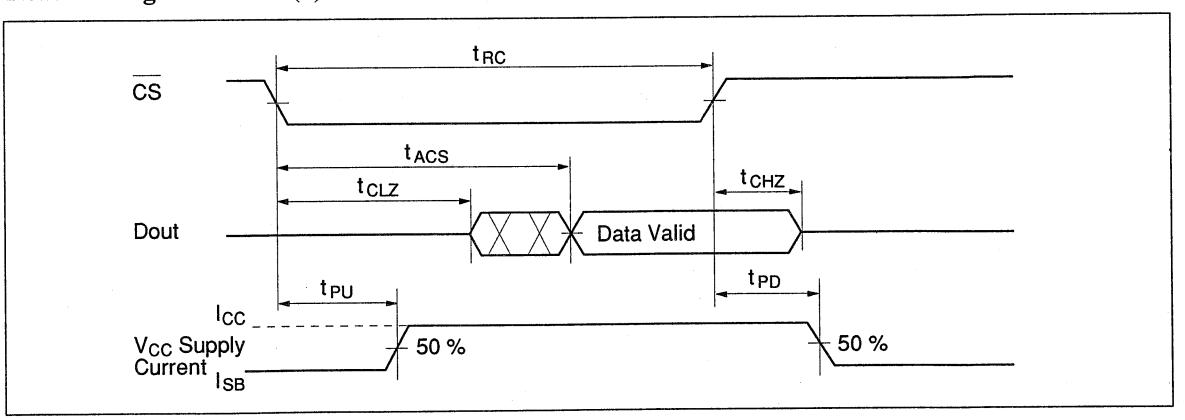
Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *2, *3, *5



Read Timing Waveform (3) *1, *2 *4, *5

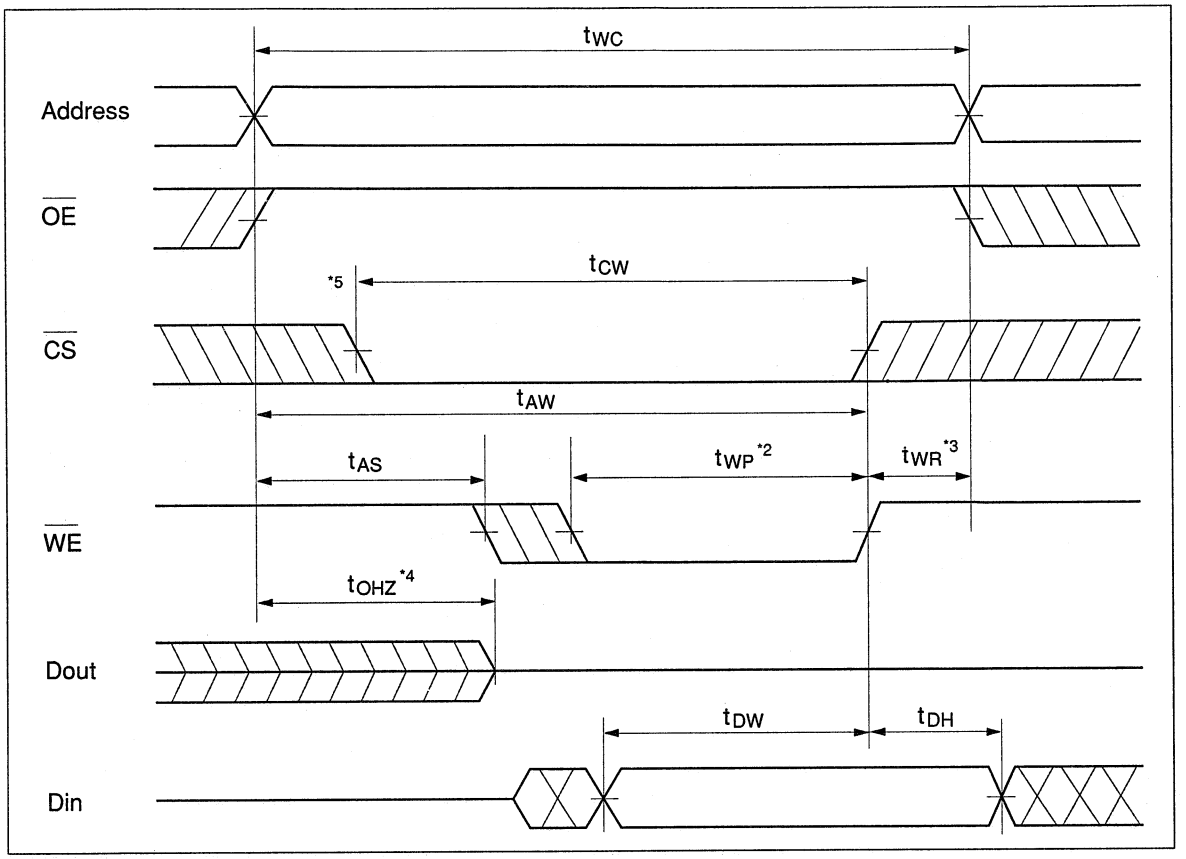


Notes:
1. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
2. $\overline{WE}$ is high for read cycle.
3. Device is continuously selected, $\overline{CS} = V_{IL}$.
4. Address valid prior to or coincident with $\overline{CS}$ transition low.
5. $\overline{OE} = V_{IL}$.

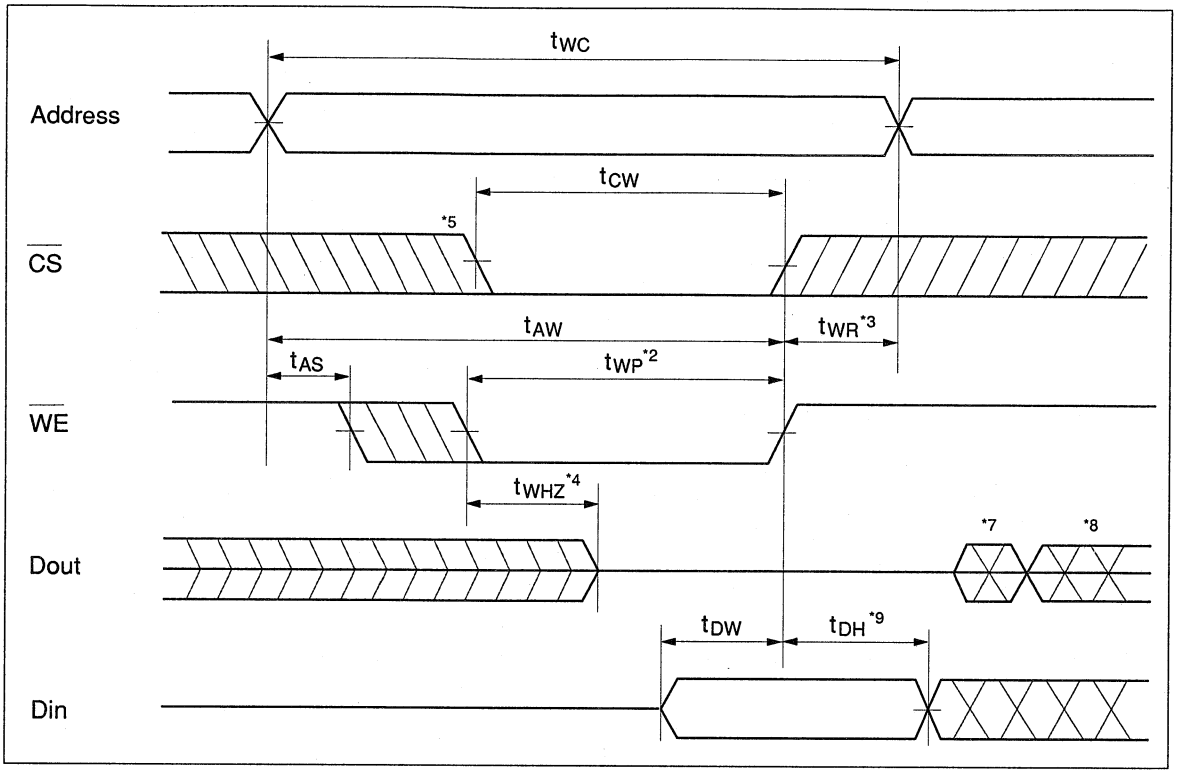
Write Cycle

Item	Symbol	HM62832UH-15		HM62832UH-20		Unit
		Min	Max	Min	Max	
Write cycle time	t_{WC}	15	—	20	—	ns
Chip selection to end of write	t_{CW}	10	—	12	—	ns
Address valid to end of write	t_{AW}	13	—	15	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	10	—	12	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Output disable to output in high-Z*1	t_{OHZ}	0	7	0	10	ns
Write to output in high-Z*1	t_{WHZ}	0	7	0	10	ns
Data to write time overlap	t_{DW}	8	—	10	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Output active from end of write*1	t_{OW}	3	—	3	—	ns

Write Timing Waveform (1)



Write Timing Waveform (2) *6



Notes:
1. Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$)
7. Dout is the same phase of write data of this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. $\overline{WE}$ must be high during all address transition except when device is disable with $\overline{CS}$.

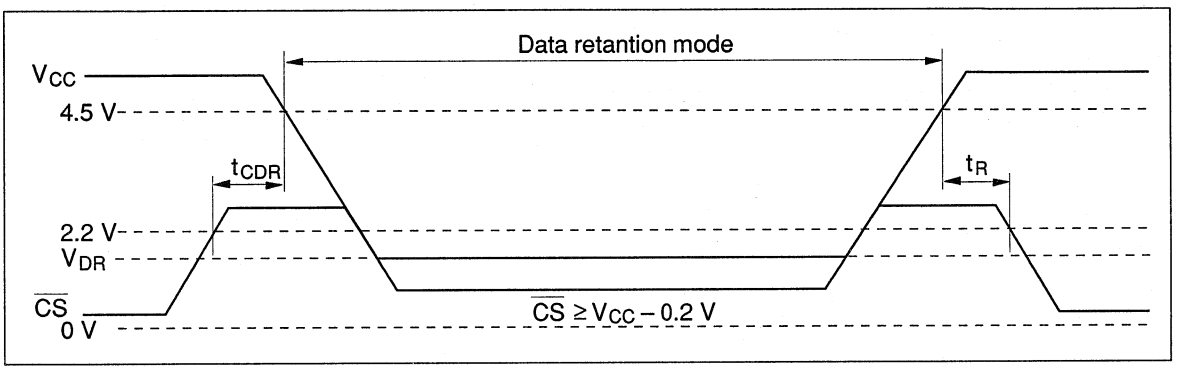
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Item	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2V$, $Vin \geq V_{CC} - 0.2$ V or $0\ V < Vin \leq 0.2$ V
Data retention current	I_{CCDR}	—	2	50*1	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

Note: 1. V_{CC} = 3.0 V

Low V_{CC} Data Retention Timing Waveform



HM67832SH Series

32,768-word × 8-bit High Speed Static Random Access Memory

Features

- 32,768 words × 8 bits organization
- Directly TTL compatible input and output
- 0.8 µm Hi-BiCMOS process
- +5 V single power supply
- Completely static memory: No clock or timing strobe required
- Low power dissipation (DC)
  operating: 400 mW typ
- Super fast access time: 10/12 ns (max)

Ordering Information

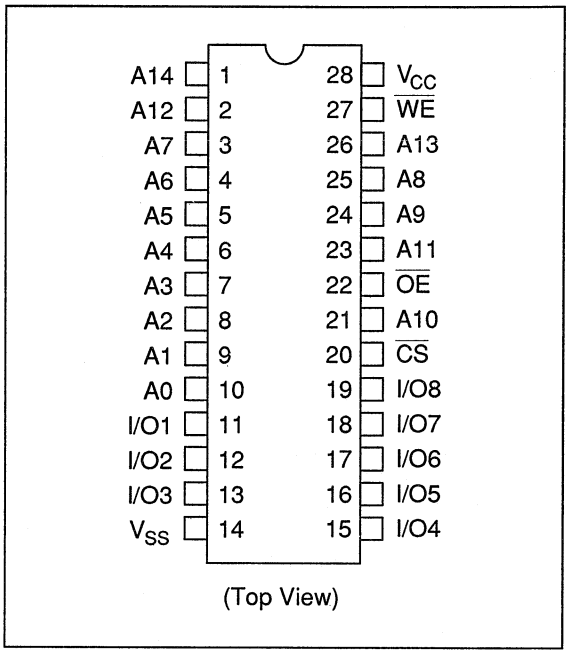
Type No.	Access Time	Package
HM67832SHJP-10*	10 ns	300 mil 28 pin plastic SOJ (CP-28DN)
HM67832SHJP-12*	12 ns	

*Organization: 32k × 8

Pin Description

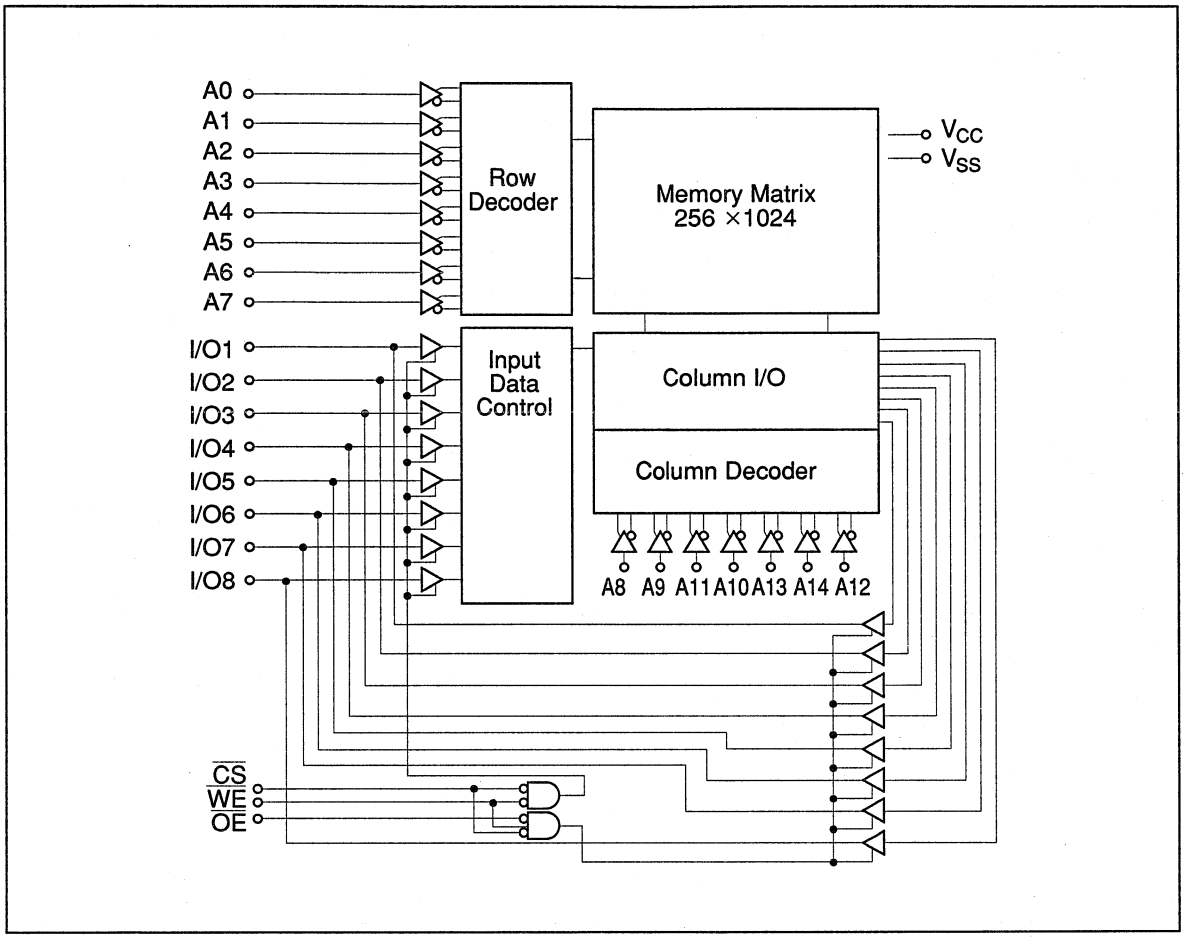
Pin Name	Function
A0–A14	Address input
I/O1–I/O8	Data input/output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
V_{SS}	Ground
V_{CC}	Power supply

Pin Arrangement



(Top View)

Block Diagram



Function Table

Input						
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Output	Mode	V_{CC} Current	Reference Cycle
H	X	X	High Z	Not selected	I_{SB}, I_{SB1}	—
L	H	H	High Z	Output disable	I_{CC}, I_{CC1}	—
L	H	L	Data out	Read	I_{CC}, I_{CC1}	Read cycle 1, 2, 3
L	L	H	Data in	Write	I_{CC}, I_{CC1}	Write cycle 1, 2, 3, 4
L	L	L	Data in	Write	I_{CC}, I_{CC1}	Write cycle 5, 6

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage with respect to V_{SS}	V_{CC}	–0.5 to +7.0	V
Voltage on any pin with respect to V_{SS}	V_T	–0.5 to V_{CC} + 0.5	V
Power dissipation	P_T	1.0	W
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range (with bias)	T_{stg}(bias)	–10 to +85	°C
Storage temperature range	T_{stg}	–55 to +125	°C

For the DC and AC specifications shown in these tables, this device was tested under a minimum transverse air flow exceeding 500 linear feet per minute.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input low voltage	V_{IL}	–3.0[1)]	—	0.8	V

Note 1) Pulse width 10 ns, DC: –0.5 V

DC Characteristics (V_{CC} = 5.0 V ± 10%, Ta = 0 to +70°C)

		–10			–12				
Item	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2	—	—	2	µA	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	10	—	—	10	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $\overline{WE}$ = V_{IL}, $V_{I/O}$ = 0 V to V_{CC}
Average operating current	I_{CC1}	—	150	200	—	140	195	mA	Min. cycle, $I_{I/O}$ = 0 mA
Standby power supply current	I_{SB}	—	—	40	—	—	40	mA	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}
	I_{SB1}	—	—	30	—	—	30	mA	$\overline{CS}$ ≥ V_{CC} –0.2 V, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V
Output low voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH} = –4 mA

Note 1) Typical limits are at V_{CC} = 5.0 V, Ta = 25°C, and specified loading.

Capacitance (Ta =25°C, f=1 MHz)

Item	Symbol	Max	Unit	Test Condition
Input capacitance	C_{in}[1]	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$[1]	10	pF	$V_{I/O}$ = 0 V

Note 1) This parameter is sampled and has not been 100% tested.

AC Characteristics (V_{CC} = 5 V± 10%, Ta = 0 to +70°C, unless otherwise noted)

Test conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5 V
- Output load: See figure 1
- Input rise and fall time: 4 ns
- Output reference level: 1.5 V

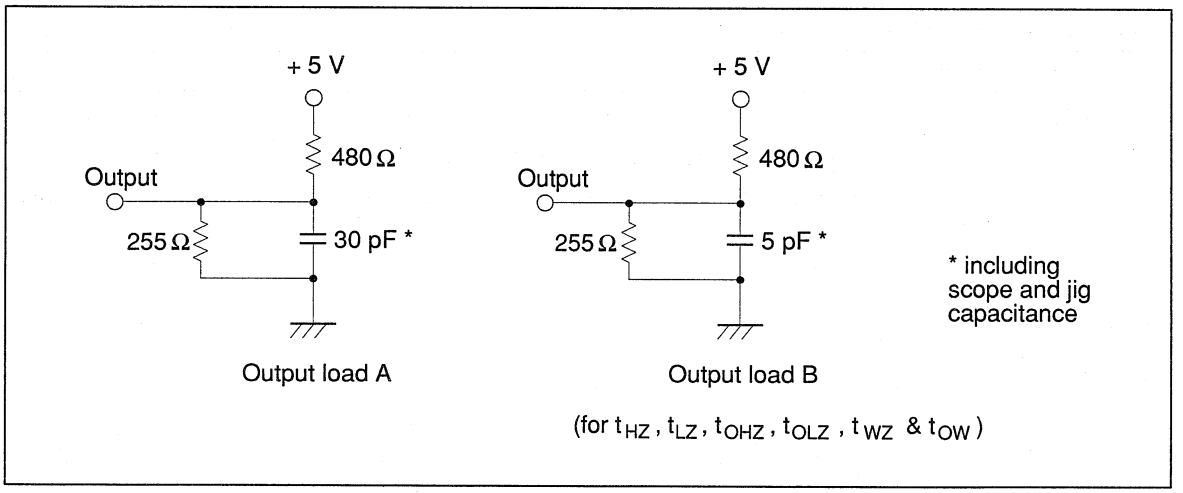


Figure 1 Output Load

Read Cycle

		–10		–12		
Item	Symbol	Min	Max	Min	Max	Unit
Read cycle time	t_{RC}	10	–	12	–	ns
Address access time	t_{AA}	–	10	–	12	ns
Chip select access time	t_{ACS}	–	10	–	12	ns
Chip selection to output low Z	t_{LZ}[1) 2)]	3	–	3	–	ns
Output enable to output valid	t_{OE}	–	5	–	6	ns
Output enable to output low Z	t_{OLZ}[1) 2)]	0	–	0	–	ns
Chip deselection to output high Z	t_{HZ}[1) 2)]	0	5	0	5	ns
Output hold from address change	t_{OH}	3	–	3	–	ns

Notes 1) This parameter is sampled and has not been 100% tested.

2) Transition is measured ±200 mV from steady state voltage with loading specified in figure 1, load (B).

Write Cycle

Item	Symbol	–10 Min	–10 Max	–12 Min	–12 Max	Unit
Write cycle time	t_{WC} [1]	10	–	12	–	ns
Chip selection to end of write	t_{CW}	8	–	9	–	ns
Address valid to end of write	t_{AW}	10	–	11	–	ns
Address setup time	t_{AS}	0	–	0	–	ns
Write pulse width	t_{WP}	8	–	9	–	ns
Write recovery time	t_{WR}	0	–	0	–	ns
Data valid to end of write	t_{DW}	6	–	6	–	ns
Data hold time	t_{DH}	0	–	0	–	ns
Write enable to output high Z	t_{WZ} [2] [3]	0	5	0	6	ns
Output disable to output high Z	t_{OHZ} [2] [3]	0	6	0	6	ns
Output active from end of write	t_{OW} [2] [3]	3	–	3	–	ns

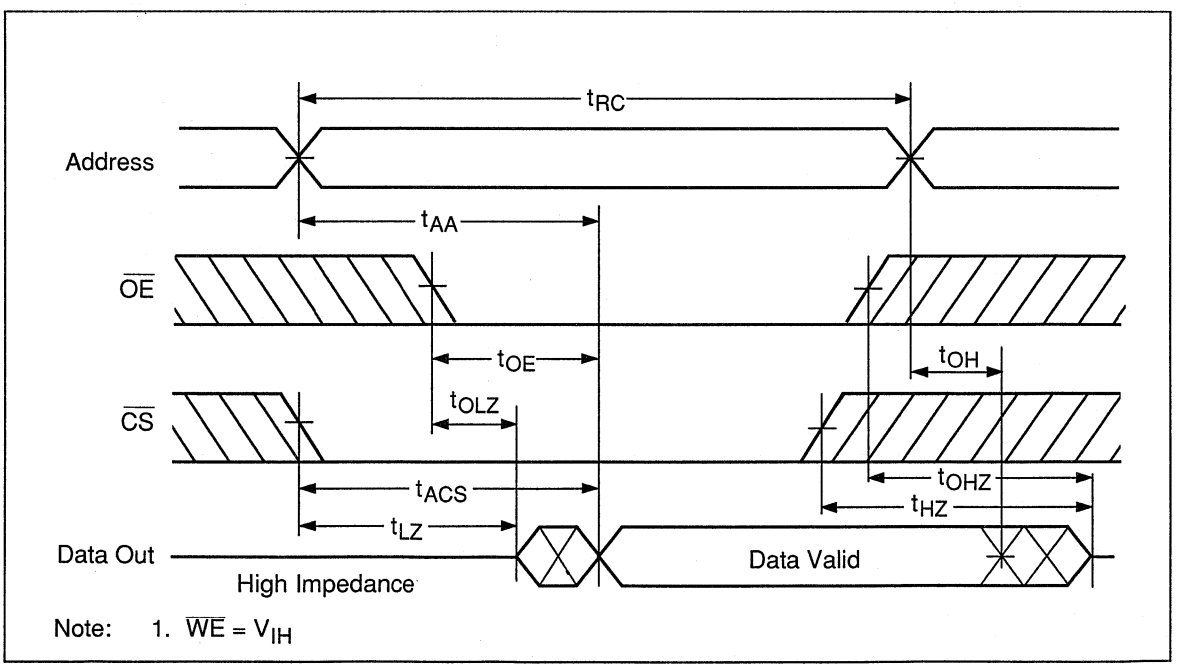
Notes 1) All write cycle timings are referenced from the last valid address to the first changing address.

2) This parameter is sampled and has not been 100% tested.

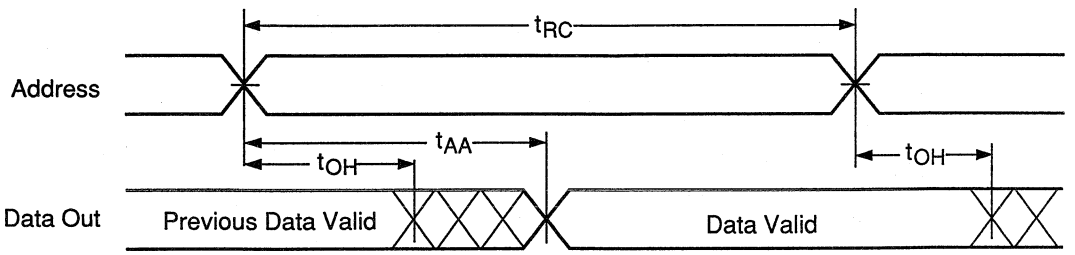
3) Transition is measured ±200 mV from steady state voltage with loading specified in figure 1, load (B).

Timing Waveforms

Read Cycle 1

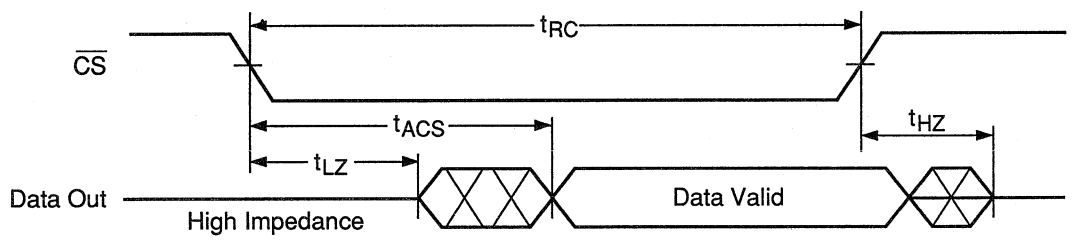


Read Cycle 2



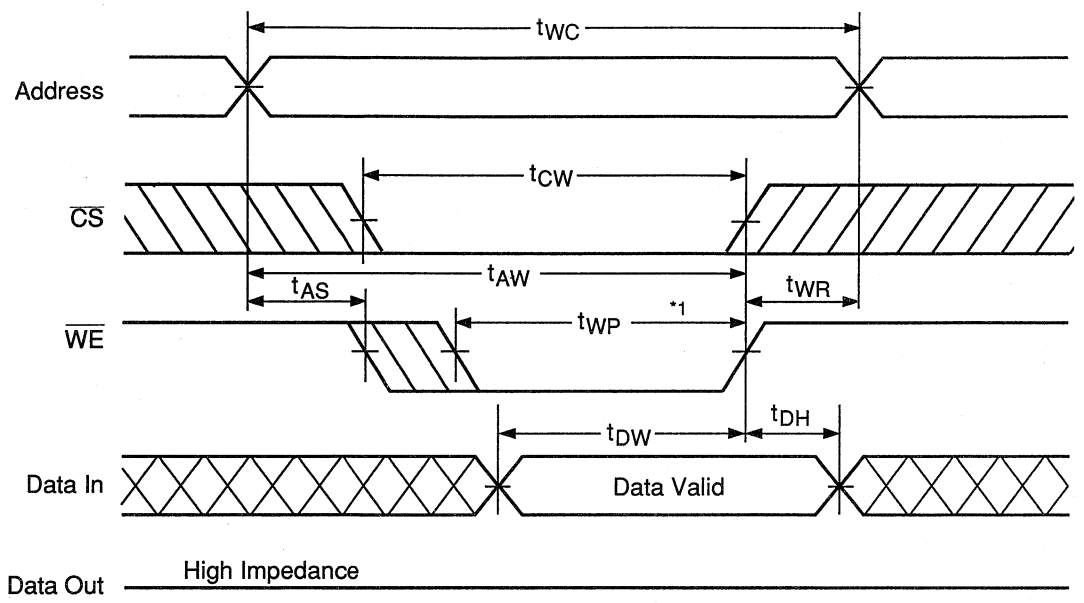
Notes: 1. $\overline{WE} = V_{IH}$
2. $\overline{CS} = V_{IL}$
3. $\overline{OE} = V_{IL}$

Read Cycle 3



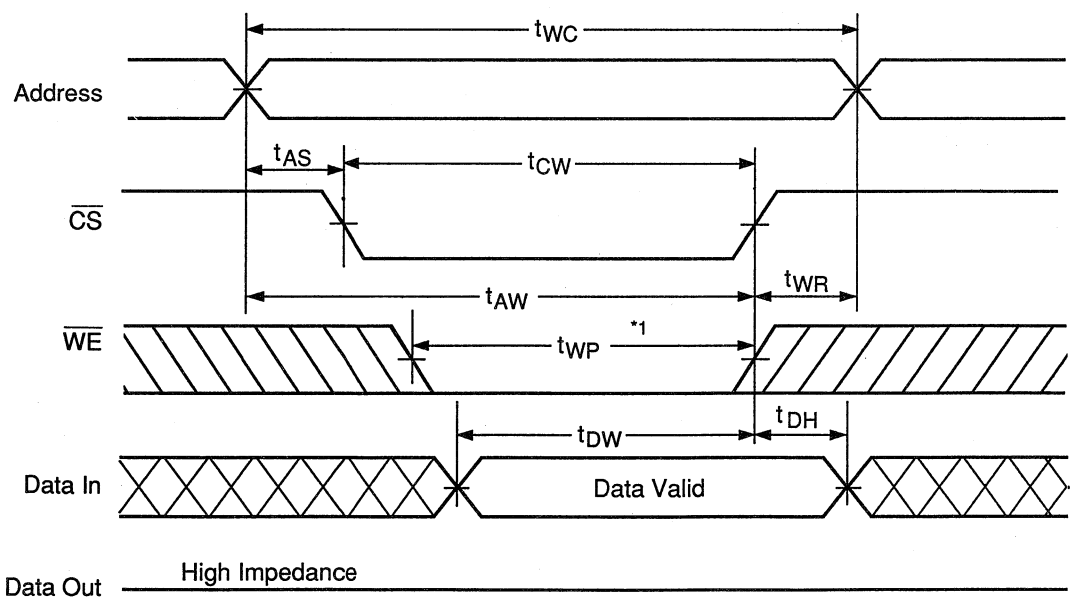
Notes: 1. $\overline{WE} = V_{IH}$
2. $\overline{OE} = V_{IL}$
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle 1 ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



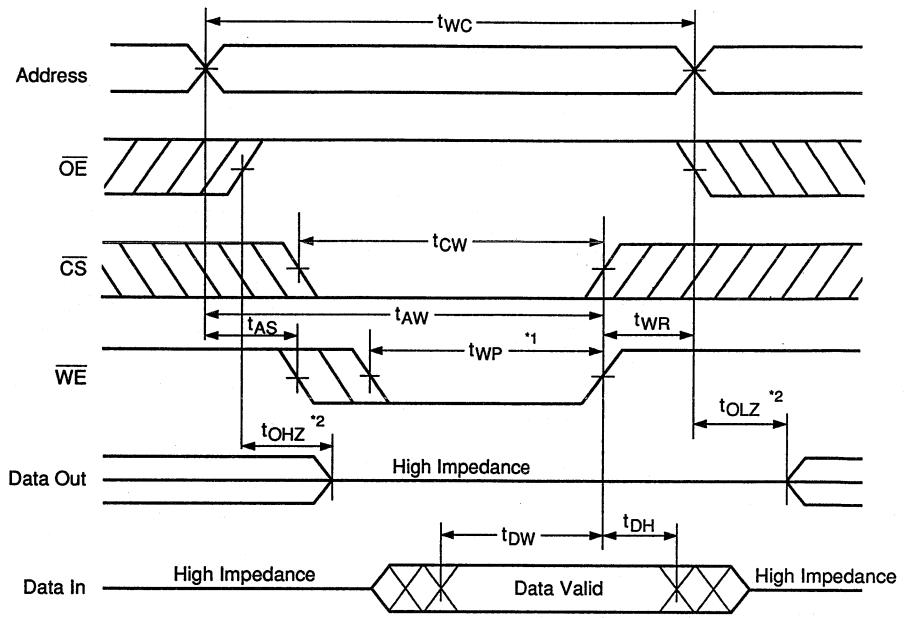
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle 2 ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



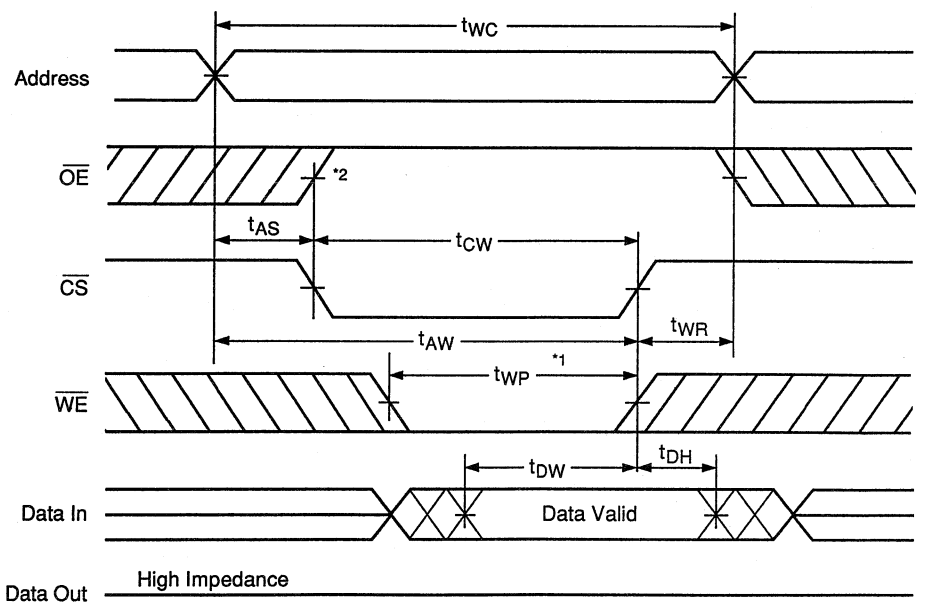
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle 3 ($\overline{OE}$ = clocked, $\overline{WE}$ controlled)



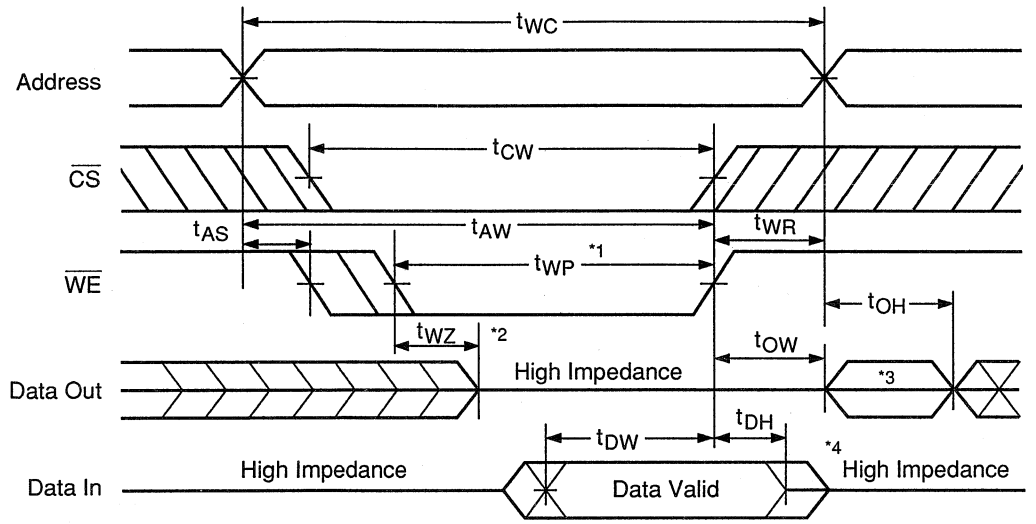
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

Write Cycle 4 ($\overline{OE}$ = clocked, $\overline{CS}$ controlled)



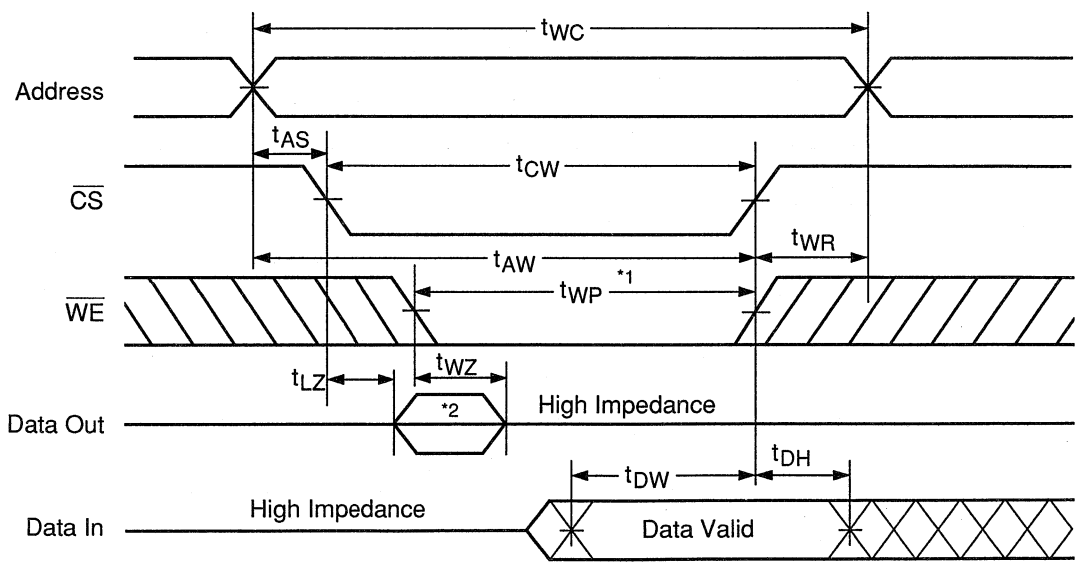
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in a high impedance state.

Write Cycle 5 ($\overline{OE}$ = L, $\overline{WE}$ controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. During this period, I/O pins are output state so that the input signals of opposite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.

Write Cycle 6 ($\overline{OE}$ = L, $\overline{CS}$ controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.

HM6709A Series

65536-word × 4-bit High Speed Static Random Access Memory

Features

- 65536-words × 4 bit organization
- Fully TTL compatible input and output
- 1.0 µm Hi-BiCMOS process
- +5 V single supply
- Completely static memory
  No clock or timing strobe required
- Low power dissipation
  Operating: 450 mW typ
- Super fast
  Address access time: 15/20/25 ns (max)
  $\overline{OE}$ access time: 7/10/10 ns (max)

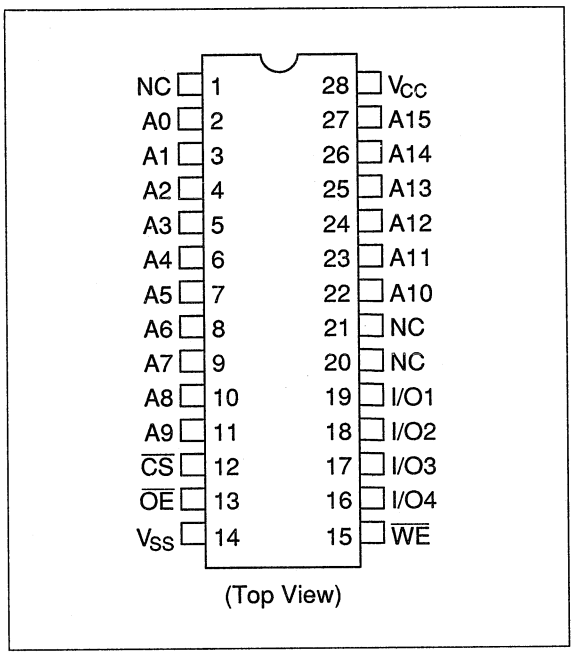
Ordering Information

Type No.	Access time	Package
HM6709AJP-15	15 ns	300-mil 28-pin plastic SOJ (CP-28DN)
HM6709AJP-20	20 ns	
HM6709AJP-25	25 ns	

Pin Description

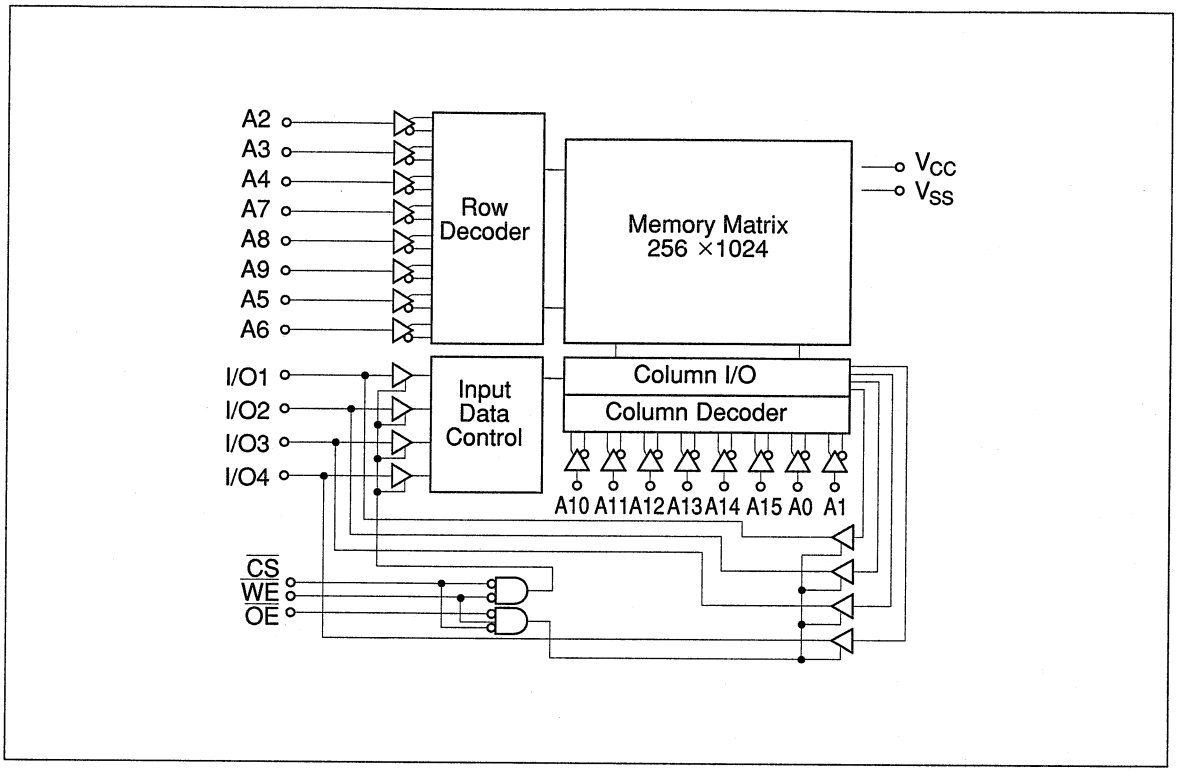
Pin name	Function
A0 – A15	Address input
I/O1 – I/O4	Data input/output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
V_{SS}	Ground
V_{CC}	Power supply

Pin Arrangement



(Top View)

Block Diagram



Function Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O pin	V_{CC} current	Ref. cycle
H	X	X	Not selected	High-Z	I_{SB}, I_{SB1}	—
L	H	H	Output disable	High-Z	I_{CC}, I_{CC1}	—
L	H	L	Read	Data out	I_{CC}, I_{CC1}	Read cycle (1), (2), (3)
L	L	H	Write	Data in	I_{CC}, I_{CC1}	Write cycle (1), (2), (3), (4)
L	L	L	Write	Data in	I_{CC}, I_{CC1}	Write cycle (5), (6)

Absolute Maximum Rating

Item	Symbol	Rating	Unit
Terminal voltage to V_{SS} pin	V_T	–0.5 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range (with bias)	Tstg (Bias)	–10 to +85	°C
Storage temperature range	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to + 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input high voltage	V_{IH}	2.2	—	V_{CC} +0.5	V
Input low voltage	V_{IL}	–3.0*1	—	0.8	V

Note: 1. Pulse width 15 ns, DC : –0.5 V

DC Characteristics (V_{CC} = 5.0V ± 10%, Ta = 0 to +70°C)

Item	Symbol	HM6709A-15 Min	HM6709A-15 Typ	HM6709A-15 Max	HM6709A-20/25 Min	HM6709A-20/25 Typ	HM6709A-20/25 Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	2	—	—	2	µA	V_{CC} = 5.5 V, Vin = 0 V to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	10	—	—	10	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $\overline{WE}$ = V_{IL} $V_{I/O}$ = 0 V to V_{CC}
Operating power supply current	I_{CC}	—	—	100	—	—	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA
Average operating current	I_{CC1}	—	—	140	—	—	120	mA	min. cycle, Duty : 100%, $I_{I/O}$ = 0 mA
Standby power supply current	I_{SB}	—	—	30	—	—	30	mA	$\overline{CS}$ = V_{IH}, Vin = V_{IH} or V_{IL}
	I_{SB1}	—	—	10	—	—	10	mA	$\overline{CS}$ ≥ V_{CC} –0.2 V Vin ≤ 0.2 V or Vin ≥ V_{CC} –0.2 V
Output low voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH} = –4 mA

Capacitance (Ta = 25°C, f = 1 MHz)

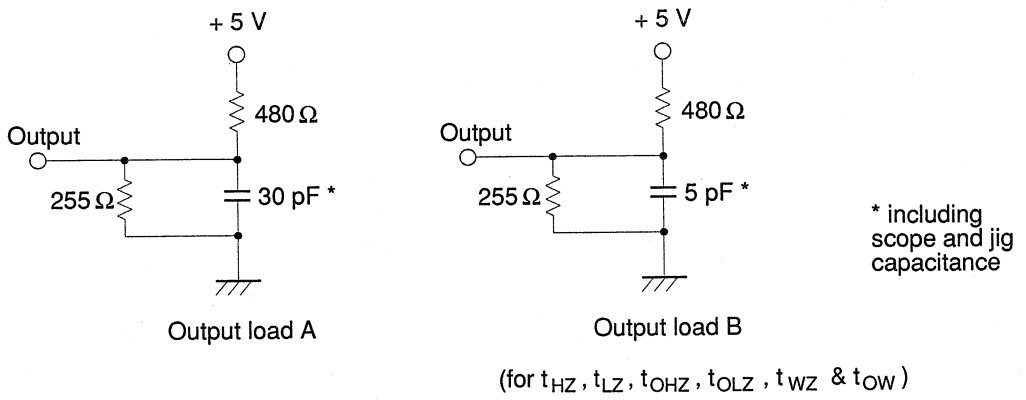
Item	Symbol	Max	Unit	Test condition
Input capacitance	C_{in}*1	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$*1	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC} = 5 V ± 10%, Ta = 0°C to +70°C, unless otherwise noted)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5 V
- Output load: See figures
- Input rise and fall times: 4 ns
- Output reference levels: 1.5 V



Read Cycle

Item	Symbol	HM6709A-15 Min	HM6709A-15 Max	HM6709A-20 Min	HM6709A-20 Max	HM6709A-25 Min	HM6709A-25 Max	Unit
Read cycle time	t_{RC}	15	—	20	—	25	—	ns
Address access time	t_{AA}	—	15	—	20	—	25	ns
Chip select access time	t_{ACS}	—	15	—	20	—	25	ns
Chip selection to output in low-Z	t_{LZ}*1, *2	4	—	4	—	4	—	ns
Output enable to output valid	t_{OE}	0	7	0	10	0	10	ns
Output enable to output in low-Z	t_{OLZ}*1, *2	0	—	0	—	0	—	ns
Chip deselection to output in high-Z	t_{HZ}*1, *2	0	6	0	8	0	10	ns
Output hold from address change	t_{OH}	4	—	5	—	5	—	ns

Notes: 1. This parameter is sampled and not 100% tested.
2. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).

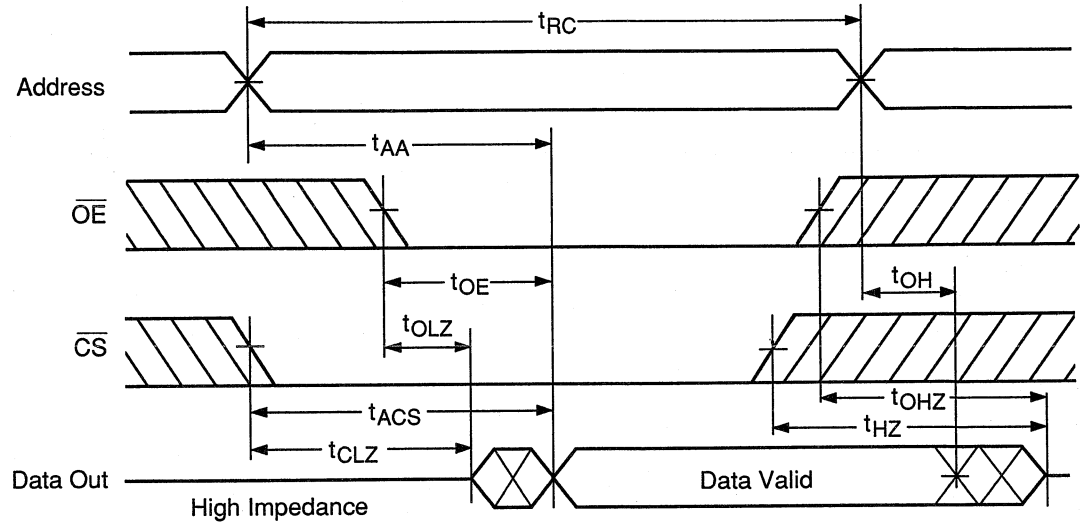
Write Cycle

Item	Symbol	HM6709A-15 Min	HM6709A-15 Max	HM6709A-20 Min	HM6709A-20 Max	HM6709A-25 Min	HM6709A-25 Max	Unit
Write cycle time	t_{WC}*1	15	—	20	—	25	—	ns
Chip selection to end of write	t_{CW}	10	—	15	—	20	—	ns
Address valid to end of write	t_{AW}	10	—	15	—	20	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	10	—	15	—	20	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Data valid to end of write	t_{DW}	8	—	10	—	12	—	ns
Data hold time	t_{DH}	0	—	0	—	0	—	ns
Write enable to output in high-Z	t_{WZ}*2, *3	0	6	0	8	0	10	ns
Output disable to output in high-Z	t_{OHZ}*2, *3	0	6	0	8	0	10	ns
Output active from end of write	t_{OW}*2, *3	0	—	0	—	0	—	ns

Notes: 1. All write cycle timings are referenced from the last valid address to the first transitioning address.
2. This parameter is sampled and not 100% tested.
3. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).

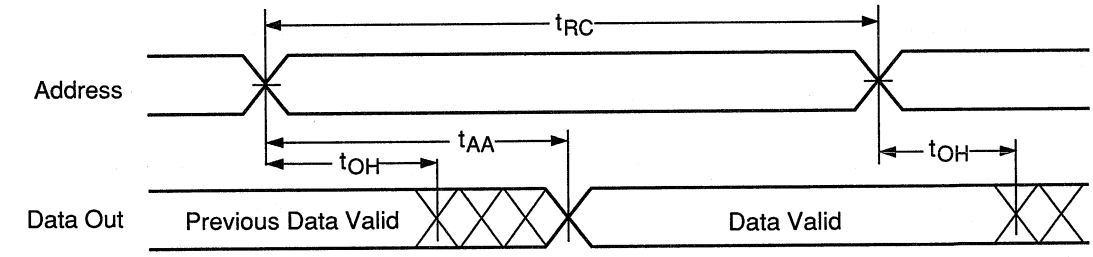
Timing Waveforms

Read Cycle (1) *1



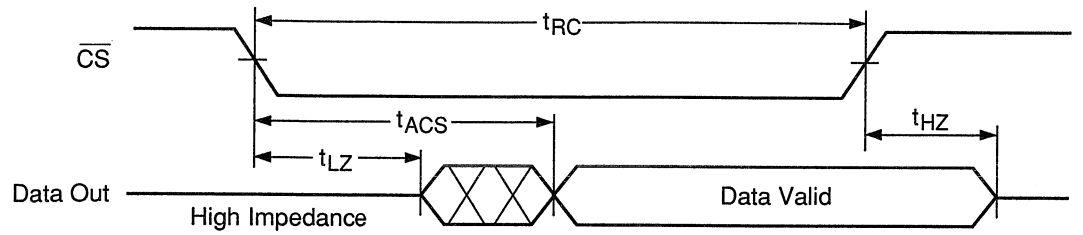
Note: 1. $\overline{WE} = V_{IH}$

Read Cycle (2) *1, *2, *3



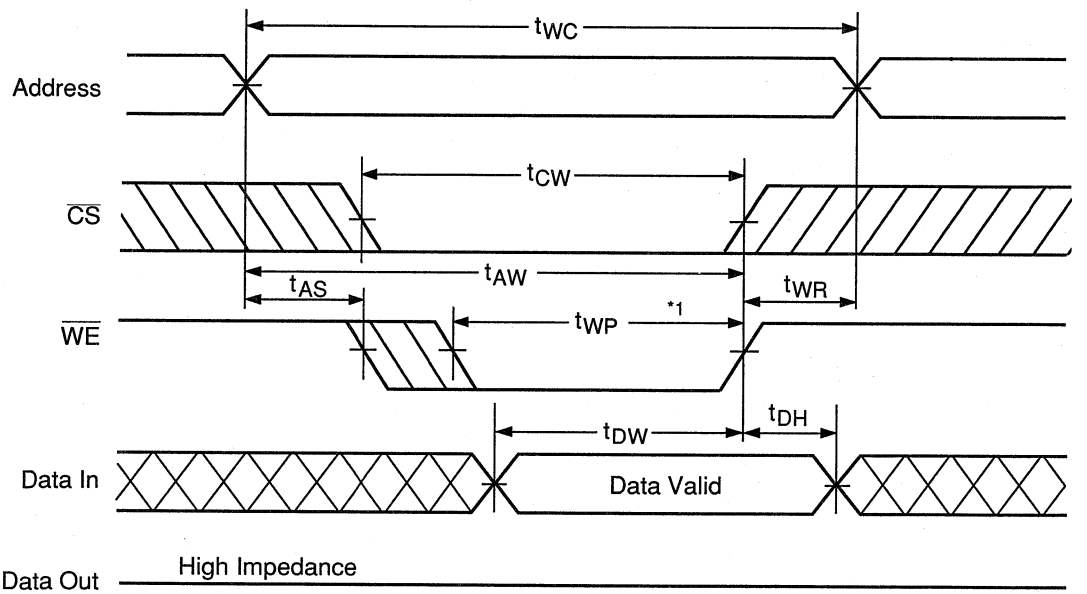
Notes: 1. $\overline{WE} = V_{IH}$
2. $\overline{CS} = V_{IL}$
3. $\overline{OE} = V_{IL}$

Read Cycle (3) *1, *2, *3



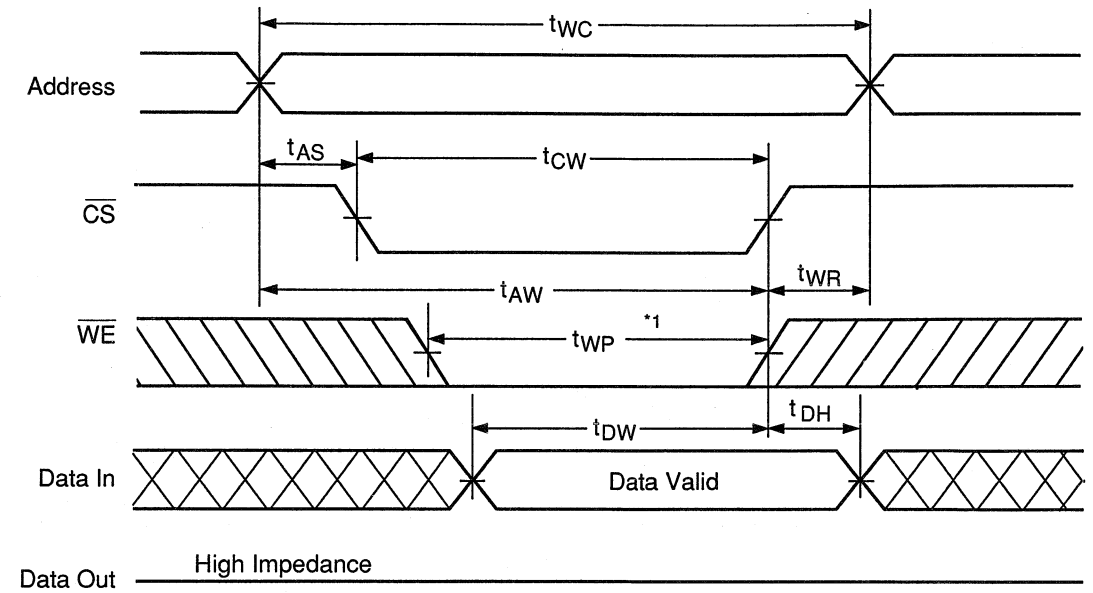
Notes: 1. $\overline{WE} = V_{IH}$
2. $\overline{OE} = V_{IL}$
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle (1) *1 ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



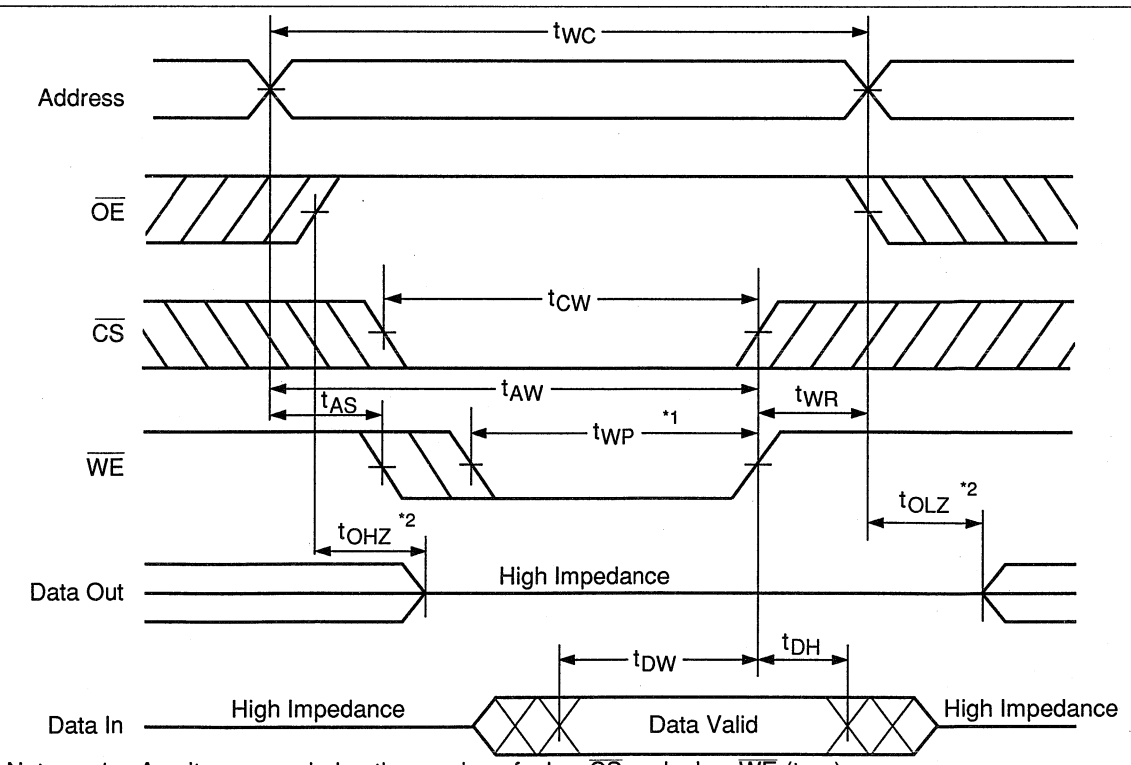
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle (2) *1 ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



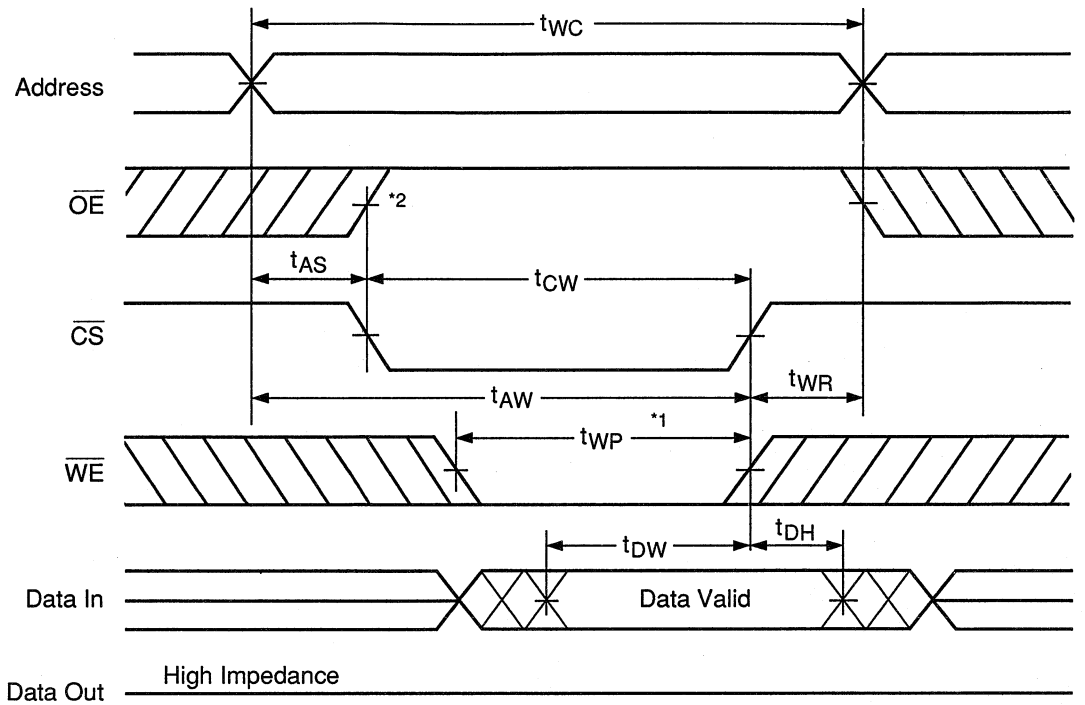
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle (3) *1, *2 ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



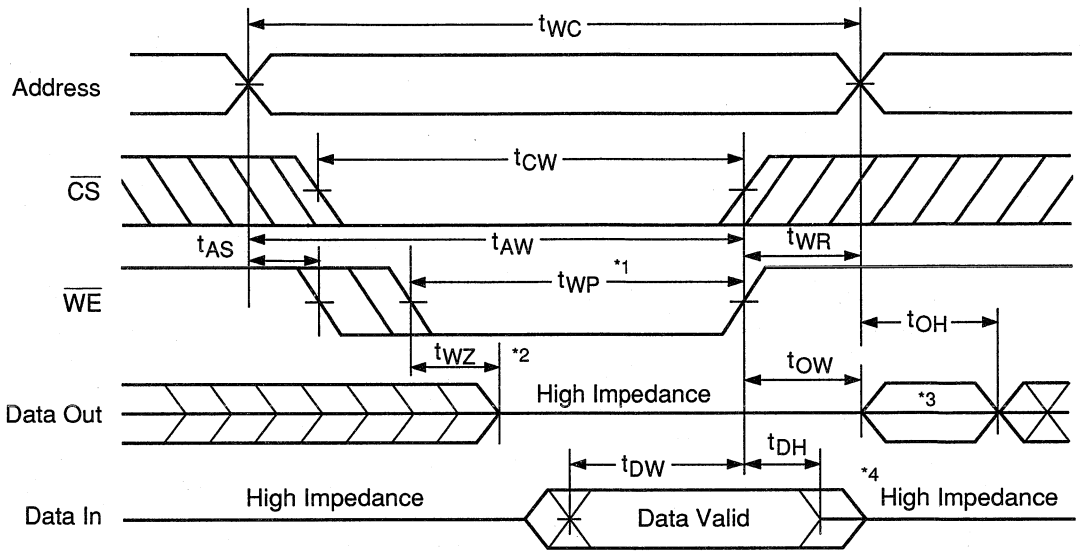
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

Write Cycle (4) *1, *2 ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



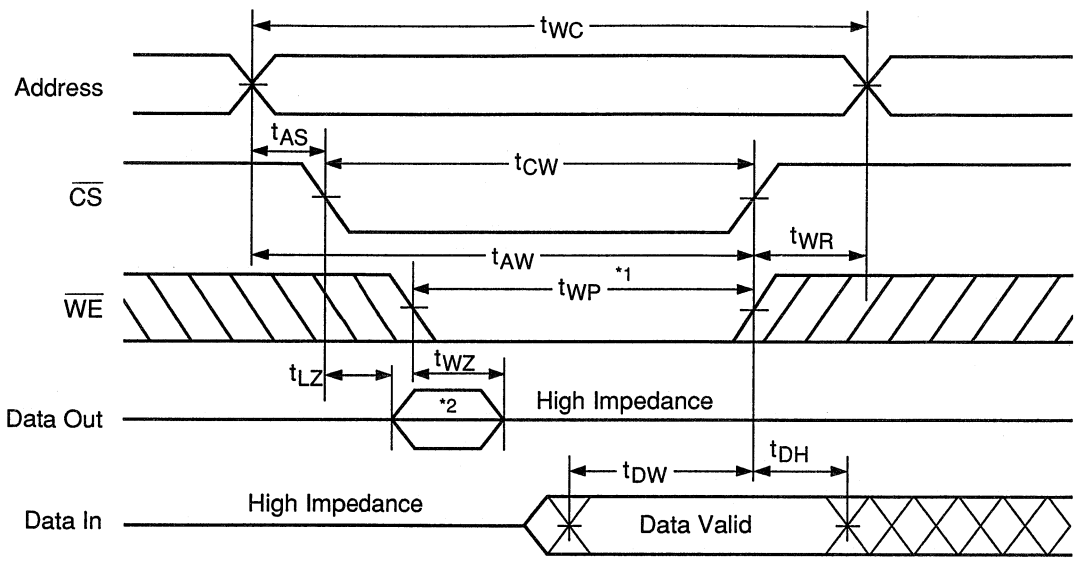
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

Write Cycle (5) *1, *2, *3, *4 ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. During this period, I/O pins are output state so that the input signals of opposite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.

Write Cycle (6) *1, *2 ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.

HM6208H Series

65536-Word × 4-Bit High Speed CMOS Static RAM

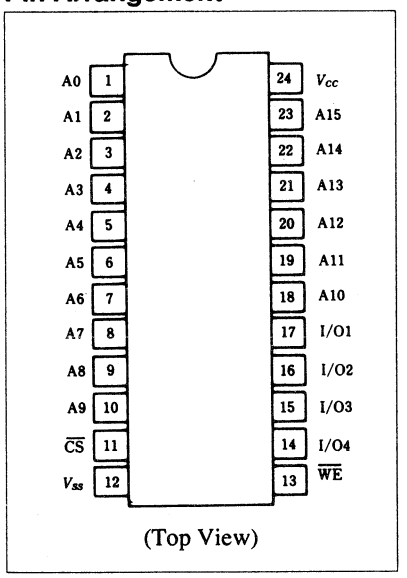
Features

- Single 5 V supply and high density 24-pin package
- High speed: Access time 25/35/45 ns (max)
- Low power
  - Operation: 300 mW (typ)
  - Standby: 100 μW (typ)
  - 30 μW (typ) (L-version)
- Completely static memory required
  - No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation (L-version)

Ordering Information

Type No.	Access Time	Package
HM6208HP-25	25 ns	300-mil 24-pin plastic DIP (DP-24NC)
HM6208HP-35	35 ns	
HM6208HP-45	45 ns	
HM6208HLP-25	25 ns	
HM6208HLP-35	35 ns	
HM6208HLP-45	45 ns	
HM6208HJP-25	25 ns	300-mil 24-pin SOJ (CP-24D)
HM6208HJP-35	35 ns	
HM6208HJP-45	45 ns	
HM6208HLJP-25	25 ns	
HM6208HLJP-35	35 ns	
HM6208HLJP-45	45 ns	

Pin Arrangement

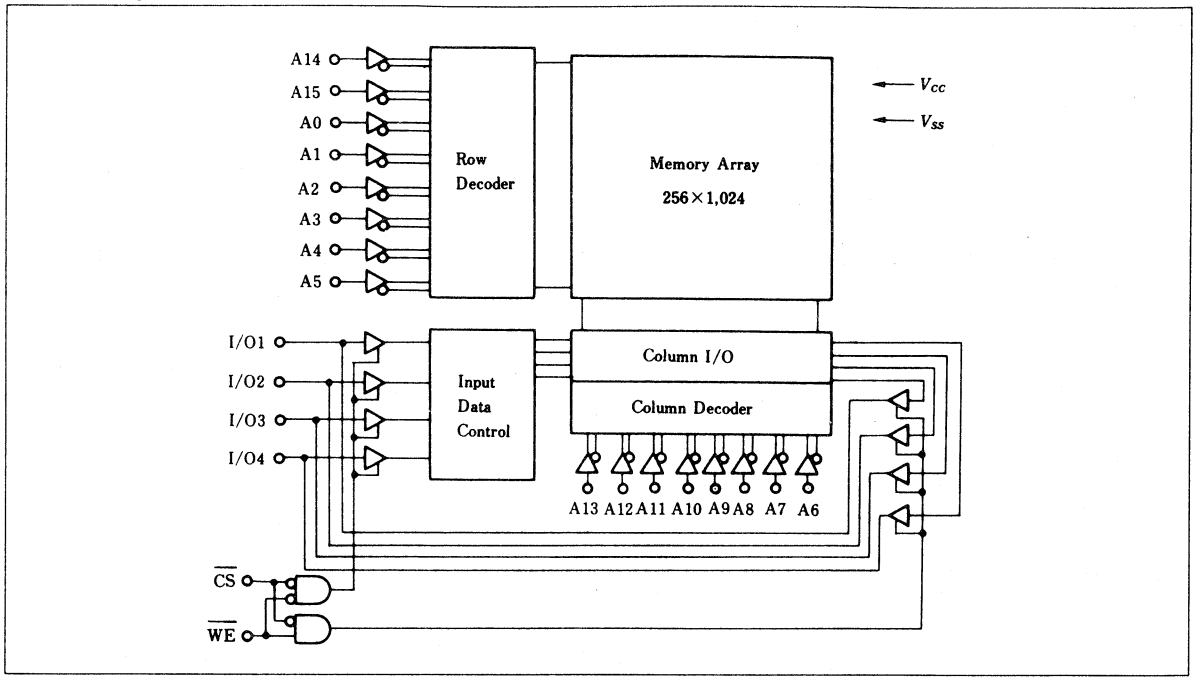


(Top View)

Pin Description

Pin Name	Function
A0 – A15	Address
I/O1 – I/O4	Input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	Vcc Current	I/O Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	Icc	Dout	Read cycle
L	L	Write	Icc	Din	Write cycle

Note: × means don't care.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	Vin	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C

Note: *1. Vin min = −2.5 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: *1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	HM6208H-25			HM6208H-35 HM6208H-45			Unit	Test Conditions	Note
		Min	Typ*1	Max	Min	Typ*1	Max			
Input leakage current	I_{LI}	—	—	2.0	—	—	2.0	µA	V_{CC}=Max Vin=Vss to V_{CC}	
Output leakage current	I_{LO}	—	—	10.0	—	—	10.0	µA	$\overline{CS}$=V_{IH} $V_{I/O}$=Vss to V_{CC}	
Operating power supply current	I_{CC}	—	60	120	—	50	100	mA	$\overline{CS}$=V_{IL}, $I_{I/O}$=0 mA Min cycle duty=100%	
	I_{CC1}	—	40	80	—	40	80	mA	$\overline{CS}$=V_{IL}, $I_{I/O}$=0 mA t_{cycle}=50 ns duty=100%	
Standby power supply current	I_{SB}	—	20	40	—	15	30	mA	$\overline{CS}$=V_{IH}, Min cycle	
Standby power supply current(1)	I_{SB1}	—	0.02	2.0	—	0.02	2.0	mA	$\overline{CS}$>V_{CC} -0.2 V 0 V≤Vin < 0.2 V or Vin≥V_{CC} -0.2 V	
		—	0.006	0.1	—	0.006	0.1			L-Version
Output low voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL}=8 mA	
Output high voltage	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH}=-4.0 mA	

Note: *1. Typical limits are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1MHz)*1

Item	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	C_{in}	—	6	pF	V_{in}=0 V
Input/output capacitance	$C_{I/O}$	—	11	pF	$V_{I/O}$=0 V

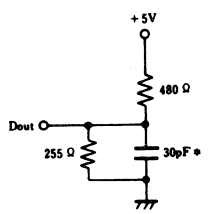
Note: *1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

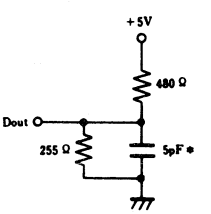
Test Conditions

- Input pulse levels: Vss to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels : 1.5 V
- Output load: See figures

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



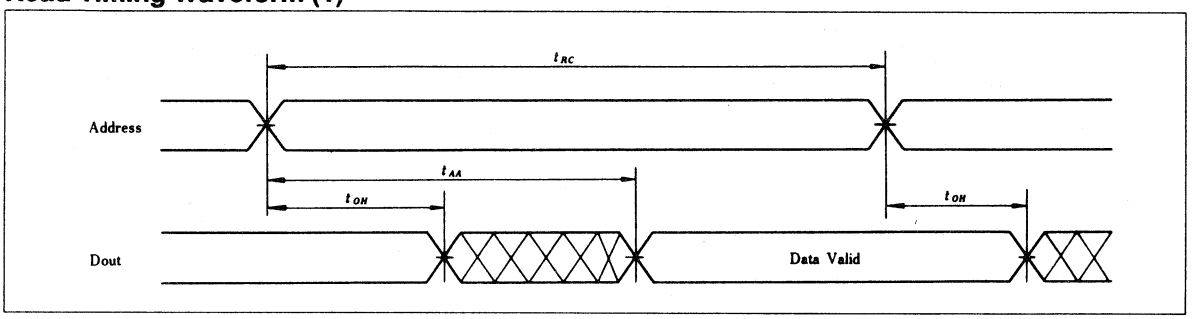
Note: * Including scope & jig.

Read cycle

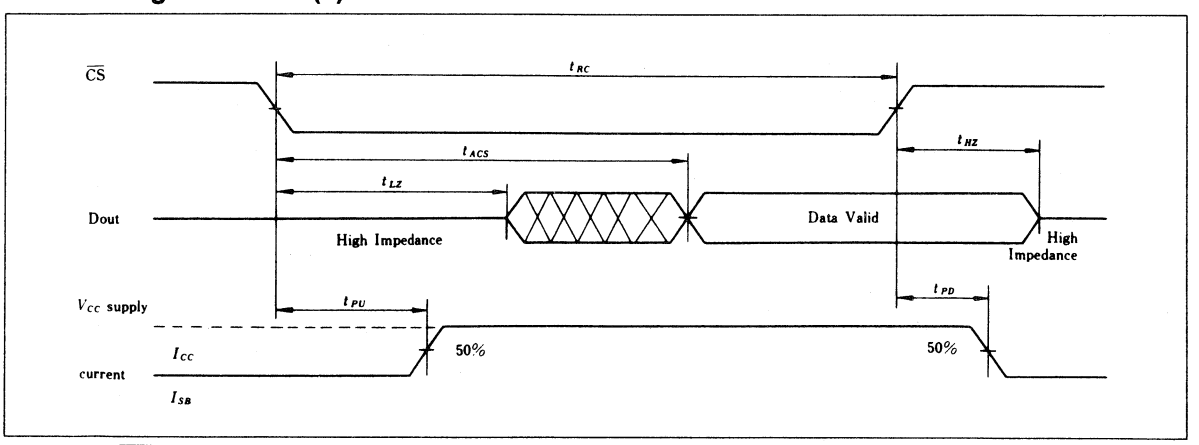
Item	Symbol	HM6208H-25		HM6208H-35		HM6208H-45		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	25	—	35	—	45	—	ns
Address access time	t_{AA}	—	25	—	35	—	45	ns
Chip select access time	t_{ACS}	—	25	—	35	—	45	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip selection to output in low-Z	t_{LZ}*1	5	—	5	—	5	—	ns
Chip deselection to output in high-Z	t_{HZ}*1	0	15	0	20	0	20	ns
Chip selection to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	15	—	25	—	30	ns

Note: *1 Transition is measured ±200 mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *3



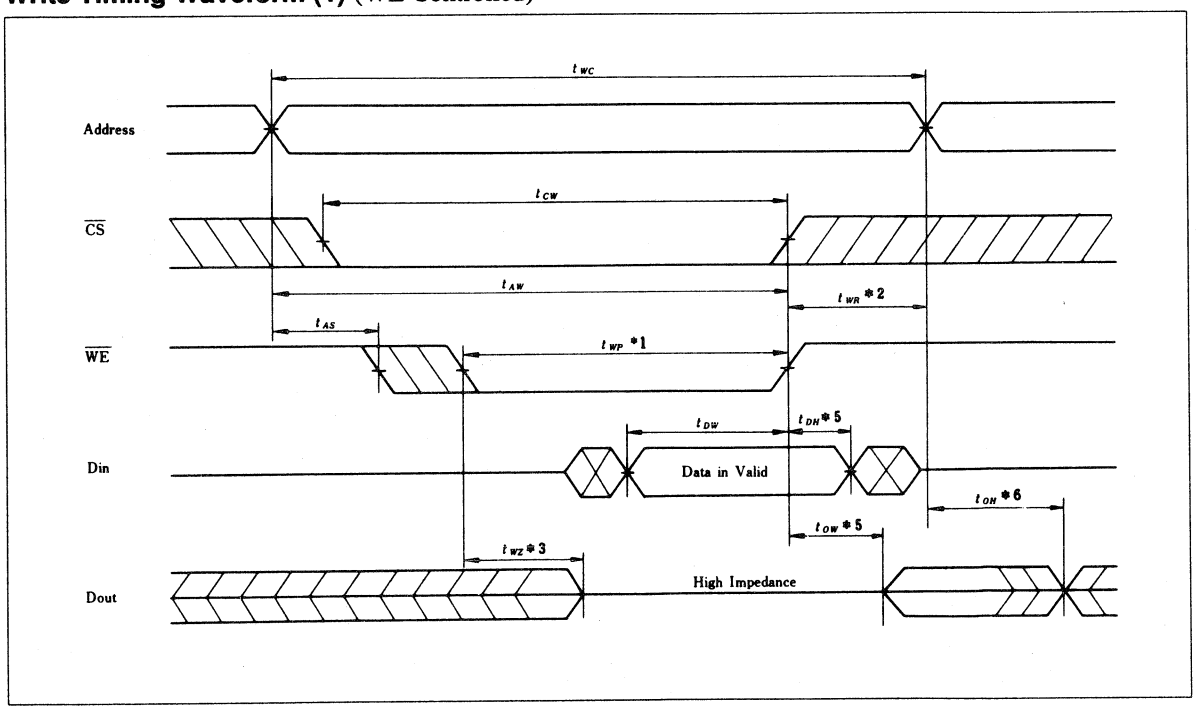
Notes: *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

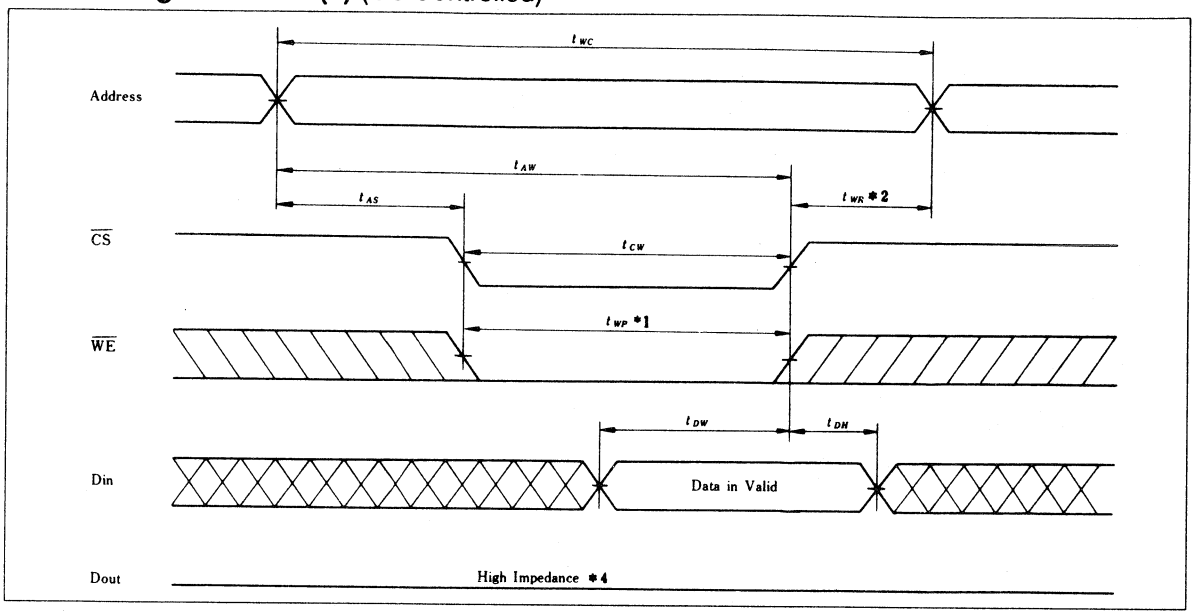
Item	Symbol	HM6208H-25		HM6208H-35		HM6208H-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write cycle time	twc	25	—	35	—	45	—	ns	
Chip selection to end of write	tcw	20	—	30	—	40	—	ns	
Address valid to end of write	taw	20	—	30	—	40	—	ns	
Address setup time	tas	0	—	0	—	0	—	ns	
Write pulse width	twp	20	—	25	—	30	—	ns	
Write recovery time	twr	3	—	3	—	3	—	ns	
Data valid to end of write	tdw	15	—	20	—	20	—	ns	
Data hold time	tdh	0	—	0	—	0	—	ns	
Write enabled to output in high-Z	twz*1	0	8	0	10	0	15	ns	
Output active from end of write	tow*1	0	—	0	—	0	—	ns	

Note: *1 Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes: *1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (tWP)
*2. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state. The input signals of the opposite phase to the outputs must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The data input signals of opposite phase to the outputs must not be applied to them.
*6. Dout is the same phase of write data of this write cycle.

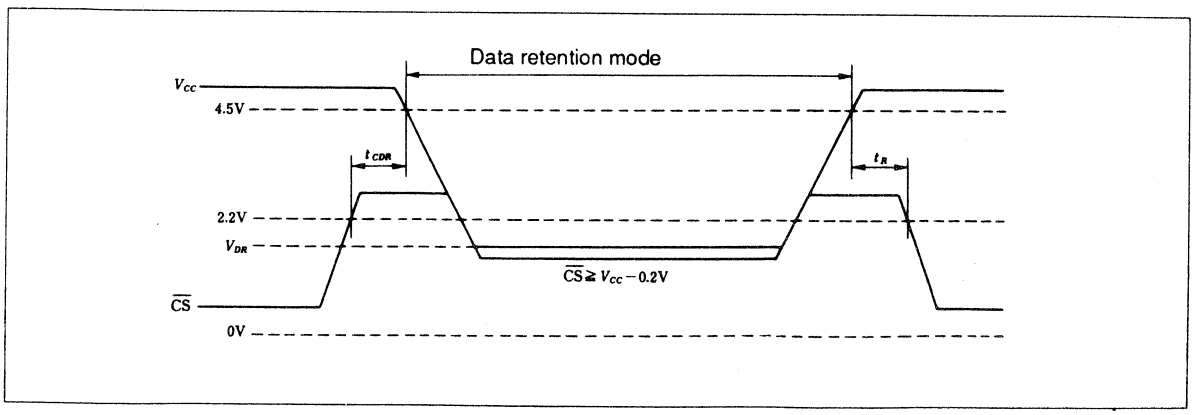
Low Vcc Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Vcc for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, Vin ≥ Vcc – 0.2 V or 0 V ≤ Vin ≤ 0.2 V
Data retention current	I_{CCDR}	—	2	50 *1	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

Note: *1. Vcc = 3.0 V.

Low Vcc Data Retention Timing Waveform



HM6708SH/HM6709SH Series

65,536-words × 4-bits High Speed Static Random Access Memory

Features

- 65,536 words × 4 bits organization
- Fully compatible with TTL input and output
- 0.8 µm Hi-BiCMOS process
- +5 V single power supply
- Completely static memory: No clock or timing strobe required
- Low power dissipation (DC) operating: 400 mW typ
- Super fast access time: 10/12 ns max

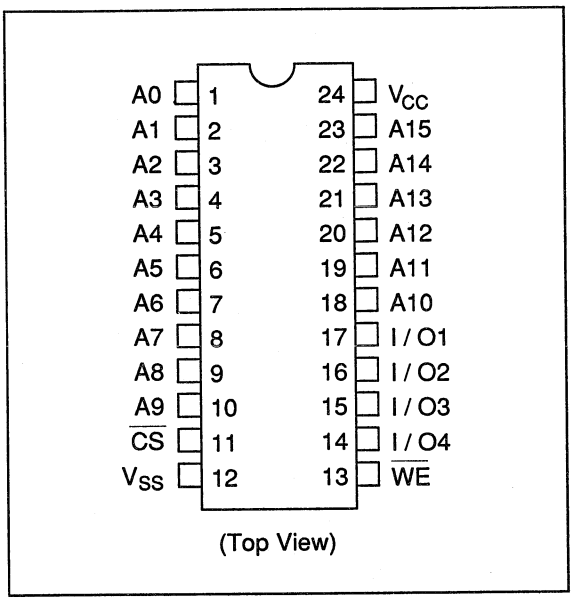
Ordering Information

Type No.	Access Time	Package
HM6708SHJP-10	10 ns	300-mil 24-pin plastic SOJ (CP-24D)
HM6708SHJP-12	12 ns	
HM6709SHJP-10	10 ns	300-mil 24-pin plastic SOJ (CP-28DN)
HM6709SHJP-12	12 ns	

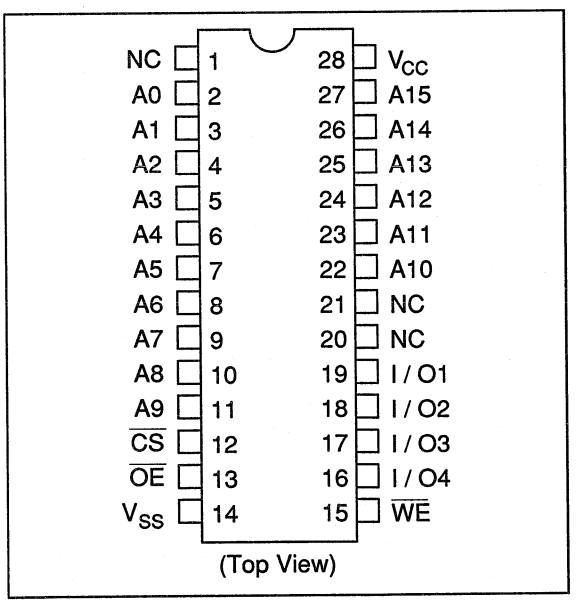
Pin Description

Pin Name	Function
A0–A15	Address input
I/O1–I/O4	Data input/output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
$\overline{OE}$ (for HM6709SH only)	Output enable
V_{SS}	Ground
V_{CC}	Power supply
NC	No connection

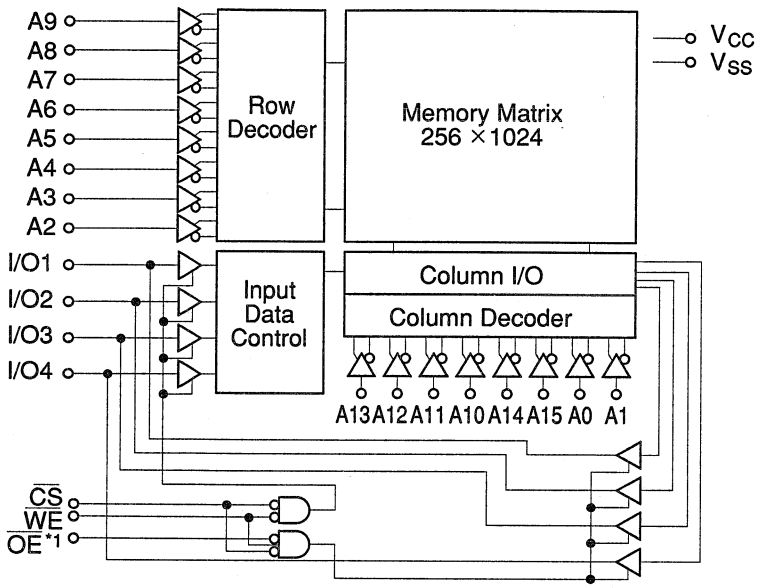
Pin Arrangement (HM6708SH Series)



Pin Arrangement (HM6709SH Series)



Block Diagram



Note: 1. HM6709SH only

Function Table (HM6708SH)

Input					
$\overline{CS}$	$\overline{WE}$	Mode	I/O Pin	V_{CC} Current	Reference Cycle
H	X	Not selected	High Z	I_{SB}, I_{SB1}	—
L	H	Write "0"	Dout	I_{CC}, I_{CC1}	Read cycle (2), (3)
L	L	Write "1"	High Z	I_{CC}, I_{CC1}	Write cycle (1), (2)

Function Table (HM6709SH)

Input						
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Reference Cycle
H	X	X	Not selected	High Z	I_{SB}, I_{SB1}	—
L	H	H	Output disable	High Z	I_{CC}, I_{CC1}	—
L	H	L	Read	Data out	I_{CC}, I_{CC1}	Read cycle (1), (2), (3)
L	L	H	Write	Data in	I_{CC}, I_{CC1}	Write cycle (1), (2), (3), (4)
L	L	L	Write	Data in	I_{CC}, I_{CC1}	Write cycle (5), (6)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage with respect to V_{SS} pin	V_{CC}	–0.5 to +7.0	V
Terminal voltage with respect to V_{SS} pin	V_T	–0.5 to V_{CC} +0.5	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range (with bias)	Tstg (Bias)	–10 to +85	°C
Storage temperature range	T_{stg}	–55 to +125	°C

For the AC and DC specifications shown in these tables, the devices were tested with a minimum transverse air flow exceeding 500 linear feet per minute.

Recommended DC Operating Conditions (0°C≤ Ta ≤ 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input low voltage	V_{IL}	–3.0[1)]	—	0.8	V

Note: 1) Pulse width 10 ns, DC: –0.5 V

Electrical Characteristics

DC Characteristics (V_{CC} = 5.0 V ± 10%, Ta = 0 to +70°C)

		–10			–12				
Item	Symbol	Min	Typ[1)]	Max	Min	Typ[1)]	Max	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2	—	—	2	µA	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	10	—	—	10	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$=V_{IH}, $\overline{WE}$ = V_{IL}, $V_{I/O}$ = 0 V to V_{CC}
Operating power supply current	I_{CC}	—	60	100	—	60	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA
Average operating current	I_{CC1}	—	130	180	—	120	175	mA	Min. cycle, $I_{I/O}$ = 0 mA
Standby power supply current	I_{SB}	—	—	40	—	—	40	mA	$\overline{CS}$ =V_{IH}, V_{IN} = V_{IH} or V_{IL}
	I_{SB1}	—	—	30	—	—	30	mA	$\overline{CS}$ ≥ V_{CC} –0.2 V, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V
Output low voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH} = –4 mA

Note: 1) Typical limits are: V_{CC} = 5.0 V, Ta = 25°C, and specified loading.

Capacitance (Ta = 25°C, f = 1 MHz)

Item	Symbol	Max	Unit	Test Condition
Input capacitance	C_{in}[1)]	6	pF	Vin = 0 V
Output capacitance	$C_{I/O}$[1)]	10	pF	$V_{I/O}$ = 0 V

Note: 1) This parameter is sampled and is not 100% tested.

AC Characteristics (V_{CC} = 5 V ± 10%, Ta = 0°C to +70°C unless otherwise noted)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5 V
- Output load: See figure 1
- Input rise and fall times: 4 ns
- Output reference levels: 1.5 V

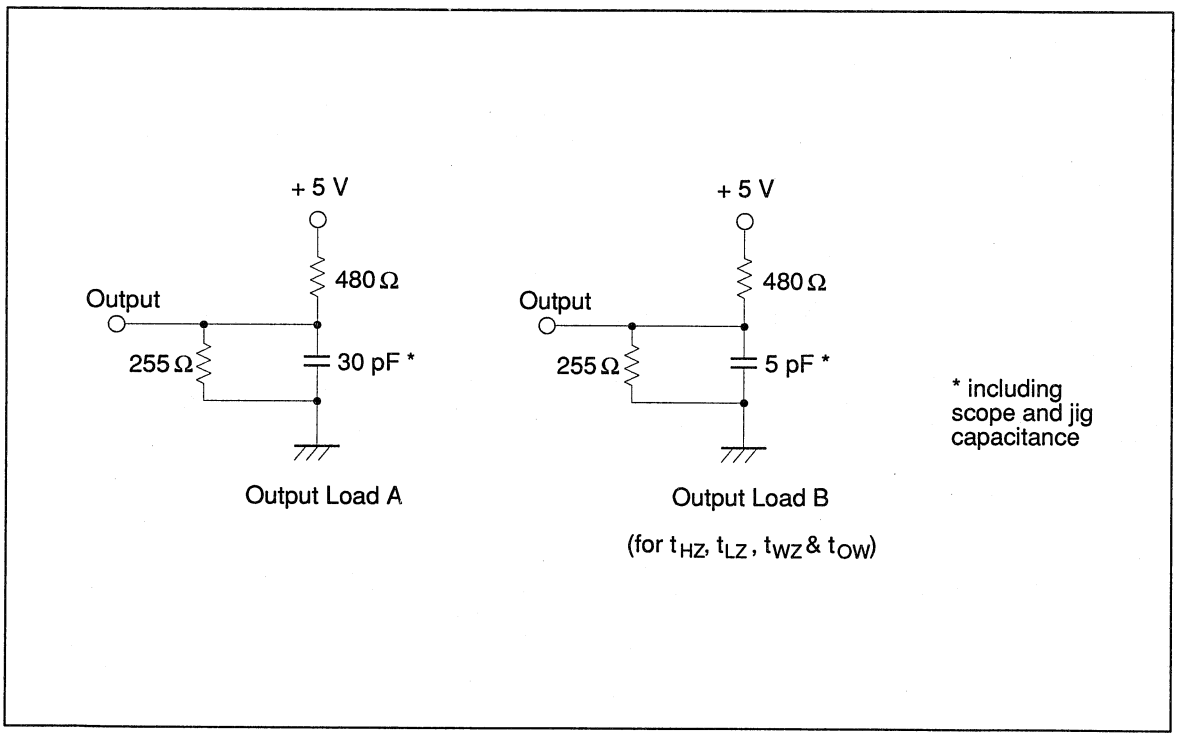


Figure 1 Output Load

Read Cycle

Item	Symbol	–10 Min	–10 Max	–12 Min	–12 Max	Unit
Read cycle time	t_{RC}	10	—	12	—	ns
Address access time	t_{AA}	—	10	—	12	ns
Chip select access time	t_{ACS}	—	10	—	12	ns
Chip selection to output in low Z	t_{LZ}[1) 2)]	3	—	3	—	ns
Output enable to output valid	t_{OE}[3)]	—	5	—	6	ns
Output enable to output in low Z	t_{OLZ}[1) 2) 3)]	0	—	0	—	ns
Chip deselection to output in high Z	t_{HZ}[1) 2)]	0	5	0	5	ns
Output hold from address change	t_{OH}	3	—	3	—	ns

Notes: 1) This parameter is sampled and is not 100% tested.

2) Transition is measured ±200 mV from steady state voltage with loading specified in figure 1, load (B).

3) These parameters are for HM6709SH.

Write Cycle

Item	Symbol	–10 Min	–10 Max	–12 Min	–12 Max	Unit
Write cycle time	t_{WC}[1)]	10	—	12	—	ns
Chip selection to end of write	t_{CW}	8	—	9	—	ns
Address valid to end of write	t_{AW}	10	—	11	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	8	—	9	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Data valid to end of write	t_{DW}	6	—	6	—	ns
Data hold time	t_{DH}	0	—	0	—	ns
Write enable to output in high Z	t_{WZ}[2) 3)]	0	5	0	6	ns
Output disable to output in high Z	t_{OHZ}[2) 3) 4)]	0	6	0	6	ns
Output active from end of write	t_{OW}[2) 3)]	3	—	3	—	ns

Notes: 1) All write cycle timings are referenced from the last valid address to the first transitioning address.

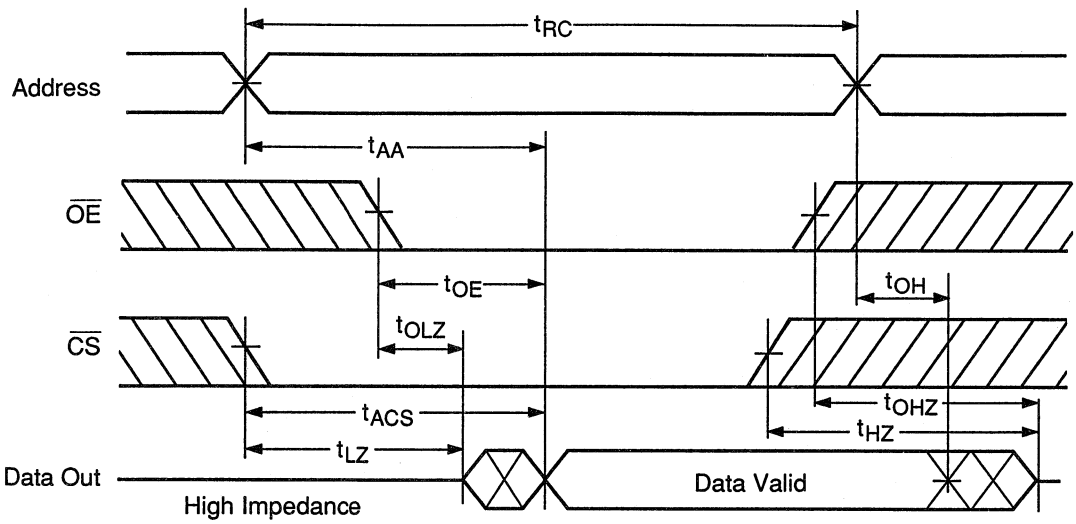
2) This parameter is sampled and is not 100% tested.

3) Transition is measured ±200 mV from steady state voltage with loading specified in figure 1, load (B).

4) These parameters are for HM6709SH.

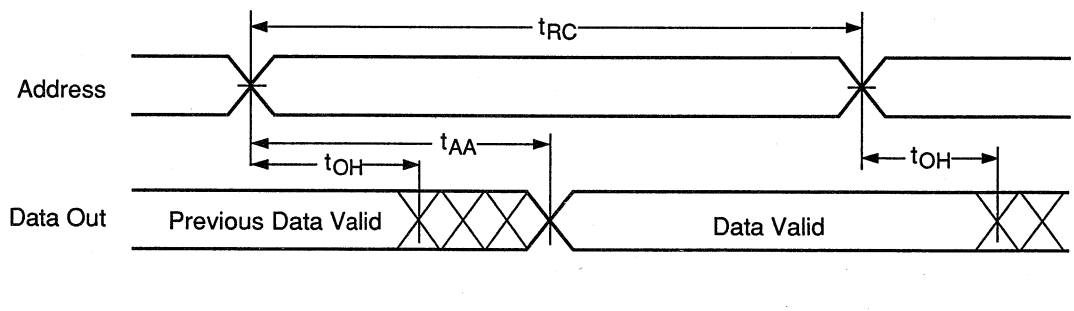
Timing Waveforms

Read Cycle 1



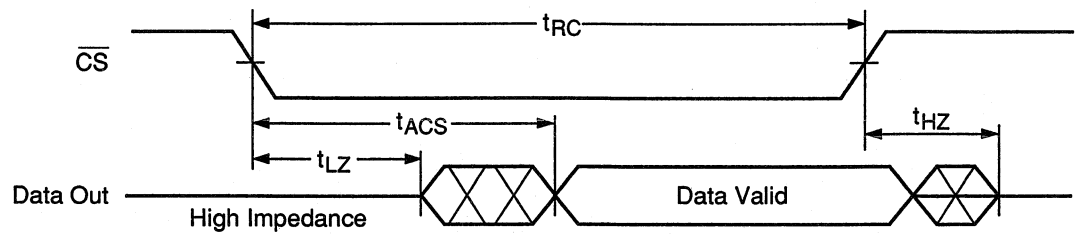
Note: 1. $\overline{WE} = V_{IH}$

Read Cycle 2



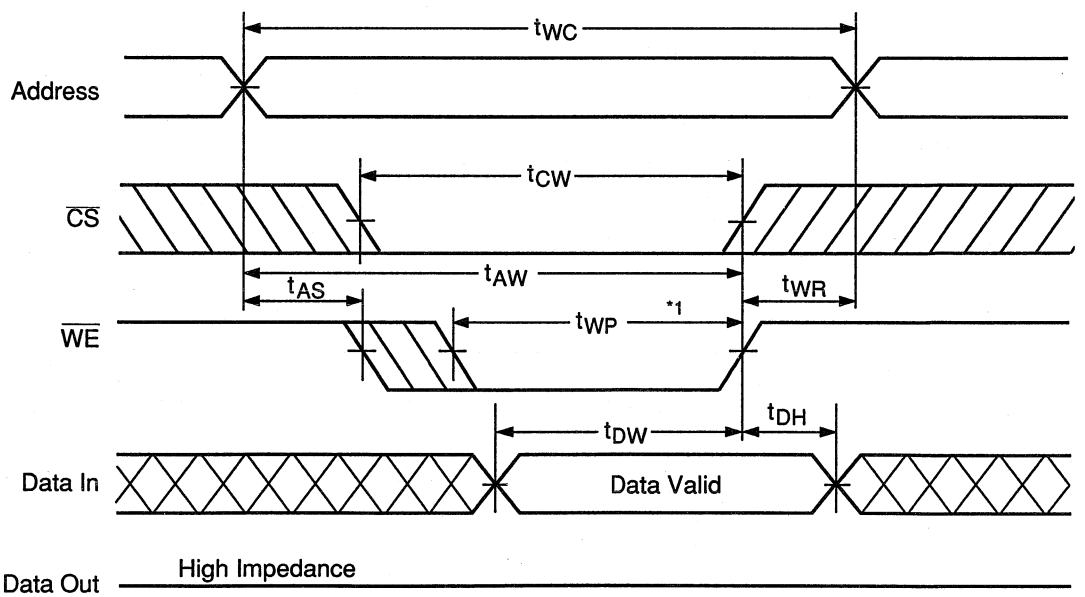
Notes: 1. $\overline{WE} = V_{IH}$
2. $\overline{CS} = V_{IL}$
3. $\overline{OE} = V_{IL}$

Read Cycle 3



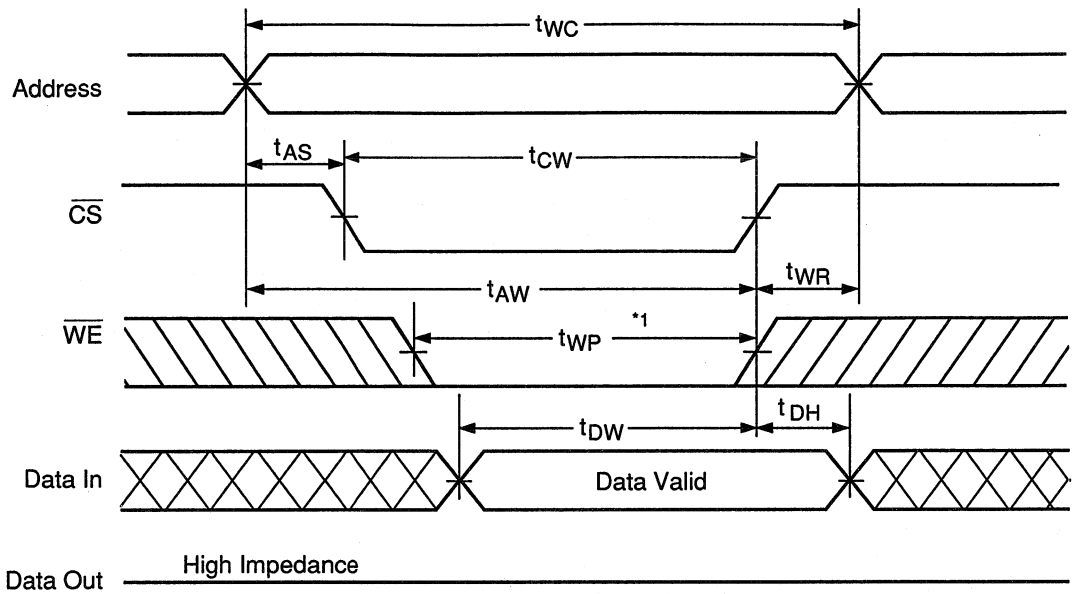
Notes: 1. $\overline{WE} = V_{IH}$
2. $\overline{OE} = V_{IL}$
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle 1 ($\overline{OE}$ = H, $\overline{WE}$ controlled)



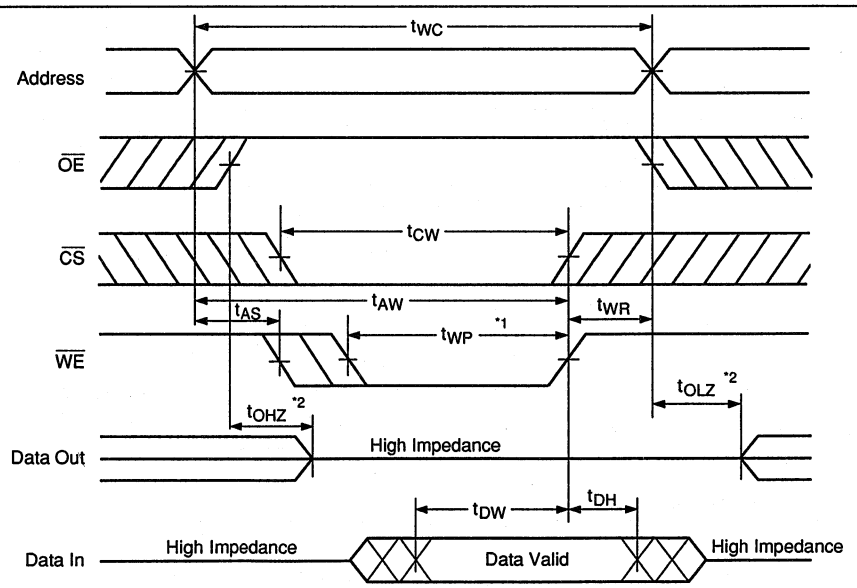
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle 2 ($\overline{OE}$ = H, $\overline{CS}$ controlled)



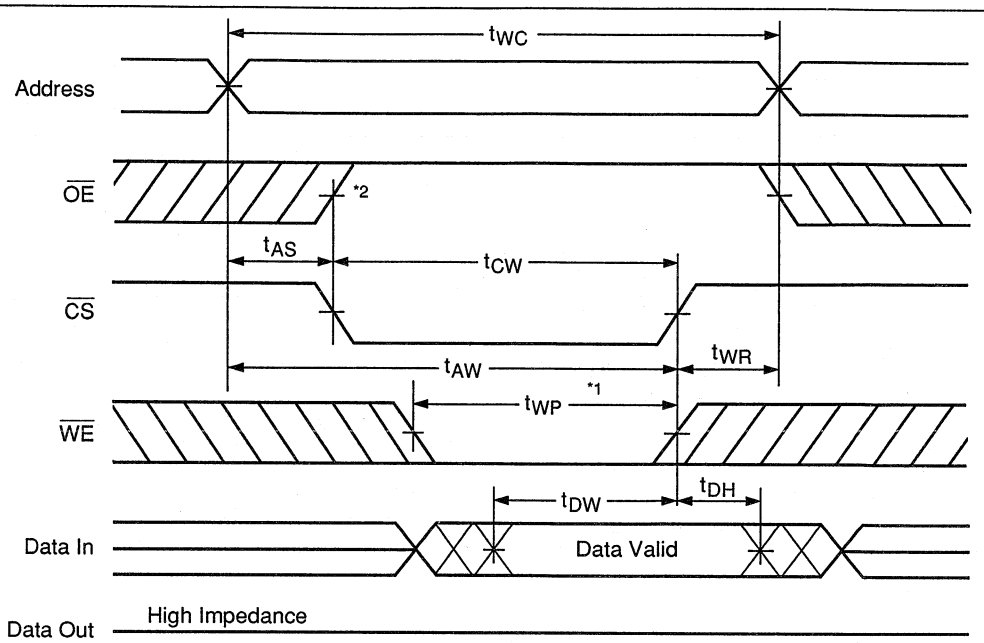
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle 3 ($\overline{OE}$ = clocked, $\overline{WE}$ controlled)



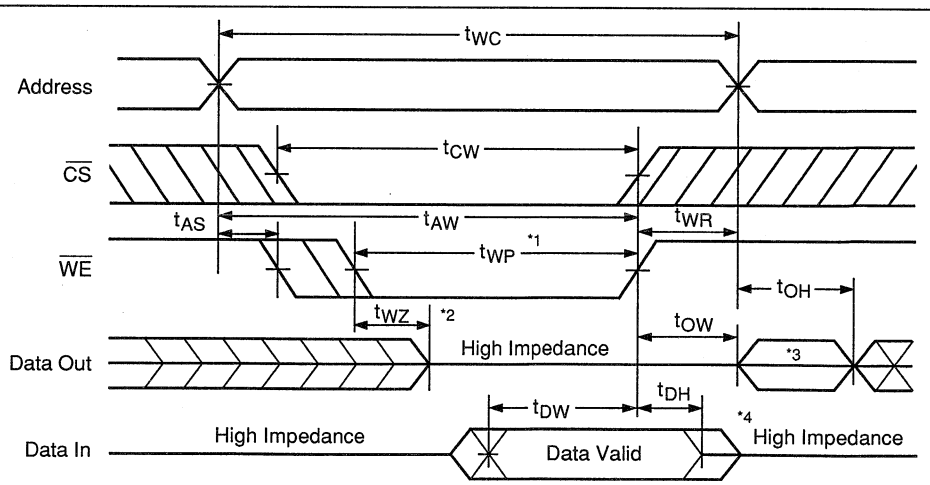
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

Write Cycle 4 ($\overline{OE}$ = clocked, $\overline{CS}$ controlled)



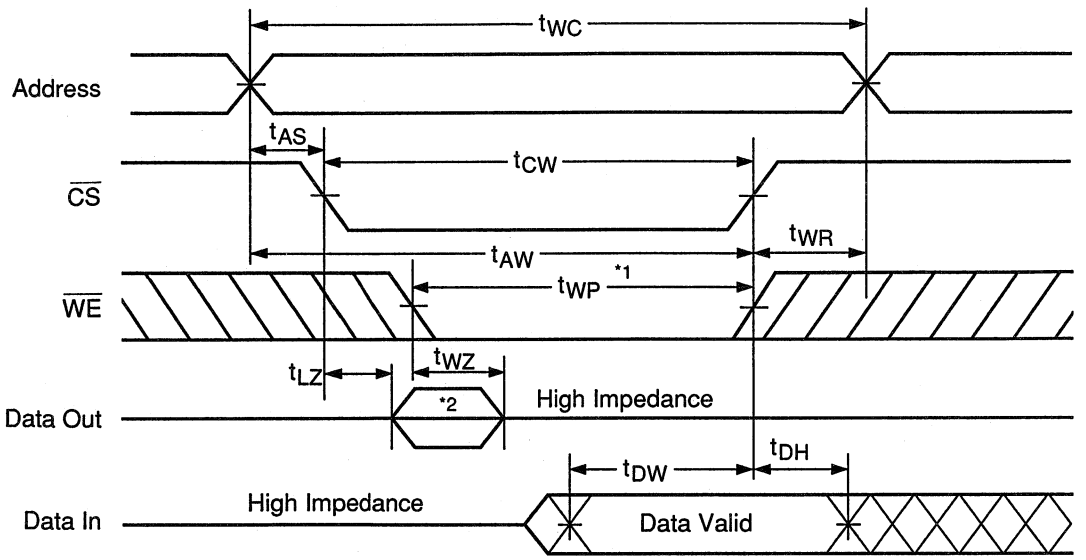
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in a high impedance state.

Write Cycle 5 ($\overline{OE}$ = L, $\overline{WE}$ controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. During this period, I/O pins are output state so that the input signals of opposite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.

Write Cycle 6 ($\overline{OE}$ = L, $\overline{CS}$ controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.

HM6708A Series

65536-word × 4-bit High Speed Static Random Access Memory

Features

- 65536-word × 4 bit organization
- Fully TTL compatible input and output
- 1.0 µm Hi-BiCMOS process
- +5 V single supply
- Completely static memory
  No clock or timing strobe required
- Low power dissipation
  Operation: 450 mW typ
- Super fast
  Access time: 15/20 ns (max)

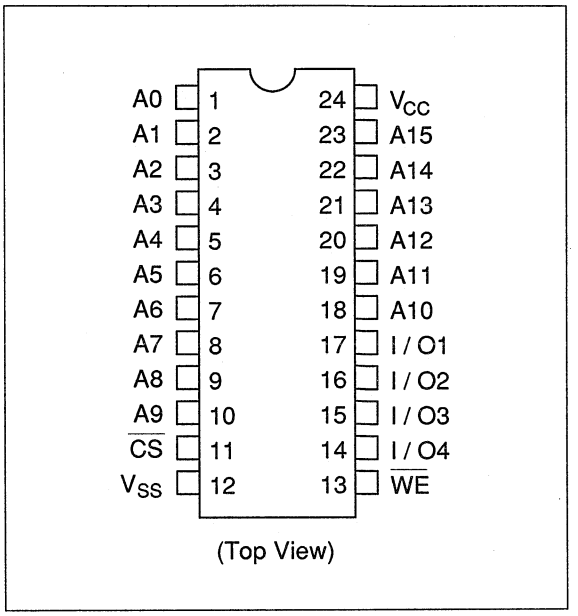
Ordering Information

Type No.	Access time	Package
HM6708AP-15	15 ns	300-mil 24-pin plastic DIP (DP-24NC)
HM6708AP-20	20 ns	
HM6708AJP-15	15 ns	300-mil 24-pin plastic SOJ (CP-24D)
HM6708AJP-20	20 ns	

Pin Description

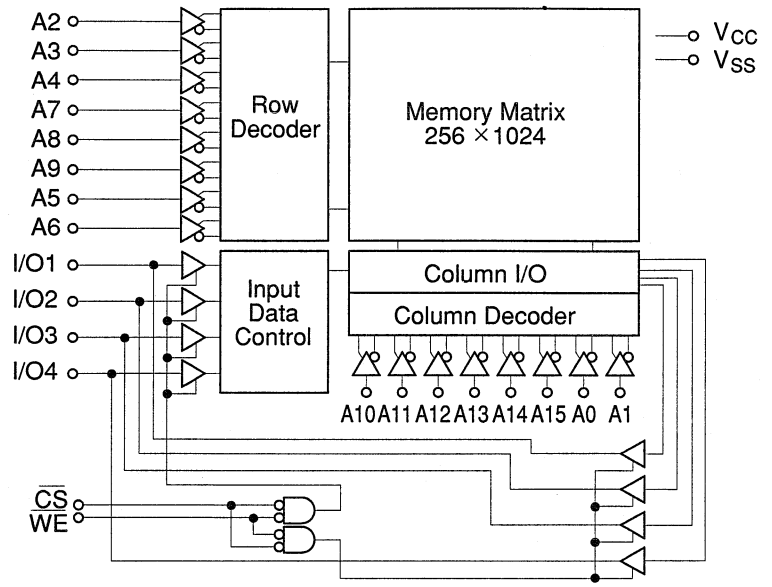
Pin name	Function
A0 – A15	Address input
I/O1 – I/O4	Data input/output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{SS}	Ground
V_{CC}	Power supply

Pin Arrangement



(Top View)

Block Diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	I/O pin	V_{CC} current	Ref. cycle
H	X	Not selected	High-Z	I_{SB}, I_{SB1}	—
L	H	Read	Data out	I_{CC}, I_{CC1}	Read cycle (1), (2)
L	L	Write	Data in	I_{CC}, I_{CC1}	Write cycle (1), (2)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage to V_{SS} pin	V_T	–0.5 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range (with bias)	Tstg (Bias)	–10 to +85	°C
Storage temperature range	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input high voltage	V_{IH}	2.2	—	V_{CC} +0.5	V
Input low voltage	V_{IL}	–3.0*1	—	0.8	V

Note: 1. Pulse width 15 ns, DC : –0.5 V

DC Characteristics (V_{CC} = 5.0 V ± 10%, Ta = 0 to +70°C)

Item	Symbol	HM6708A-15 Min	HM6708A-15 Typ	HM6708A-15 Max	HM6708A-20 Min	HM6708A-20 Typ	HM6708A-20 Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	2	—	—	2	µA	V_{CC} = 5.5 V, Vin = 0 V to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	10	—	—	10	µA	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = 0 V to V_{CC}
Operating power supply current	I_{CC}	—	—	100	—	—	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA
Average operating current	I_{CC1}	—	—	140	—	—	120	mA	min. cycle, Duty: 100%, $I_{I/O}$ = 0 mA
Standby power supply current	I_{SB}	—	—	30	—	—	30	mA	$\overline{CS}$ = V_{IH}, Vin = V_{IH} or V_{IL}
	I_{SB1}	—	—	10	—	—	10	mA	$\overline{CS}$ ≥ V_{CC} –0.2 V, Vin ≤ 0.2 V or Vin ≥ V_{CC} –0.2 V
Output low voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH} = –4 mA

Capacitance (Ta = 25°C, f = 1 MHz)

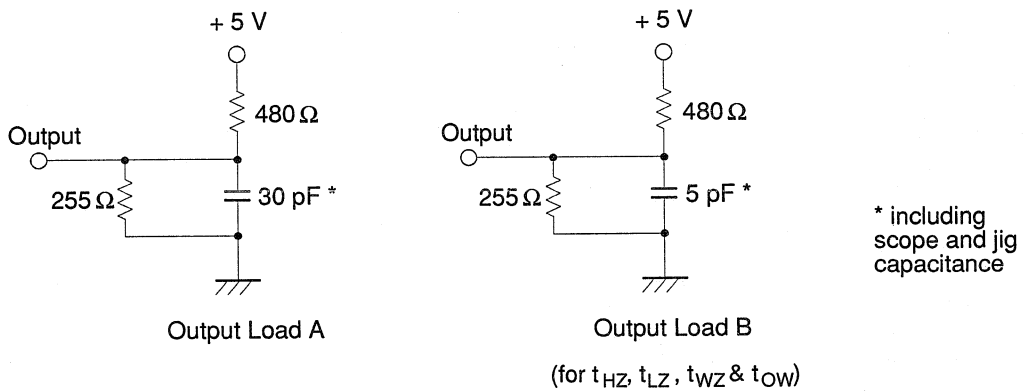
Item	Symbol	Max	Unit	Test condition
Input capacitance	C_{in}*1	6	pF	Vin = 0 V
Output capacitance	$C_{I/O}$*1	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC} = 5 V ± 10%, Ta = 0°C to +70°C unless otherwise noted)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5 V
- Output load: See figures
- Input rise and fall times: 4 ns
- Output reference levels: 1.5 V



Output Load A

Output Load B

(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

Read Cycle

Item	Symbol	HM6708A-15 Min	HM6708A-15 Max	HM6708A-20 Min	HM6708A-20 Max	Unit
Read cycle time	t_{RC}	15	—	20	—	ns
Address access time	t_{AA}	—	15	—	20	ns
Chip select access time	t_{ACS}	—	15	—	20	ns
Output hold from address change	t_{OH}	4	—	5	—	ns
Chip selection to output in low-Z	t_{LZ}*1, *2	4	—	5	—	ns
Chip deselection to output in high-Z	t_{HZ}*1, *2	0	6	0	8	ns

Notes: 1. This parameter is sampled and not 100% tested.
2. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).

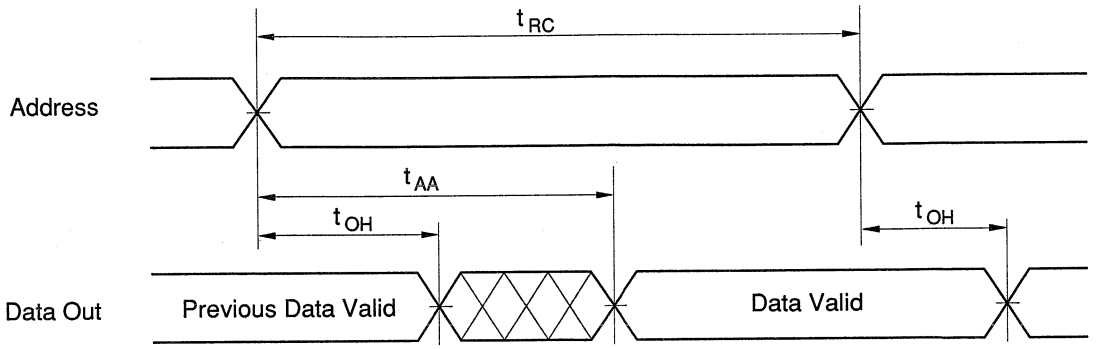
Write Cycle

Item	Symbol	HM6708A-15		HM6708A-20		Unit
		Min	Max	Min	Max	
Write cycle time	t_{WC} *1	15	—	20	—	ns
Chip selection to end of write	t_{CW}	10	—	15	—	ns
Address valid to end of write	t_{AW}	10	—	15	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	10	—	15	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Data valid to end of write	t_{DW}	8	—	10	—	ns
Data hold time	t_{DH}	0	—	0	—	ns
Write enable to output in high-Z	t_{WZ} *2, *3	0	6	0	8	ns
Output active from end of write	t_{OW} *2, *3	0	—	0	—	ns

Notes: 1. All write cycle timings are referenced from the last valid address to the first transitioning address.
2. This parameter is sampled and not 100% tested.
3. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).

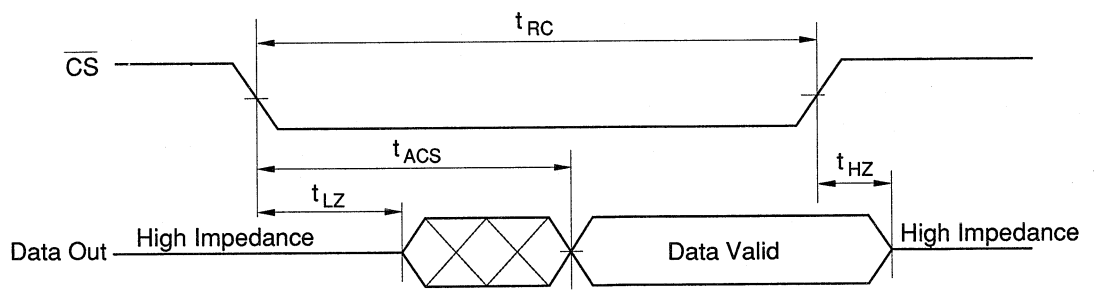
Timing Waveforms

Read Cycle (1) *1, *2



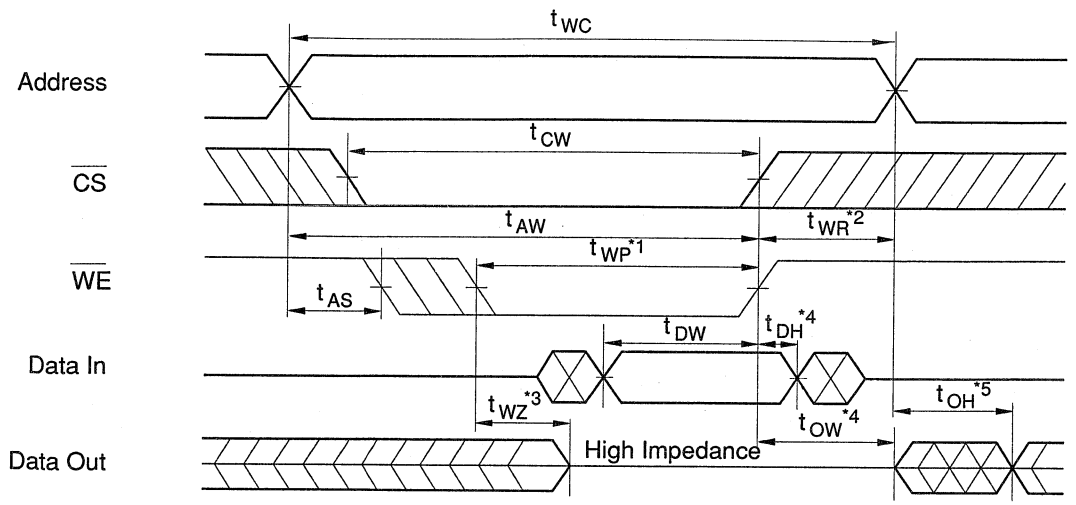
Notes : 1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.

Read Cycle (2) *1, *2



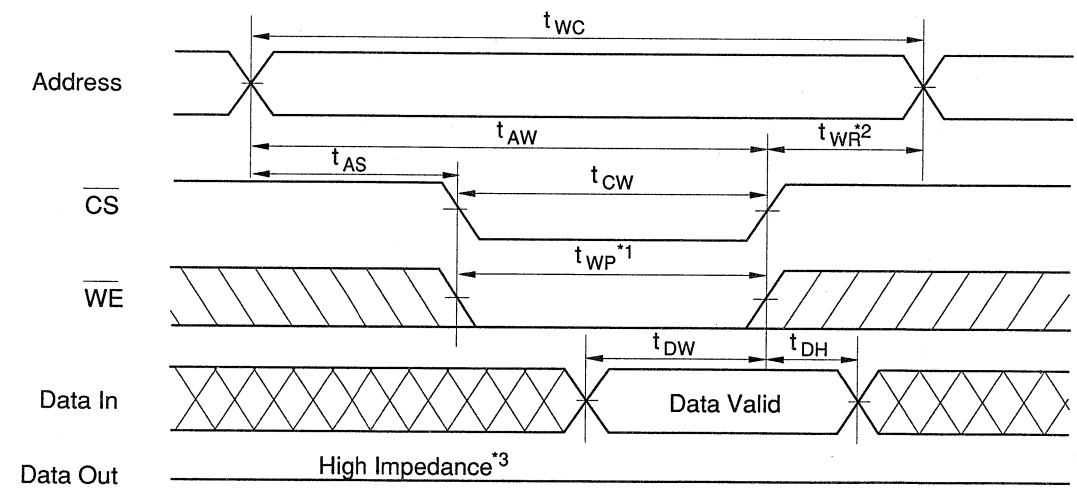
Notes : 1. $\overline{WE}$ is high for read cycle.
2. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle (1) *1, *2, *3, *4, *5 ($\overline{WE}$ Controlled)



Notes : 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I / O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If $\overline{CS}$ is low during this period, I / O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
5. Output data is the same phase of write data of this write cycle.

Write Cycle (2) *1, *2, *3 ($\overline{CS}$ Controlled)



Notes : 1. Awrite occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high inpedance state.

HM6207H Series

262144-Word × 1-Bit High Speed CMOS Static RAM

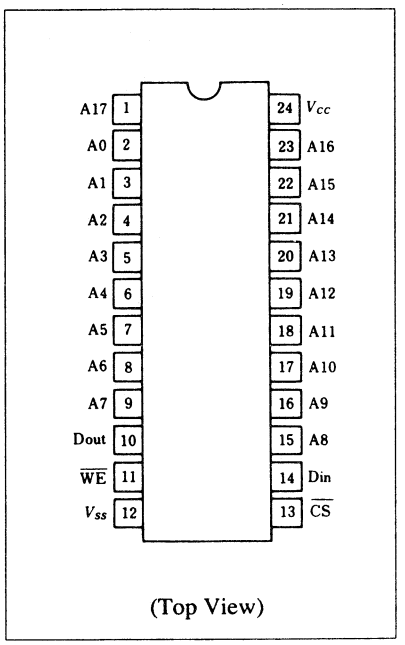
Features

- Single 5 V supply and high density 24-pin package
- High speed
  - Access time: 25/35/45 ns (max)
- Low power
  - Operation: 300 mW (typ)
  - Standby: 100 µW (typ)
  - 30 µW (typ) (L-version)
- Completely static memory required
  - No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible
  - All inputs and outputs
- Capability of battery back up operation (L-version)

Ordering Information

Type No.	Access Time	Package
HM6207HP-25	25 ns	300-mil 24-pin Plastic DIP (DP-24NC)
HM6207HP-35	35 ns	
HM6207HP-45	45 ns	
HM6207HLP-25	25 ns	
HM6207HLP-35	35 ns	
HM6207HLP-45	45 ns	
HM6207HJP-25	25 ns	300-mil 24-pin SOJ (CP-24D)
HM6207HJP-35	35 ns	
HM6207HJP-45	45 ns	
HM6207HLJP-25	25 ns	
HM6207HLJP-35	35 ns	
HM6207HLJP-45	45 ns	

Pin Arrangement

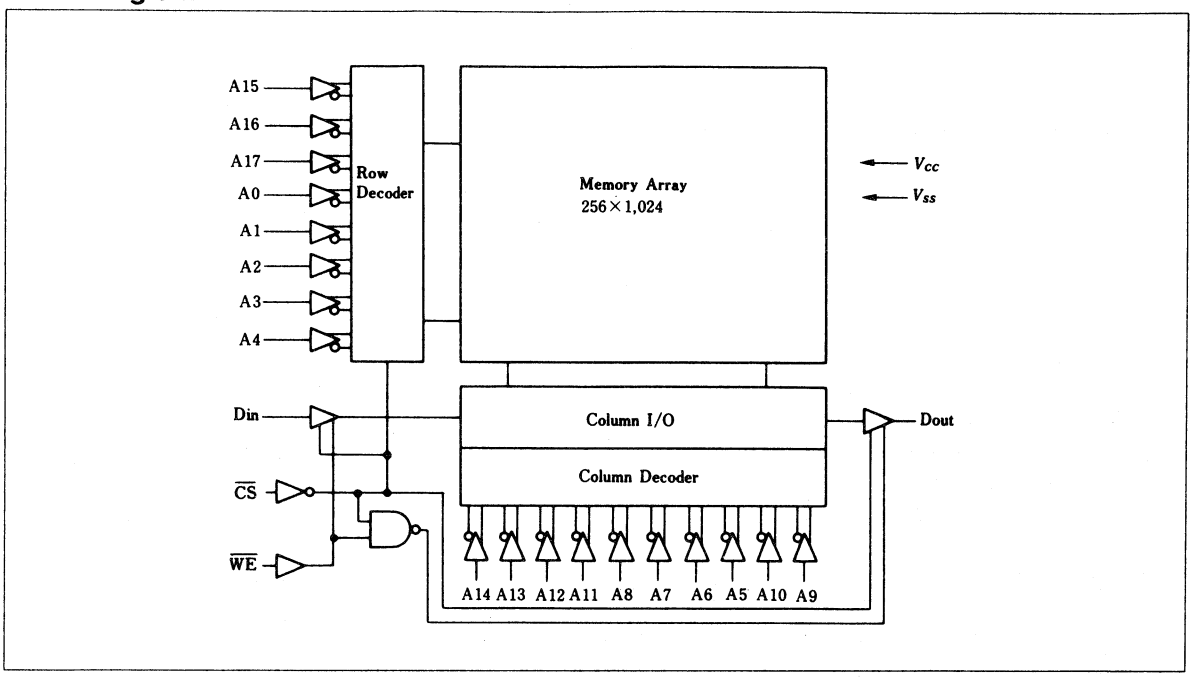


(Top View)

Pin Description

Pin Name	Function
A0 – A17	Address
Din	Data input
Dout	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	Vcc Current	I/O Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	Icc	Dout	Read cycle
L	L	Write	Icc	High-Z	Write cycle

Note: × means don't care.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	Vin	–0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–10 to +85	°C

Note: *1. Vin min = –2.5 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: *1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	HM6207H-25			HM6207H-35 HM6207H-45			Unit	Test Conditions	Note
		Min	Typ*1	Max	Min	Typ*1	Max			
Input leakage current	I_{LI}	—	—	2.0	—	—	2.0	µA	V_{CC}=Max Vin=Vss to V_{CC}	
Output leakage current	I_{LO}	—	—	10.0	—	—	10.0	µA	$\overline{CS}$=V_{IH} $V_{I/O}$=Vss to V_{CC}	
Operating power supply current	I_{CC}	—	60	120	—	50	100	mA	$\overline{CS}$=V_{IL}, $I_{I/O}$=0 mA Min cycle duty=100%	
	I_{CC1}	—	40	80	—	40	80	mA	$\overline{CS}$=V_{IL}, $I_{I/O}$=0 mA tcycle=50 ns duty=100%	
Standby power supply current	I_{SB}	—	20	40	—	15	30	mA	$\overline{CS}$=V_{IH}, Min cycle	
Standby power supply current(1)	I_{SB1}	—	0.02	2.0	—	0.02	2.0	mA	$\overline{CS}$>V_{CC} -0.2 V 0 V≤Vin< 0.2 V or Vin≥V_{CC} -0.2 V	
		—	0.006	0.1	—	0.006	0.1			L-Version
Output low voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL}=8 mA	
Output high voltage	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH}=-4.0 mA	

Note: *1. Typical limits are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1MHz)*1

Item	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	Cin	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	10	pF	Vout = 0 V

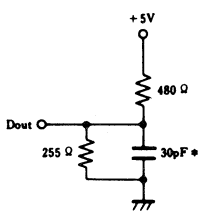
Note: *1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

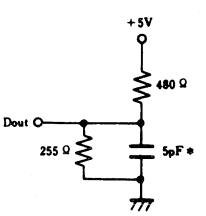
- Input pulse levels: Vss to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels : 1.5 V
- Output load: See figures

Output Load (A)



Output Load (B)

(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



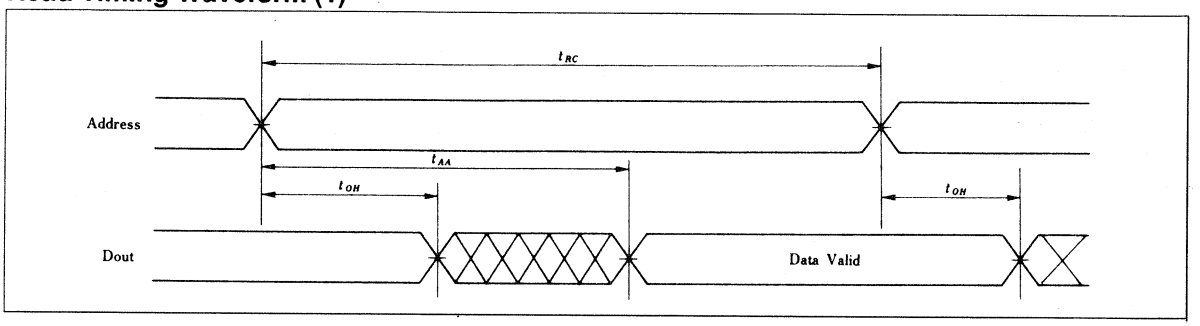
Note: * Including scope & jig.

Read cycle

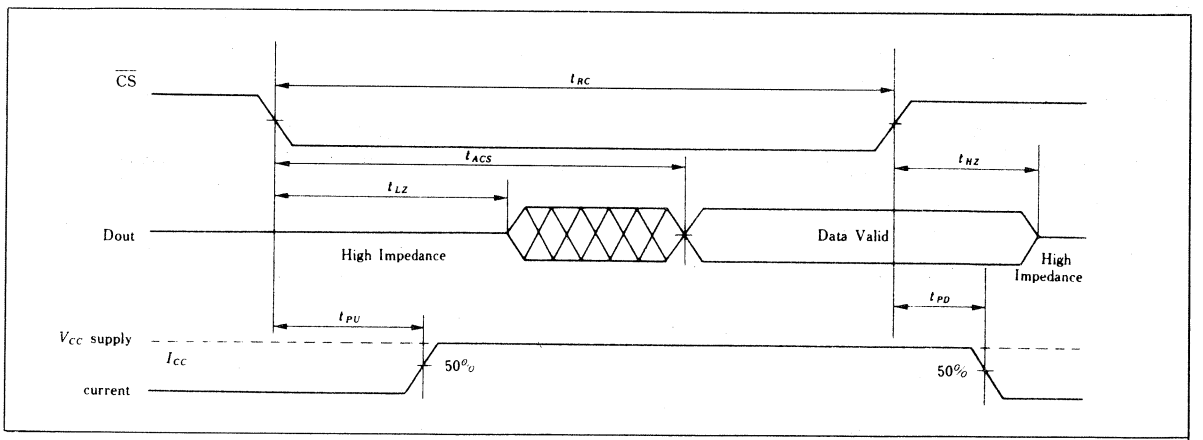
Item	Symbol	HM6207H-25		HM6207H-35		HM6207H-45		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	25	—	35	—	45	—	ns
Address access time	t_{AA}	—	25	—	35	—	45	ns
Chip select access time	t_{ACS}	—	25	—	35	—	45	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip selection to output in low-Z	t_{LZ*1}	5	—	5	—	5	—	ns
Chip deselection to output in high-Z	t_{HZ*1}	0	15	0	20	0	20	ns
Chip selection to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	15	—	25	—	30	ns

Note: *1 Transition is measured ±200 mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *3



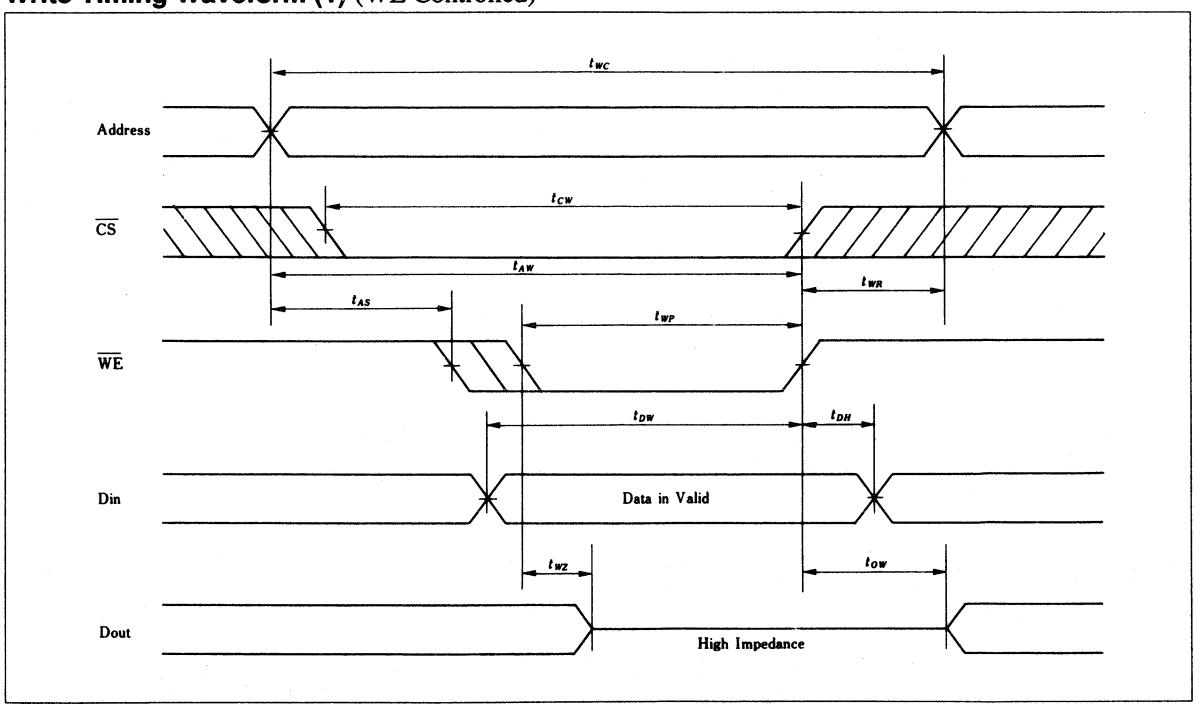
Notes: *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

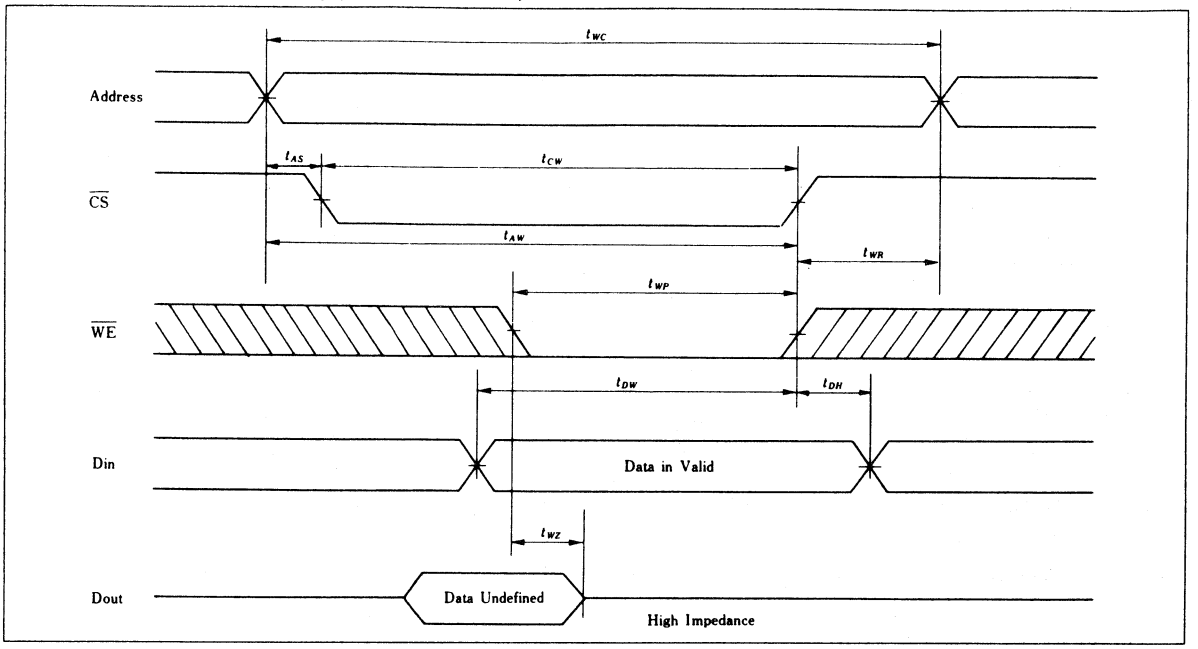
Item	Symbol	HM6207H-25		HM6207H-35		HM6207H-45		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	t_{WC}	25	—	35	—	45	—	ns
Chip selection to end of write	t_{CW}	20	—	30	—	40	—	ns
Address valid to end of write	t_{AW}	20	—	30	—	40	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	25	—	25	—	ns
Write recovery time	t_{WR}	3	—	3	—	3	—	ns
Data valid to end of write	t_{DW}	15	—	20	—	20	—	ns
Data hold time	t_{DH}	0	—	0	—	0	—	ns
Write enabled to output in high-Z	t_{WZ}*1	0	15	0	20	0	25	ns
Output active from end of write	t_{OW}*1	0	—	0	—	0	—	ns

Note: *1 Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes: *1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
*4. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

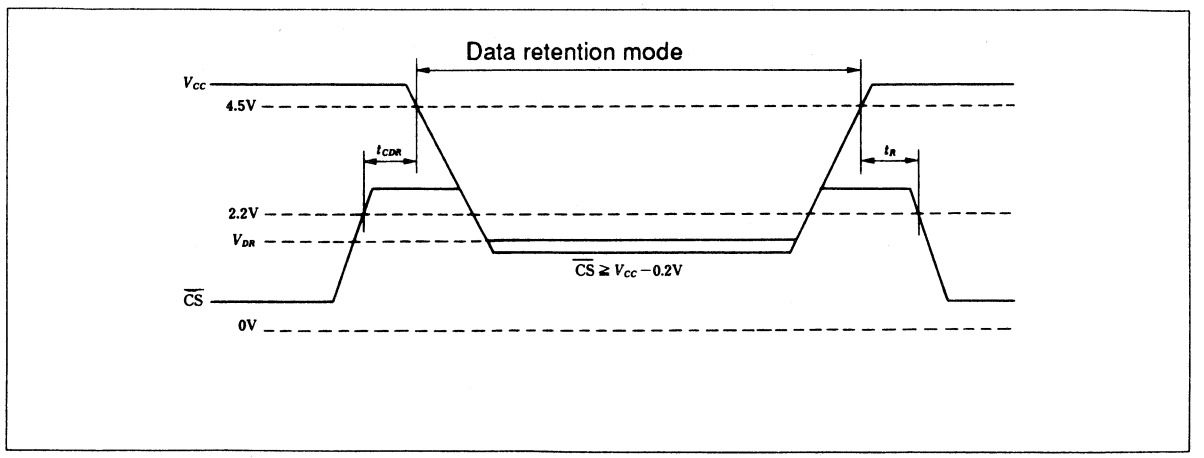
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, Vin ≥ V_{CC} – 0.2 V or 0 V ≤ Vin ≤ 0.2 V
Data retention current	I_{CCDR}	—	2	50*1	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

Note: *1. V_{CC} = 3.0 V.

Low V_{CC} Data Retention Timing Waveform



HM6707A Series

262144-word × 1-bit High Speed Static Random Access Memory

Features

- 262144-word × 1-bit organization
- Fully TTL compatible input and output
- 1.0 µm Hi-BiCMOS process
- +5 V single supply
- Completely static memory
  No clock or timing strobe required
- Low power dissipation
  Operating: 450 mW typ
- Super fast
  Access time: 15/20 ns (max)

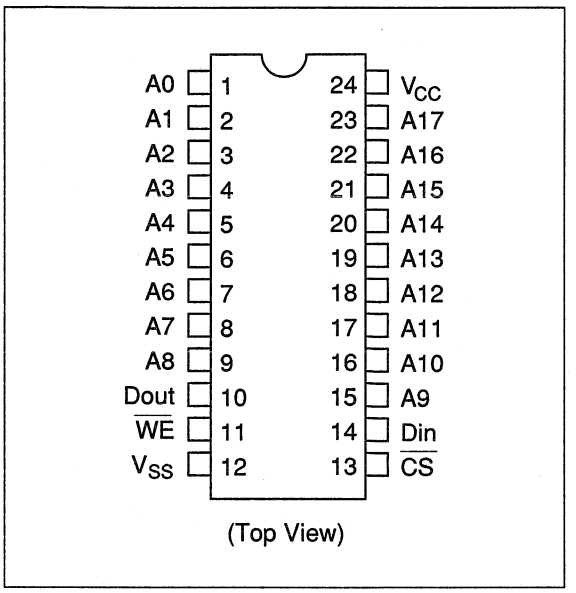
Ordering Information

Type No.	Cycle time	Package
HM6707AP-15	15 ns	300-mil 24-pin plastic DIP (DP-24NC)
HM6707AP-20	20 ns	
HM6707AJP-15	15 ns	300-mil 24-pin plastic SOJ (CP-24D)
HM6707AJP-20	20 ns	

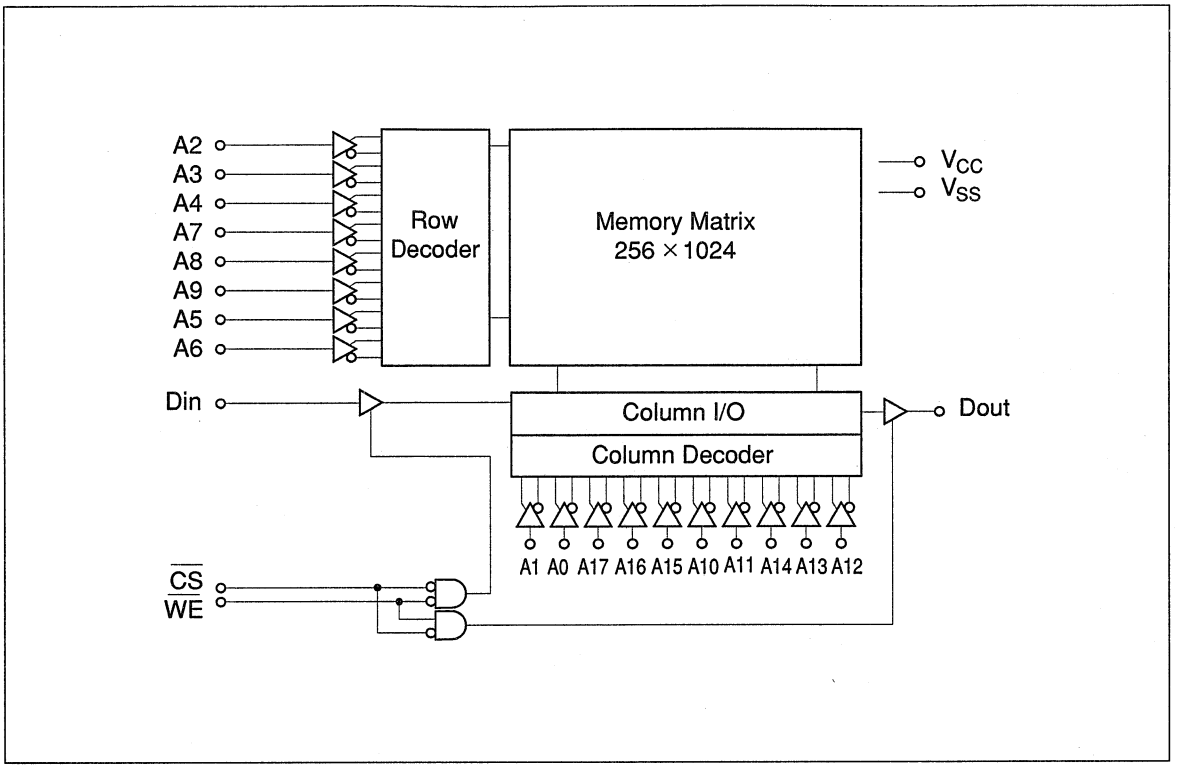
Pin Description

Pin name	Function
A0 – A17	Address input
Din	Data input
Dout	Data output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{SS}	Ground
V_{CC}	Power supply

Pin Arrangement



Block Diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	Output	V_{CC} current
H	X	Not selected	High-Z	I_{SB}, I_{SB1}
L	H	Read	Dout	I_{CC}, I_{CC1}
L	L	Write	High-Z	I_{CC}, I_{CC1}

Absolute Maximum Rating

Item	Symbol	Rating	Unit
Terminal voltage to V_{SS} pin	V_T	–0.5 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range (with bias)	Tstg (Bias)	–10 to +85	°C
Storage temperature range	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input high voltage	V_{IH}	2.2	—	V_{CC} +0.5	V
Input low voltage	V_{IL}	–3.0*1	—	0.8	V

Note: 1. Pulse width 15 ns, DC: –0.5 V

DC Characteristics (V_{CC} = 5.0 V ± 10%, Ta = 0 to + 70°C)

		HM6707A-15			HM6707A-20				
Item	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	2	—	—	2	µA	V_{CC} = 5.5 V, Vin = 0 V to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	10	—	—	10	µA	$\overline{CS}$ = V_{IH}, Vout = 0 V to V_{CC}
Operating power supply current	I_{CC}	—	—	100	—	—	100	mA	$\overline{CS}$ = V_{IL}, Iout = 0 mA
Average operating current	I_{CC1}	—	—	140	—	—	120	mA	min. cycle, Duty: 100%, Iout = 0 mA
Standby power supply current	I_{SB}	—	—	30	—	—	30	mA	$\overline{CS}$ = V_{IH}, Vin = V_{IH} or V_{IL}
	I_{SB1}	—	—	10	—	—	10	mA	$\overline{CS}$ ≥ V_{CC} –0.2 V Vin ≤ 0.2 V or Vin ≥ V_{CC} –0.2 V
Output low voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH} = –4 mA

Capacitance (Ta = 25°C, f = 1 MHz)

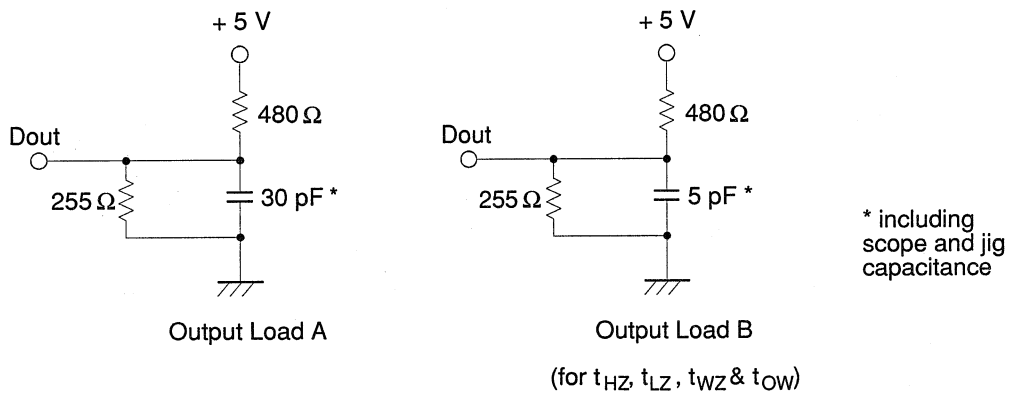
Item	Symbol	Max	Unit	Test condition
Input capacitance	Cin*1	6	pF	Vin = 0 V
Output capacitance	Cout*1	10	pF	Vout = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC} = 5V ± 10%, Ta = 0°C to +70°C, unless otherwise noted)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5 V
- Output load: See figures
- Input rise and fall times: 4 ns
- Output reference levels: 1.5 V



Read Cycle

Item	Symbol	HM6707A-15 Min	HM6707A-15 Max	HM6707A-20 Min	HM6707A-20 Max	Unit
Read cycle time	t_{RC}	15	—	20	—	ns
Address access time	t_{AA}	—	15	—	20	ns
Chip select access time	t_{ACS}	—	15	—	20	ns
Output hold from address change	t_{OH}	4	—	5	—	ns
Chip selection to output in low-Z	t_{LZ}*1, *2	4	—	5	—	ns
Chip deselection to output in high-Z	t_{HZ}*1, *2	0	6	0	8	ns

Notes: 1. This parameter is sampled and not 100% tested.
2. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).

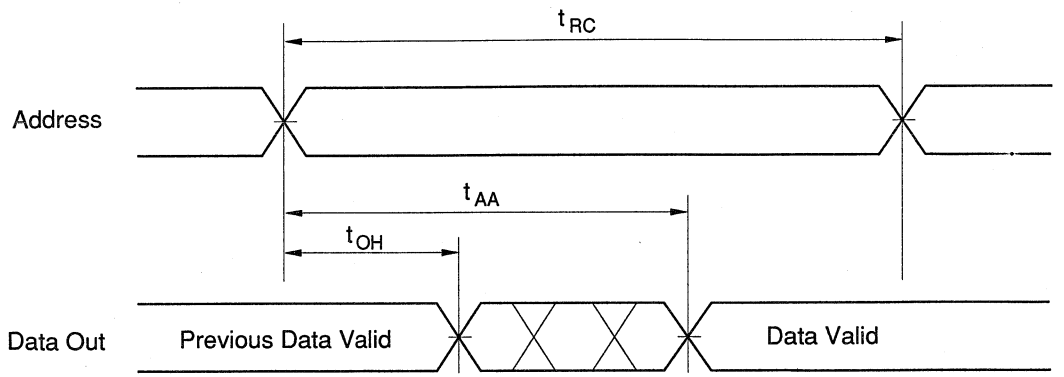
Write Cycle

Item	Symbol	HM6707A-15		HM6707A-20		Unit
		Min	Max	Min	Max	
Write cycle time	t_{WC} *1	15	—	20	—	ns
Chip selection to end of write	t_{CW}	12	—	15	—	ns
Address valid to end of write	t_{AW}	12	—	15	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	12	—	15	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Data valid to end of write	t_{DW}	10	—	10	—	ns
Data hold time	t_{DH}	0	—	0	—	ns
Write enable to output in high-Z	t_{WZ} *2, *3	0	6	0	8	ns
Output active from end of write	t_{OW} *2, *3	0	—	0	—	ns

Notes: 1 All write cycle timings are referenced from the last valid address to the first transitioning address.
2. This parameter is sampled and not 100% tested.
3. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).

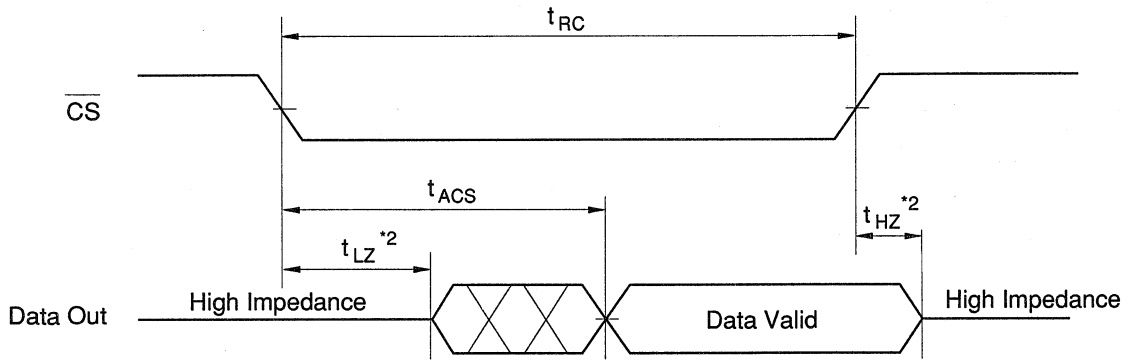
Timing Waveforms

Read Cycle (1) *1



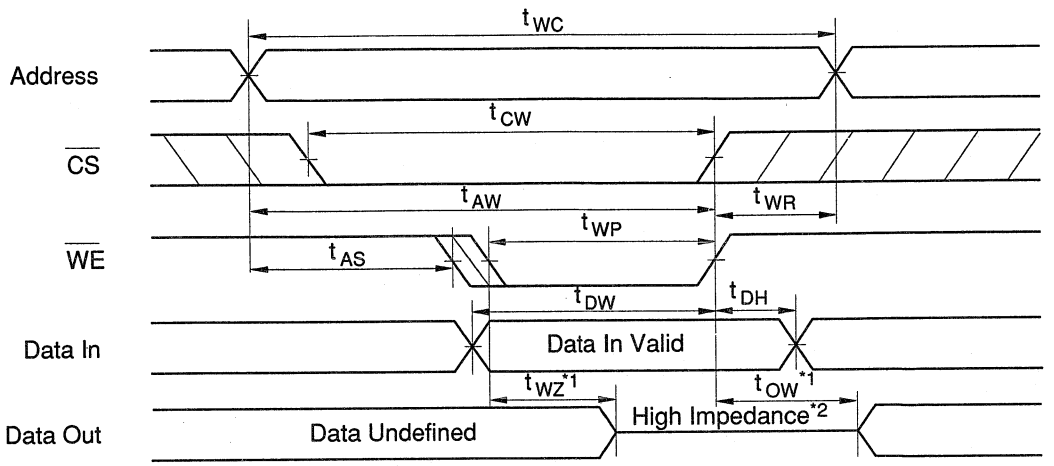
Note : 1. $\overline{WE}$ is high and $\overline{CS}$ is low for read cycle.

Read Cycle (2) *1, *2



Notes : 1. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
2. Transition is measured ± 200 mV from steady state voltage with specified loading in Load (B).

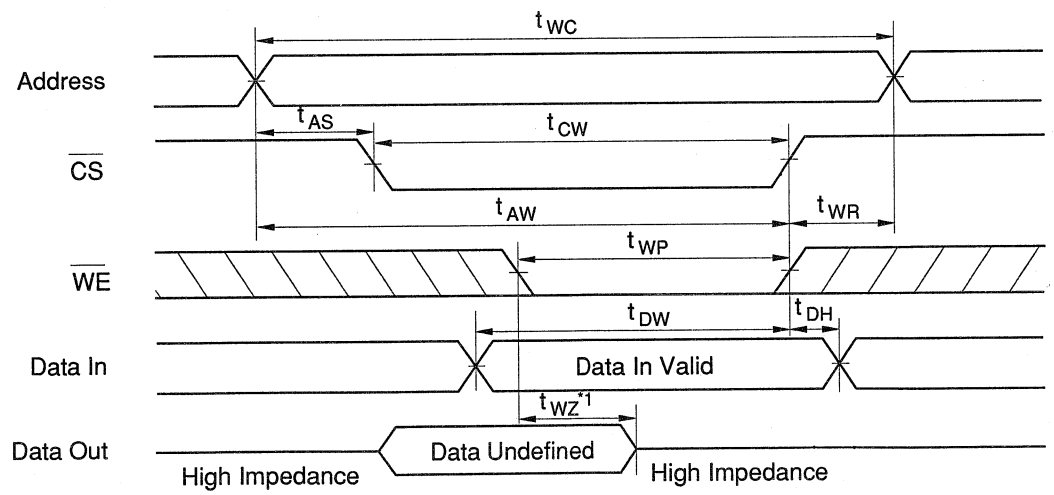
Write Cycle (1) *1, *2 ($\overline{WE}$ Controlled)



Notes : 1. Transition is measured ± 200 mV from steady state voltage with loading in Load(B).

2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

Write Cycle (2) *1 ($\overline{CS}$ Controlled)



Note : 1. Transition is measured ± 200 mV from steady state voltage with loading in Load(B).

HM628128 Series

131072-Word × 8-Bit High Speed CMOS Static RAM

The Hitachi HM628128 is a CMOS static RAM organized 128-kword x 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8 µm Hi-CMOS process technology.

It offers low power standby power dissipation; therefore, it is suitable for battery back-up systems. The device, packaged in a 525 mil SOP (460-mil body SOP) or a 600-mil plastic DIP, or a 8 × 20mm TSOP with thickness of 1.2 mm, is available for high density mounting. TSOP package is suitable for cards, and reverse type TSOP is also provided.

Features

- High speed: Fast access time 70/85/100/120 ns (max.)
- Low power
  - Standby: 10 µW (typ) (L-/L-L/L-SL version)
  - Operation: 75 mW (typ)
- Single 5 V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation (L-/L-L/L-SL version)
  - 2 chip selection for battery back up

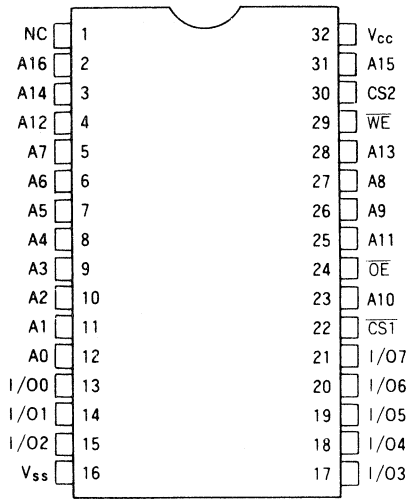
Ordering Information

Type No.	Access Time	Package
HM628128P-7	70 ns	600 mil 32-pin plastic DIP (DP-32)
HM628128P-8	85 ns	
HM628128P-10	100 ns	
HM628128P-12	120 ns	
HM628128LP-7	70 ns	
HM628128LP-8	85 ns	
HM628128LP-10	100 ns	
HM628128LP-12	120 ns	
HM628128LP-7SL	70 ns	
HM628128LP-8SL	85 ns	
HM628128LP-10SL	100 ns	
HM628128LP-12SL	120 ns	
HM628128T-7	70 ns	8mm × 20mm 32-pin TSOP (normal type) (TFP-32D)
HM628128T-8	85 ns	
HM628128T-10	100 ns	
HM628128T-12	120 ns	
HM628128LT-7	70 ns	
HM628128LT-8	85 ns	
HM628128LT-10	100 ns	
HM628128LT-12	120 ns	
HM628128LT-7L	70 ns	
HM628128LT-8L	85 ns	
HM628128LT-10L	100 ns	
HM628128LT-12L	120 ns	
HM628128LT-7SL	70 ns	
HM628128LT-8SL	85 ns	
HM628128LT-10SL	100 ns	
HM628128LT-12 SL	120 ns	

Type No.	Access Time	Package
HM628128FP-7	70 ns	525 mil 32-pin plastic DIP (FP-32D)
HM628128FP-8	85 ns	
HM628128FP-10	100 ns	
HM628128FP-12	120 ns	
HM628128LFP-7	70 ns	
HM628128LFP-8	85 ns	
HM628128LFP-10	100 ns	
HM628128LFP-12	120 ns	
HM628128LFP-7SL	70 ns	
HM628128LFP-8SL	85 ns	
HM628128LFP-10SL	100 ns	
HM628128LFP-12SL	120 ns	
HM628128R-7	70 ns	8mm × 20mm 32-pin TSOP (reverse type) (TFP-32DR)
HM628128R-8	85 ns	
HM628128R-10	100 ns	
HM628128R-12	120 ns	
HM628128LR-7	70 ns	
HM628128LR-8	85 ns	
HM628128LR-10	100 ns	
HM628128LR-12	120 ns	
HM628128LR-7L	70 ns	
HM628128LR-8L	85 ns	
HM628128LR-10L	100 ns	
HM628128LR-12L	120 ns	
HM628128LR-7SL	70 ns	
HM628128LR-8SL	85 ns	
HM628128LR-10SL	100 ns	
HM628128LR-12 SL	120 ns	

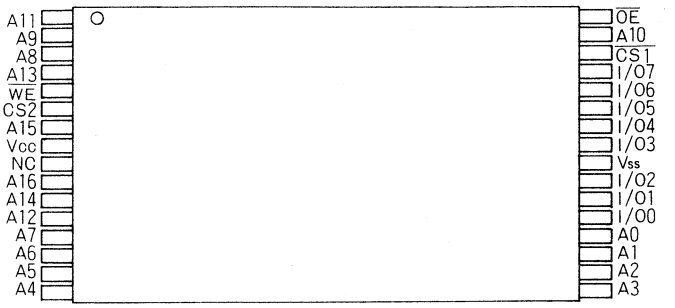
Pin Arrangement

● HM628128P Series
● HM628128FP Series



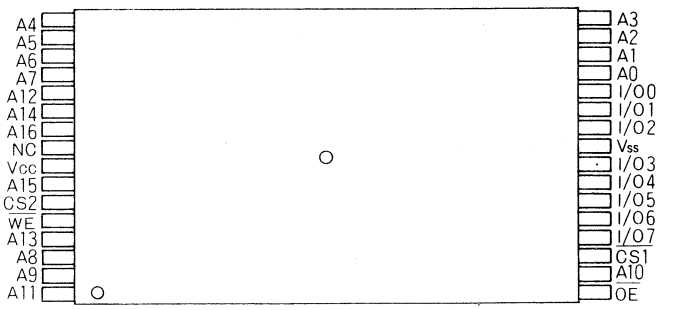
(Top View)

● HM628128T Series (Normal type TSOP)



(Top View)

● HM628128R Series (Reverse type TSOP)

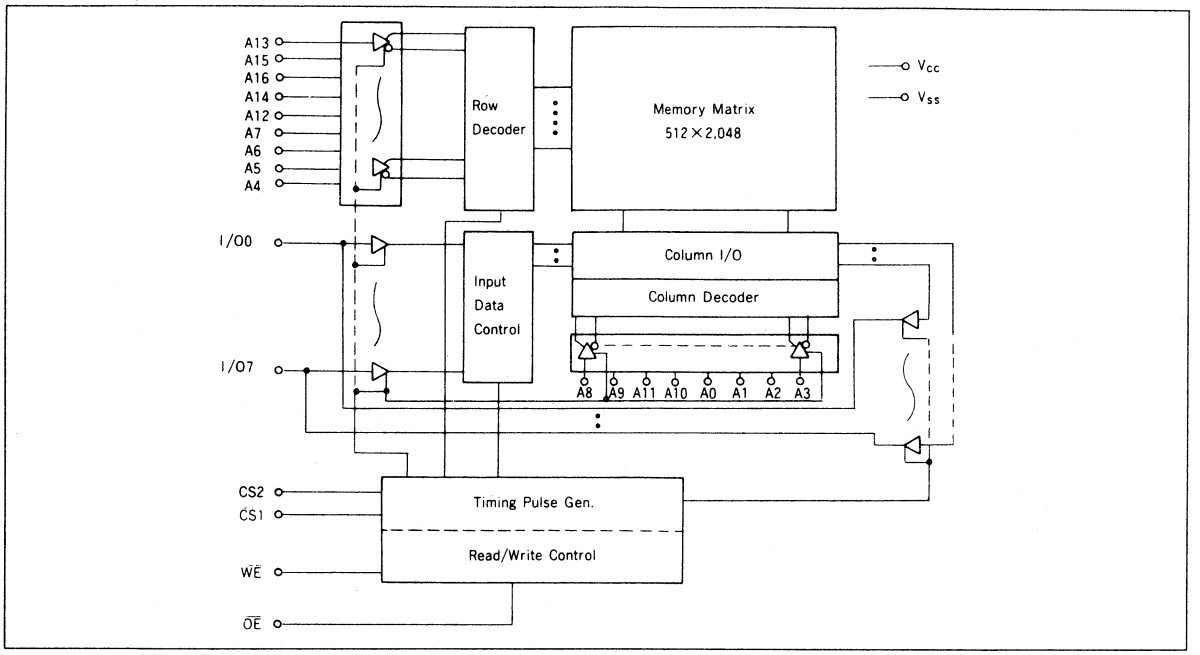


(Top View)

Pin Description

Pin Name	Function
A0 – A16	Address
I/O0 – I/O7	Input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
NC	No connection
Vcc	Power supply
Vss	Ground

Block Diagram



Function Table

$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	Mode	Vcc Current	Dout Pin	Ref. Cycle
×	H	×	×	Not selected	I_{SB}, I_{SB1}	High-Z	
×	×	L	×		I_{SB}, I_{SB1}	High-Z	
H	L	H	H	Output disable	Icc	High-Z	
H	L	H	L	Read	Icc	Dout	Read cycle
L	L	H	H	Write	Icc	Din	Write cycle (1)
L	L	H	L		Icc	Din	Write cycle (2)

Note: × : H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_T	–0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Note: *1. –3.0 V for pulse half-width ≤ 30 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V	
Input low (logic 0) voltage	V_{IL}	–0.3*1	—	0.8	V	

Note: *1. –3.0 V for pulse half-width ≤ 30 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min	Typ*1	Max	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	Vin = Vss to Vcc
Output leakage current	$\|I_{LO}\|$	—	—	2	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$= Vss to Vcc
Operating power supply current: DC	I_{CC}	—	15	35	mA	$\overline{CS1}$= V_{IL}, CS2 = V_{IH}, others = V_{IH}/V_{IL} $I_{I/O}$= 0 mA
Operating power supply current	I_{CC1}	—	45	70	mA	Min cycle, duty = 100%, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, others = V_{IH}/V_{IL} $I_{I/O}$ = 0 mA
	I_{CC2}	—	15	30	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA $\overline{CS1}$ ≤ 0.2 V, CS2 ≥Vcc – 0.2 V V_{IH} ≥ Vcc – 0.2V, V_{IL} ≤ 0.2V
Standby power supply current: DC	I_{SB}	—	1	3	mA	$\overline{CS1}$ = V_{IH}, CS2 = V_{IH} or CS2 = V_{IL}
Standby power supply current (1): DC	I_{SB1}	—	0.02	2	mA	Vin ≥ 0 V $\overline{CS1}$ ≥ Vcc – 0.2 V, CS2 ≥ Vcc – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V
		—	2*2	100*2	µA	
		—	2*3	50*3	µA	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –1.0 mA

Notes: *1. Typical values are at Vcc = 5.0 V, Ta = +25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.
*3. This characteristics is guaranteed only for L-L/L-SL version.

Capacitance (Ta = 25°C, f = 1.0 MHz)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note: This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, Vcc = 5 V ± 10%, unless otherwise noted)

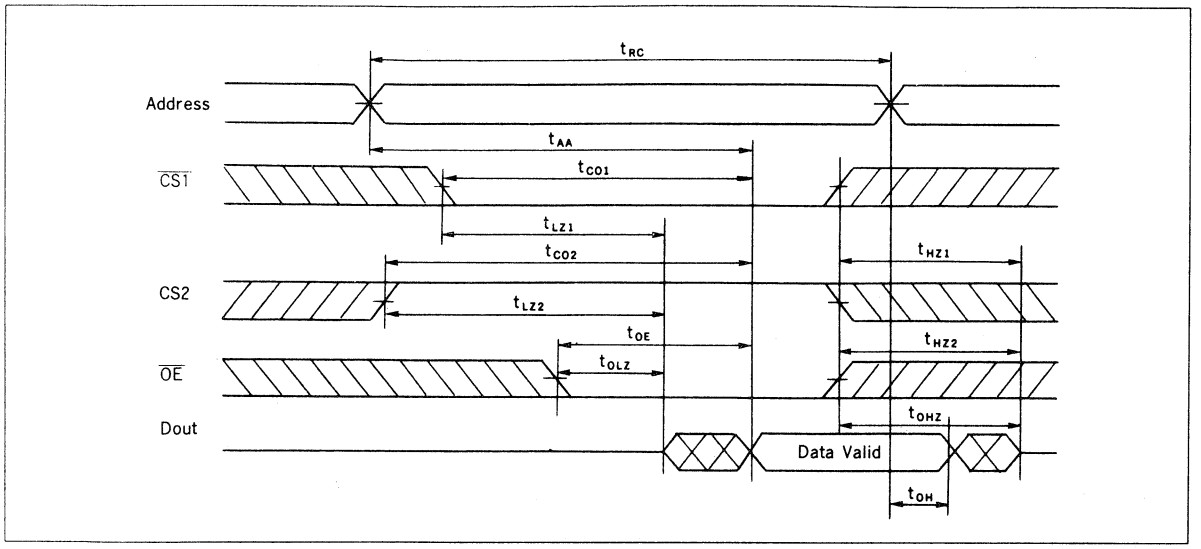
Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall times : 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate and CL (100pF) (Including scope & jig)

Read Cycle

Item	Symbol	HM628128-7		HM628128-8		HM628128-10		HM628128-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t_{RC}	70	—	85	—	100	—	120	—	ns	
Address access time	t_{AA}	—	70	—	85	—	100	—	120	ns	
Chip selection ($\overline{CS1}$) to output valid	t_{CO1}	—	70	—	85	—	100	—	120	ns	
Chip selection (CS2) to output valid	t_{CO2}	—	70	—	85	—	100	—	120	ns	
Output enable ($\overline{OE}$) to output valid	t_{OE}	—	35	—	45	—	50	—	60	ns	
Chip selection ($\overline{CS1}$) to output in low-Z	t_{LZ1}	10	—	10	—	10	—	10	—	ns	*1, *2, *3
Chip selection (CS2) to output in low-Z	t_{LZ2}	10	—	10	—	10	—	10	—	ns	*1, *2, *3
Output enable ($\overline{OE}$) to output in low-Z	t_{OLZ}	5	—	5	—	5	—	5	—	ns	*1, *2, *3
Chip deselection ($\overline{CS1}$) to output in high-Z	t_{HZ1}	0	25	0	30	0	35	0	45	ns	*1, *2, *3
Chip deselection (CS2) to output in high-Z	t_{HZ2}	0	25	0	30	0	35	0	45	ns	*1, *2, *3
Output disable ($\overline{OE}$) to output in high-Z	t_{OHZ}	0	25	0	30	0	35	0	45	ns	*1, *2, *3
Output hold from address change	t_{OH}	10	—	10	—	10	—	10	—	ns	

Read Timing Waveform*4

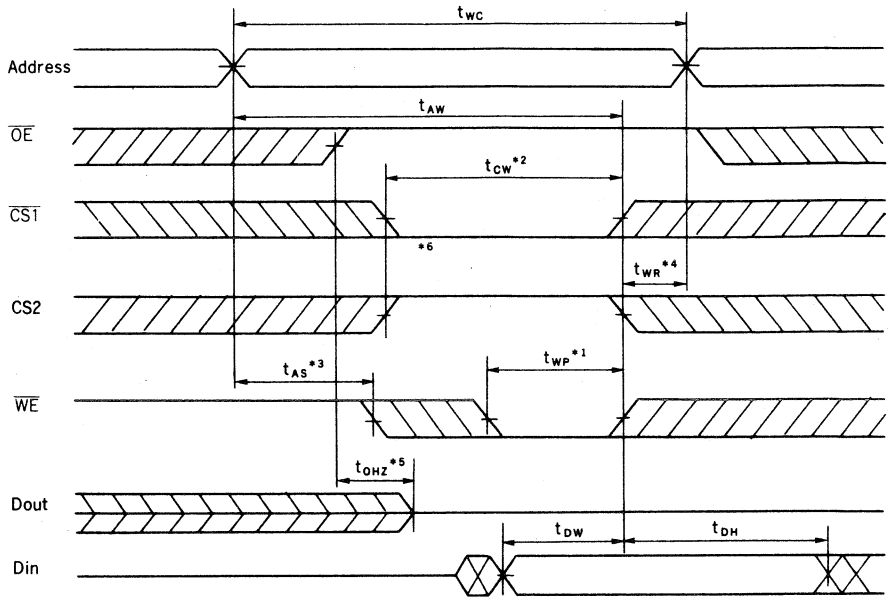


Notes: *1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
*2. At any given temperature and voltage condition, tHZ max is less than tLZ min both for a given device and from device to device.
*3. This parameter is sampled and not 100% tested.
*4. $\overline{WE}$ is high for read cycle.

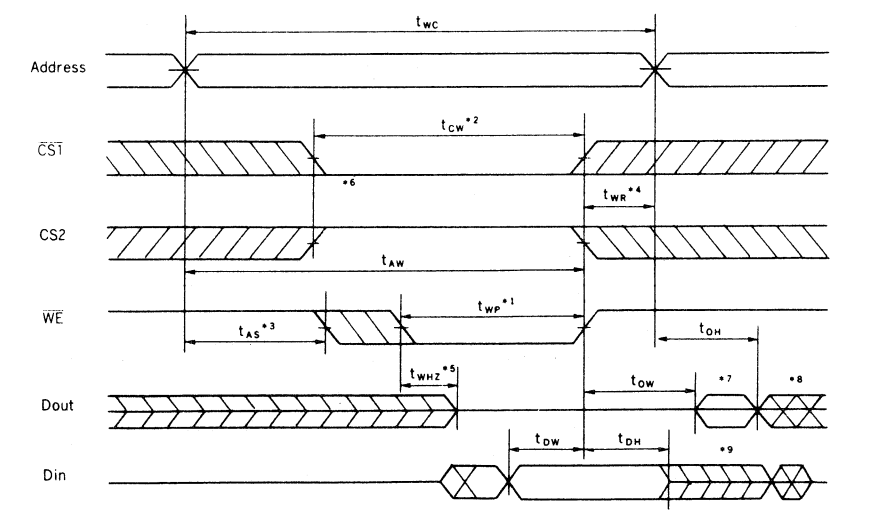
Write Cycle

Item	Symbol	HM628128-7		HM628128-8		HM628128-10		HM628128-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	tWC	70	—	85	—	100	—	120	—	ns	
Chip selection to end of write	tCW	60	—	75	—	80	—	85	—	ns	
Address setup time	tAS	0	—	0	—	0	—	0	—	ns	
Address valid to end of write	tAW	60	—	75	—	80	—	85	—	ns	
Write pulse width	tWP	50	—	55	—	60	—	70	—	ns	
Write recovery time	tWR	5	—	5	—	5	—	10	—	ns	
		10	—	10	—	10	—	15	—	ns	*11
Write to output in high-Z	tWHZ	0	25	0	30	0	35	0	40	ns	*10
Data to write time overlap	tDW	30	—	35	—	40	—	45	—	ns	
Write hold from write time	tDH	0	—	0	—	0	—	0	—	ns	
Output active from end of write	tOW	5	—	5	—	5	—	5	—	ns	*10

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Write Timing Waveform (2) ($\overline{OE}$ Low Fix)



Notes: *1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.

*2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.

*3. t_{AS} is measured from the address valid to the beginning of write.

*4. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.

*5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.

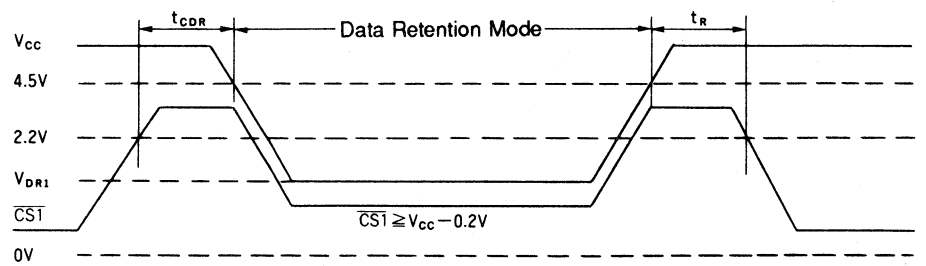
*6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
*7. Dout is the same phase of the latest written data in this write cycle.
*8. Dout is the read data of next address.
*9. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
*10. This parameter is sampled and not 100% tested.
*11. This value is measured from CS2 going low to the end of write cycle.

Low Vcc Data Retention Characteristics (Ta = 0 to +70°C)

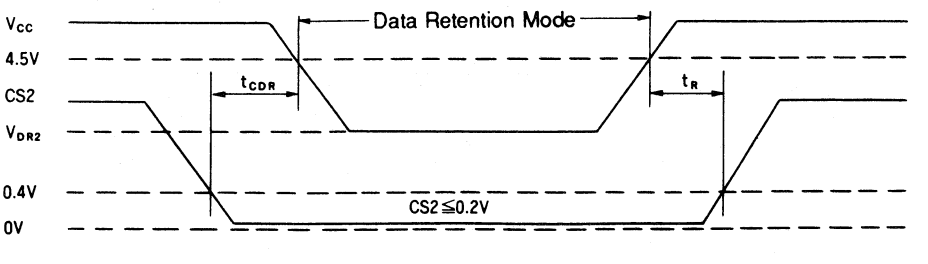
(This characteristics is guaranteed only for L, L-L and L-SL version.)

Item	Symbol		Min	Typ	Max	Unit	Test Conditions*4
Vcc for data retention	V_{DR}		2.0	—	—	V	$\overline{CS1} \geq Vcc-0.2$ V, CS2 ≥ Vcc–0.2 V, or 0 V ≤ CS2 ≤ 0.2 V Vin ≥ 0 V
Data retention current	I_{CCDR}	L	—	1	50*1	µA	Vcc = 3.0 V, Vin ≥ 0 V, $\overline{CS1} \geq Vcc-0.2$ V, CS2 ≥ Vcc–0.2 V or 0 V ≤ CS2 ≤ 0.2 V
		L-L	—	1	30*2	µA	
		L-SL	—	1	15*3		
Chip deselect to data retention time	t_{CDR}		0	—	—	ns	See Retention Waveform
Operation recovery time	t_R		5	—	—	ms	

Low Vcc Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)

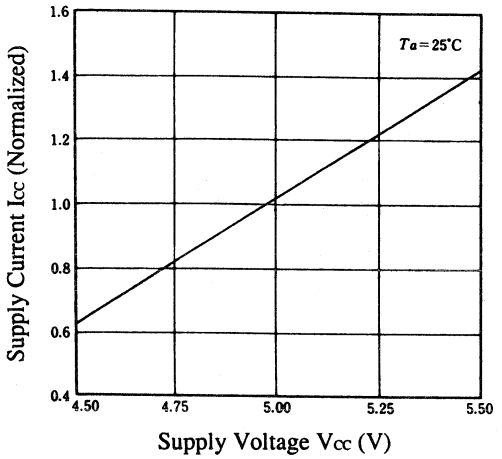


Low Vcc Data Retention Timing Waveform (2) (CS2 Controlled)

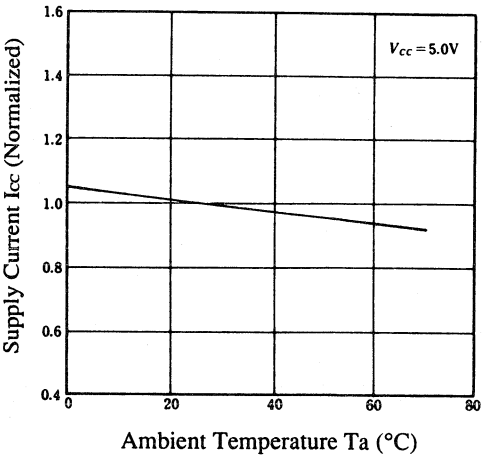


Notes: *1. 20 µA max at Ta = 0 to 40°C.
*2. 6 µA max at Ta = 0 to 40°C
*3. 3 µA max at Ta = 0 to 40°C.
*4. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer and $\overline{OE}$ buffer and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 ≥ Vcc – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

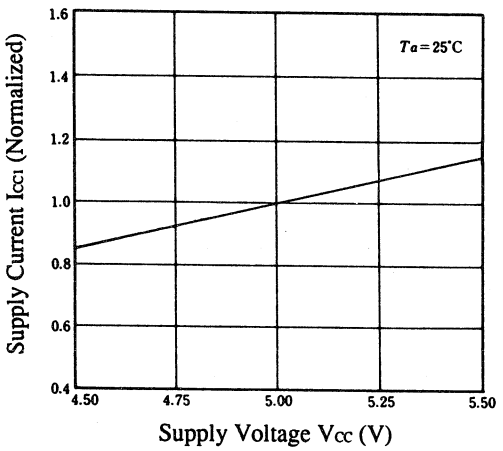
Supply Current vs. Supply Voltage (1)



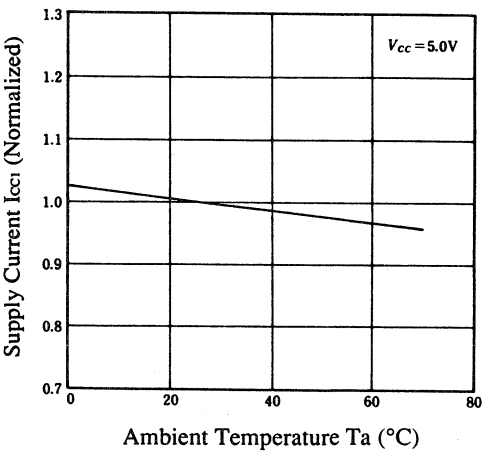
Supply Current vs. Ambient Temperature (1)



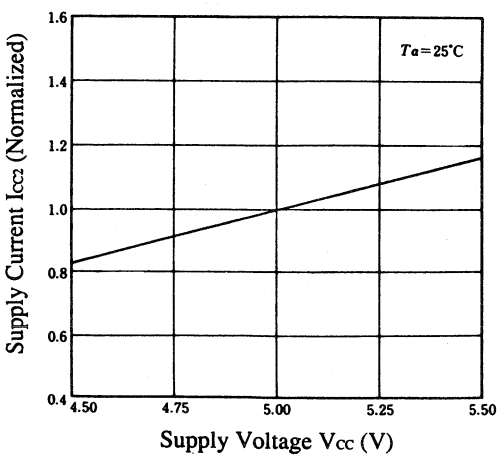
Supply Current vs. Supply Voltage (2)



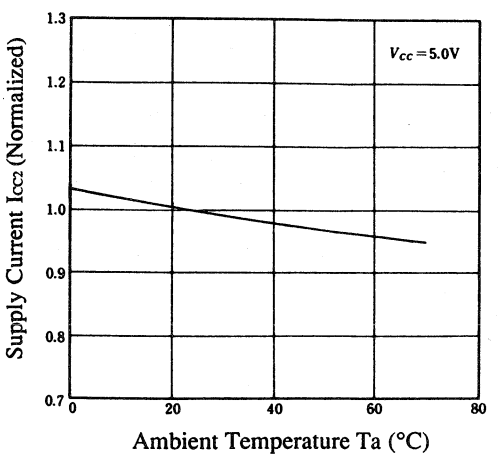
Supply Current vs. Ambient Temperature (2)



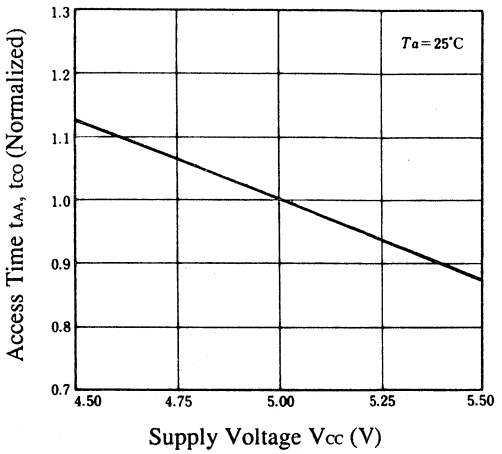
Supply Current vs. Supply Voltage (3)



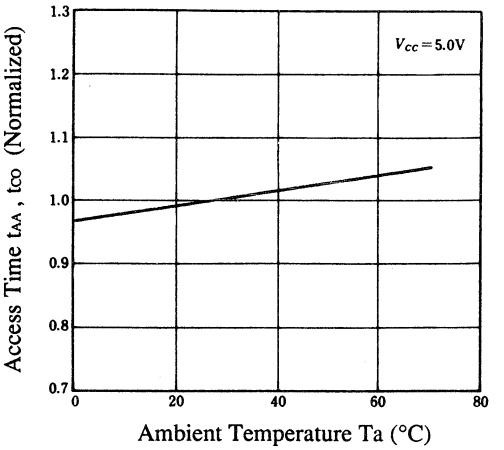
Supply Current vs. Ambient Temperature (3)



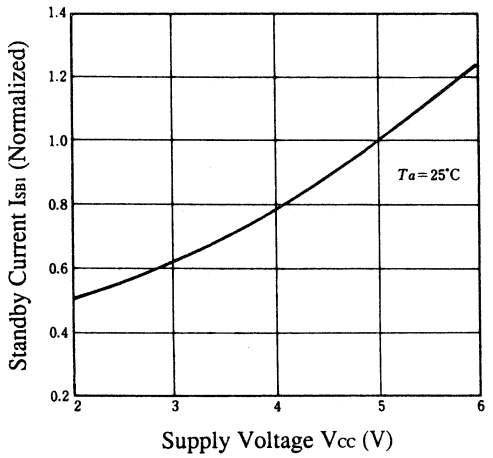
Access Time vs. Supply Voltage



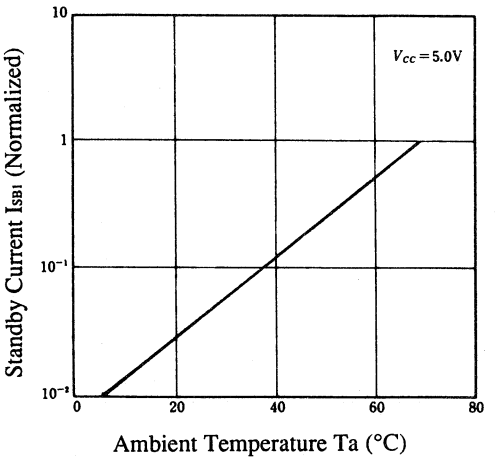
Access Time vs. Ambient Temperature



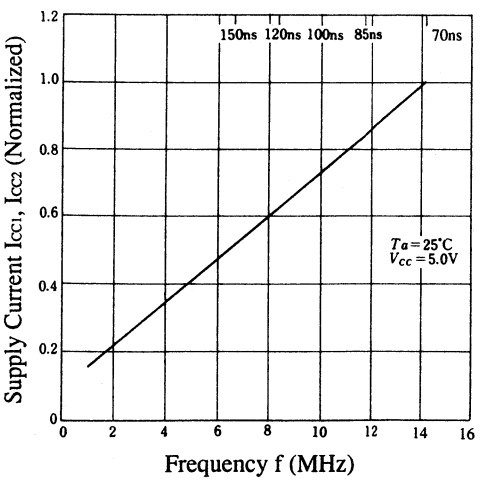
Standby Current vs. Supply Voltage



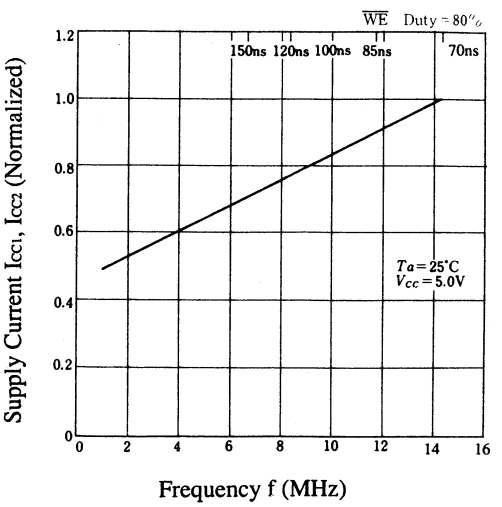
Standby Current vs. Ambient Temperature



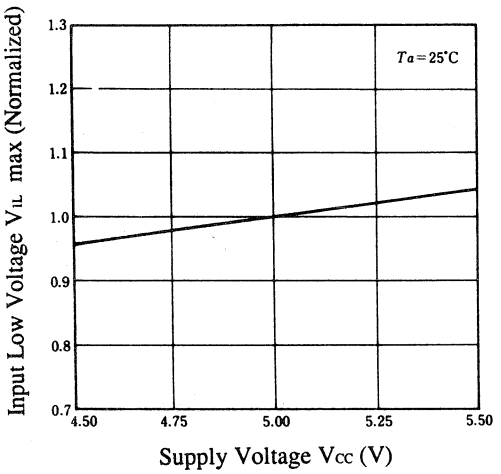
Supply Current vs. Frequency (Read)



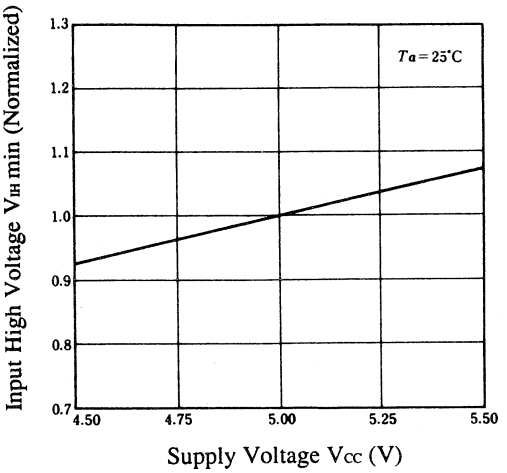
Supply Current vs. Frequency (Write)



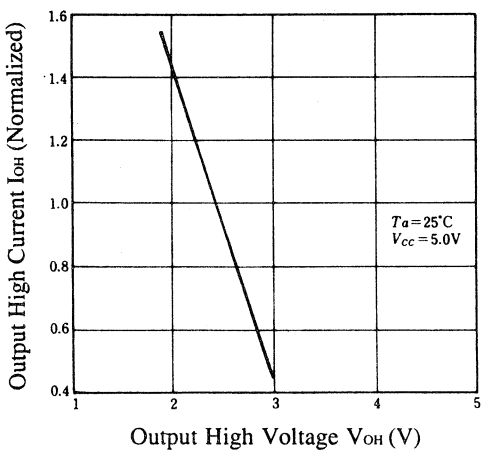
Input Low Voltage vs. Supply Voltage



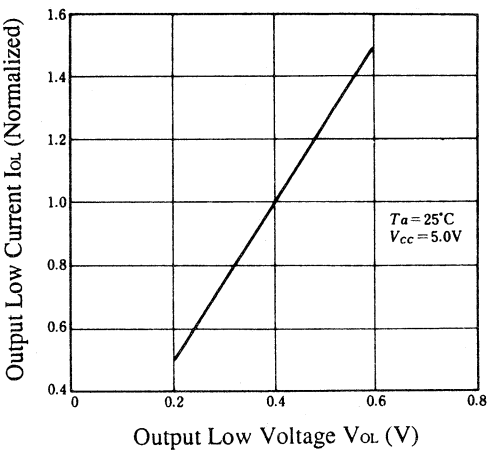
Input High Voltage vs. Supply Voltage



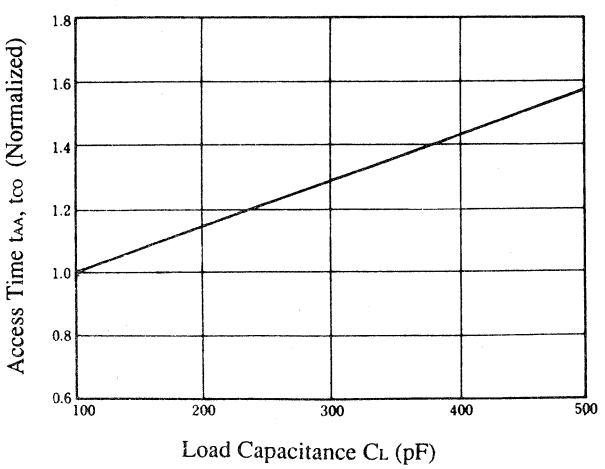
Output High Current vs. Output High Voltage



Output Low Current vs. Output Low Voltage



Access Time vs. Load Capacitance



HM628128A Series — Preliminary

131,072-word × 8-bit High Speed CMOS Static RAM

The Hitachi HM628128A is a CMOS static RAM organized 128 kword × 8 bit. It realizes higher density, higher performance and low power consumption by employing 0.8 µm Hi-CMOS process technology.
It offers low power standby power dissipation; therefore, it is suitable for battery back-up systems. The device, packaged in a 525-mil SOP (460-mil body SOP) or a 600-mil plastic DIP, or a 8 × 20 mm TSOP with thickness of 1.2 mm, is available for high density mounting. TSOP package is suitable for cards, and reverse type TSOP is also provided.

Features

- High speed
  - Fast access time: 55/70/85/100 ns (max)
- Low power
  - Active: 75 mW (typ)
  - Standby: 10 µW (typ) (L-/L-L/L-SL version)
- Single 5 V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  - Three state output
- Directly TTL compatible
  - All inputs and outputs
- Capability of battery back up operation (L-/L-L/L-SL version)
  - 2 chip selection for battery back up

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Ordering Information

Type No.	Access time	Package
HM628128AP–5	55 ns	600-mil 32-pin plastic DIP (DP-32)
HM628128AP–7	70 ns	
HM628128AP–8	85 ns	
HM628128AP–10	100 ns	
HM628128ALP–5	55 ns	
HM628128ALP–7	70 ns	
HM628128ALP–8	85 ns	
HM628128ALP–10	100 ns	
HM628128ALP–5SL	55 ns	
HM628128ALP–7SL	70 ns	
HM628128ALP–8SL	85 ns	
HM628128ALP–10SL	100 ns	
HM628128AFP–5	55 ns	525-mil 32-pin plastic SOP (FP-32D)
HM628128AFP–7	70 ns	
HM628128AFP–8	85 ns	
HM628128AFP–10	100 ns	
HM628128ALFP–5	55 ns	
HM628128ALFP–7	70 ns	
HM628128ALFP–8	85 ns	
HM628128ALFP–10	100 ns	
HM628128ALFP–5SL	55 ns	
HM628128ALFP–7SL	70 ns	
HM628128ALFP–8SL	85 ns	
HM628128ALFP–10SL	100 ns	

Type No.	Access time	Package
HM628128AT–5	55 ns	8 mm × 20 mm 32-pin TSOP (normal type) (TFP-32D)
HM628128AT–7	70 ns	
HM628128AT–8	85 ns	
HM628128AT–10	100 ns	
HM628128ALT–5	55 ns	
HM628128ALT–7	70 ns	
HM628128ALT–8	85 ns	
HM628128ALT–10	100 ns	
HM628128ALT–5L	55 ns	
HM628128ALT–7L	70 ns	
HM628128ALT–8L	85 ns	
HM628128ALT–10L	100 ns	
HM628128AR–5	55 ns	8 mm × 20 mm 32-pin TSOP (reverse type) (TFP-32DR)
HM628128AR–7	70 ns	
HM628128AR–8	85 ns	
HM628128AR–10	100 ns	
HM628128ALR–5	55 ns	
HM628128ALR–7	70 ns	
HM628128ALR–8	85 ns	
HM628128ALR–10	100 ns	
HM628128ALR–5L	55 ns	
HM628128ALR–7L	70 ns	
HM628128ALR–8L	85 ns	
HM628128ALR–10L	100 ns	

HM629128 Series — Preliminary

131,072-word × 9-bit High Speed CMOS Static RAM

The Hitachi HM629128 is a CMOS static RAM organized 128 kword × 9 bit. It realizes higher density, higher performance and low power consumption by employing 0.8 µm Hi-CMOS process technology.

It offers low power standby power dissipation; therefore, it is suitable for battery back-up systems. The device, packaged in a 525-mil SOP (460-mil body SOP) or a 600-mil plastic DIP, or a 8 × 20 mm TSOP with thickness of 1.2 mm, is available for high density mounting. TSOP package is suitable for cards, and reverse type TSOP is also provided.

Features

- High speed
  - Fast access time: 55/70/85/100 ns (max)
- Low power
  - Active: 75 mW (typ)
  - Standby: 10 µW (typ) (L-/L-L/L-SL version)
- Single 5 V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  - Three state output
- Directly TTL compatible
  - All inputs and outputs
- Capability of battery back up operation (L-/L-L/L-SL version)

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Ordering Information

Type No.	Access time	Package
HM629128P–5	55 ns	600-mil 32-pin plastic DIP (DP-32)
HM629128P–7	70 ns	
HM629128P–8	85 ns	
HM629128P–10	100 ns	
HM629128LP–5	55 ns	
HM629128LP–7	70 ns	
HM629128LP–8	85 ns	
HM629128LP–10	100 ns	
HM629128LP–5SL	55 ns	
HM629128LP–7SL	70 ns	
HM629128LP–8SL	85 ns	
HM629128LP–10SL	100 ns	
HM629128FP–5	55 ns	525-mil 32-pin plastic SOP (FP-32D)
HM629128FP–7	70 ns	
HM629128FP–8	85 ns	
HM629128FP–10	100 ns	
HM629128LFP–5	55 ns	
HM629128LFP–7	70 ns	
HM629128LFP–8	85 ns	
HM629128LFP–10	100 ns	
HM629128LFP–5SL	55 ns	
HM629128LFP–7SL	70 ns	
HM629128LFP–8SL	85 ns	
HM629128LFP–10SL	100 ns	

Type No.	Access time	Package
HM629128T–5	55 ns	8 mm x 20 mm 32-pin TSOP (normal type) (TFP-32D)
HM629128T–7	70 ns	
HM629128T–8	85 ns	
HM629128T–10	100 ns	
HM629128LT–5	55 ns	
HM629128LT–7	70 ns	
HM629128LT–8	85 ns	
HM629128LT–10	100 ns	
HM629128LT–5L	55 ns	
HM629128LT–7L	70 ns	
HM629128LT–8L	85 ns	
HM629128LT–10L	100 ns	
HM629128R–5	55 ns	8 mm x 20 mm 32-pin TSOP (reverse type) (TFP-32DR)
HM629128R–7	70 ns	
HM629128R–8	85 ns	
HM629128R–10	100 ns	
HM629128LR–5	55 ns	
HM629128LR–7	70 ns	
HM629128LR–8	85 ns	
HM629128LR–10	100 ns	
HM629128LR–5L	55 ns	
HM629128LR–7L	70 ns	
HM629128LR–8L	85 ns	
HM629128LR–10L	100 ns	

HM62V8128 Series — Preliminary

131,072-word × 8-bit High Speed CMOS Static RAM

The Hitachi HM62V8128 is a CMOS static RAM organized 128 kword × 8 bit. It realizes higher density, higher performance and low power consumption by employing 0.8 µm Hi-CMOS process technology.
It offers low power standby power dissipation; therefore, it is suitable for battery back-up systems. The device, packaged in a 525-mil SOP (460-mil body SOP) or a 600-mil plastic DIP, or a 8 × 20 mm TSOP with thickness of 1.2 mm, is available for high density mounting. TSOP package is suitable for cards, and reverse type TSOP is also provided.

Features

- Single 3 V supply
- High speed
  - Fast access time: 150 ns (max)
- Low power
  - Active: 30 mW (typ)
  - Standby: 3 µW (typ) (L-/L-L/L-SL version)
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  - Three state output
- All inputs and outputs CMOS compatible.
- Capability of battery back up operation (L-/L-L/L-SL version)
  - 2 chip selection for battery back up

Ordering Information

Type No.	Access time	Package
HM62V8128P-15	150ns	600-mil 32-pin plastic DIP (DP-32)
HM62V8128LP-15	150 ns	
HM62V8128LP-15SL	150ns	
HM62V8128FP-15	150 ns	525-mil 32-pin plastic SOP (FP-32D)
HM62V8128LFP-15	150 ns	
HM62V8128LFP-15SL	150 ns	
HM62V8128T-15	150 ns	8 mm × 20 mm 32-pin TSOP (normal type) (TFP-32D)
HM62V8128LT-15	150 ns	
HM62V8128LT-15L	150 ns	
HM62V8128R-15	150 ns	8 mm × 20 mm 32-pin TSOP (reverse type) (TFP-32DR)
HM62V8128LR-15	150 ns	
HM62V8128LR-15L	150 ns	

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

HM624256A Series

262144-word × 4-bit High Speed CMOS Static RAM

The Hitachi HM624256A is a high speed 1M Static RAM organized as 256-kword × 4-bit. It realizes high speed access time (20/25/35 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology.

It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM624256A, packaged in a 400-mil plastic SOJ is available for high density mounting.

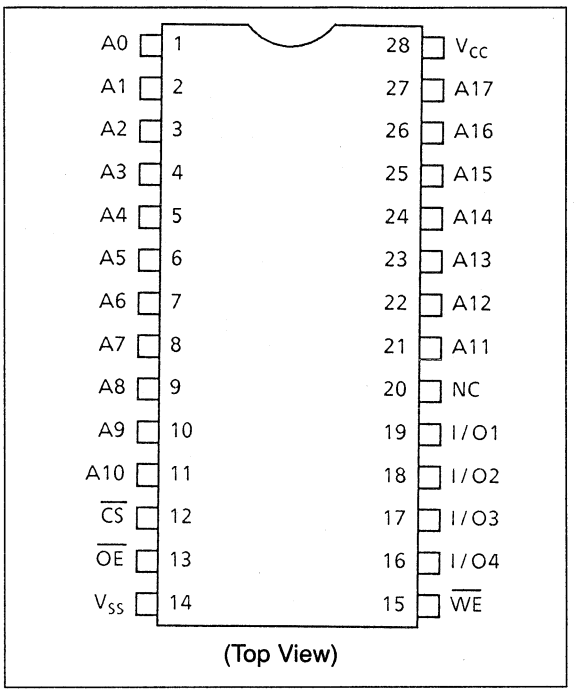
Features

- Single 5 V supply and high density 28-pin package (DIP and SOJ)
- High speed
  Access time: 20/25/35 ns (maximum)
- Low power dissipation
  Active mode: 350 mW (typical)
  Standby mode: 100 µW (typical)
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible
  All inputs and outputs

Ordering Information

Type No.	Access time	Package
HM624256AP-20	20 ns	400 mil 28-pin plastic DIP (DP-28C)
HM624256AP-25	25 ns	
HM624256AP-35	35 ns	
HM624256ALP-20	20 ns	
HM624256ALP-25	25 ns	
HM624256ALP-35	35 ns	
HM624256AJP-20	20 ns	400 mil 28-pin plastic SOJ (CP-28D)
HM624256AJP-25	25 ns	
HM624256AJP-35	35 ns	
HM624256ALJP-20	20 ns	
HM624256ALJP-25	25 ns	
HM624256ALJP-35	35 ns	

Pin Arrangement

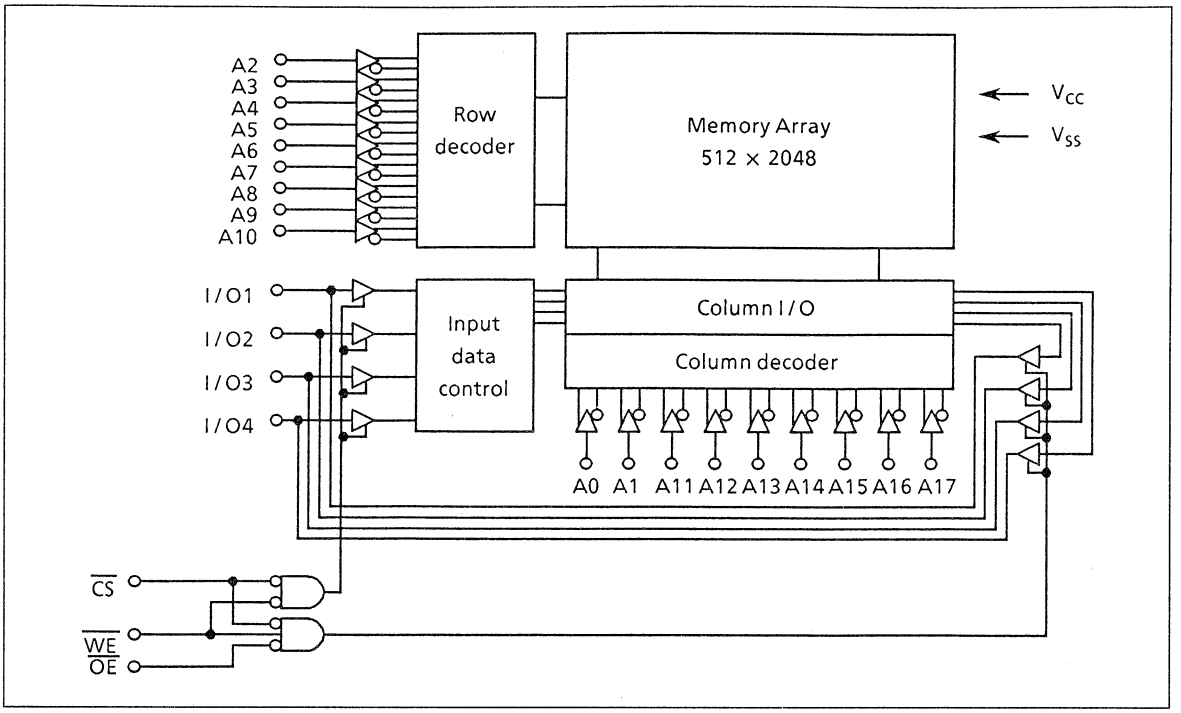


(Top View)

Pin Description

Pin name	Function
A0 – A17	Address
I/O1 – I/O4	Input/output
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
H	X	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	I_{CC}	Dout	Read cycle (1) – (3)
L	H	L	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: 1. X: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	Vin	–0.5[*1] to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–10 to +85	°C

Note: 1. Vin min = –2.0 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: 1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM624256A-20			HM624256A-25/35				
Parameter	Symbol	Min	Typ*1	Max	Min	Typ*1	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	—	—	2.0	µA	V_{CC} = max Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	2.0	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current	I_{CC}	—	—	150	—	—	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, min cycle
Standby power supply current	I_{SB}	—	—	60	—	—	40	mA	$\overline{CS}$ = V_{IH}, min cycle
Standby power supply current (1)	I_{SB1}	—	0.02	2.0	—	0.02	2.0	mA	$\overline{CS}$ ≥ V_{CC} –0.2 V 0 V ≤ Vin ≤ 0.2 V or Vin ≥ V_{CC} –0.2 V
	I_{SB1}*2	—	—	100*2	—	—	100*2	µA	
Output low voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH} = –4 mA

Notes: 1. Typical limits are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.
2. LP and LJP version

Capacitance (Ta = 25°C, f = 1 MHz)

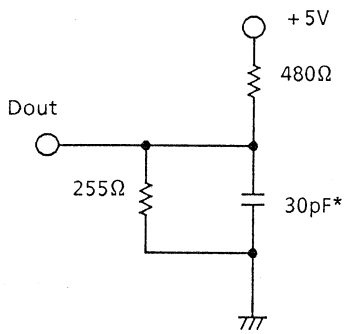
Parameter	Symbol	Min	Max	Unit	Test conditions
Input capacitance	Cin	—	5*2	pF	Vin = 0 V
			6*3		
Input/output capacitance	$C_{I/O}$	—	8	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.
2. SOJ package
3. DIP package

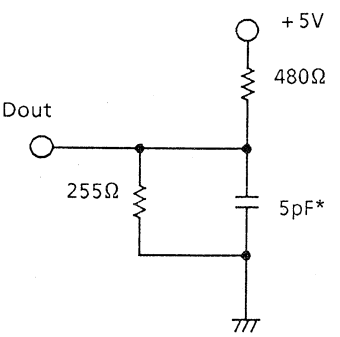
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0V to 3.0 V
- Input rise and fall times: 4 ns
- Input timing reference levels: 1.5 V
- Output timing reference levels: 1.5 V
- Output load: See figures



Output Load (A)
* Including scope & jig

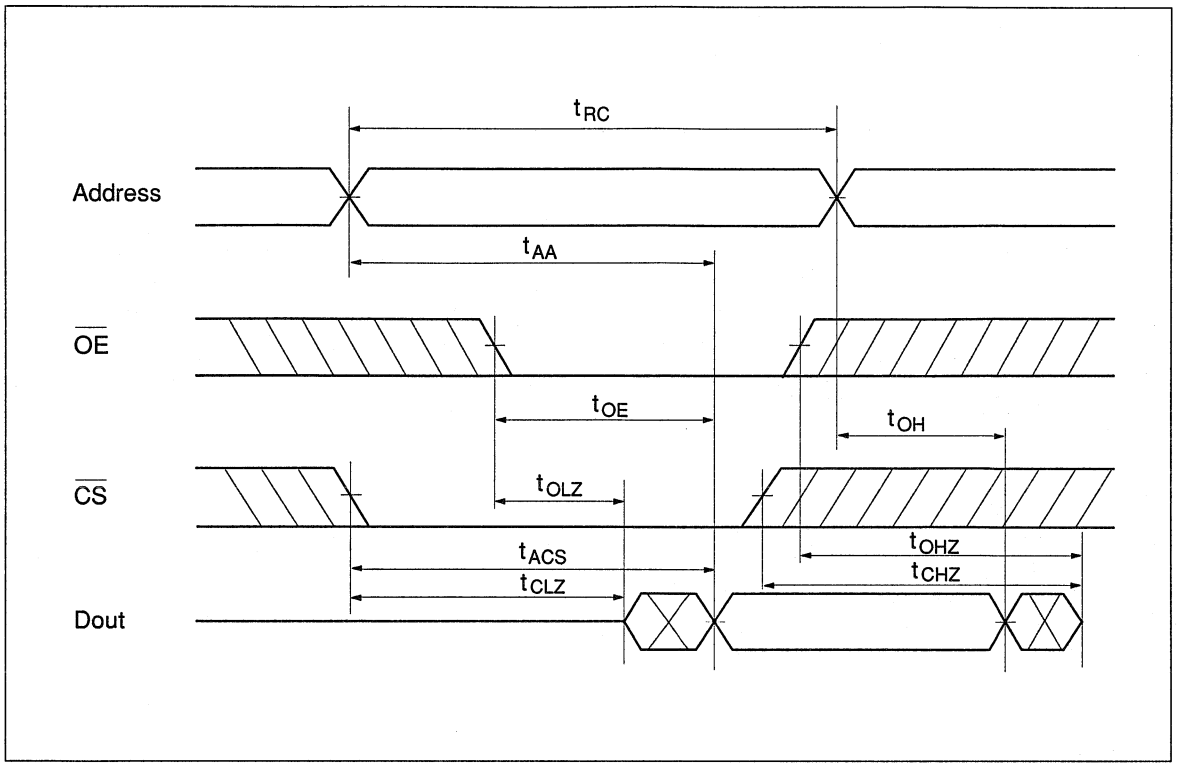


Output Load (B)
(for t_{CHZ}, t_{CLZ}, t_{WHZ} & t_{OW})

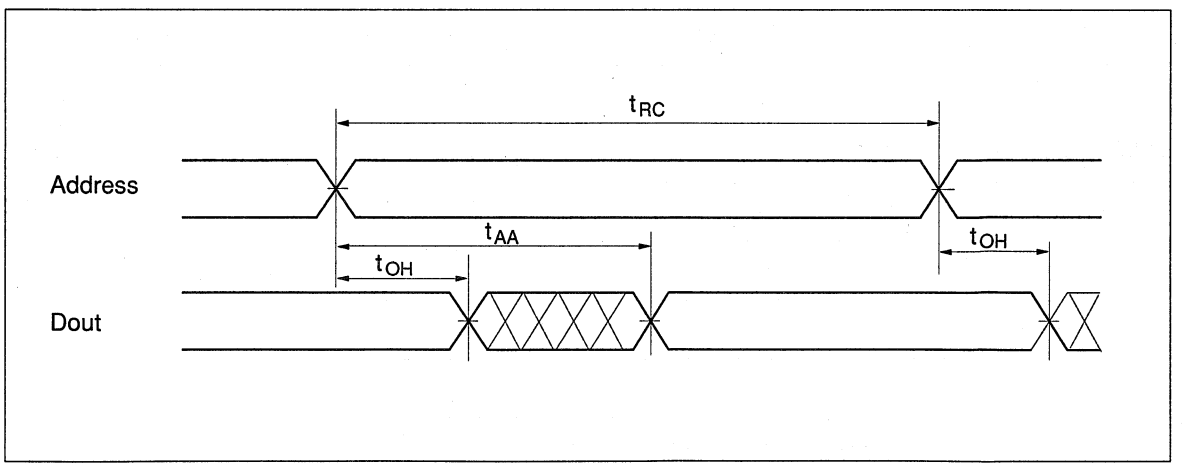
Read Cycle

		HM624256A-20		HM624256A-25		HM624256A-35		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	20	—	25	—	35	—	ns
Address access time	t_{AA}	—	20	—	25	—	35	ns
Chip select access time	t_{ACS}	—	20	—	25	—	35	ns
Chip selection to output in low-Z	t_{CLZ}*1	5	—	5	—	5	—	ns
Output enable to output valid	t_{OE}	—	10	—	12	—	15	ns
Output enable to output in low-Z	t_{OLZ}*1	0	—	0	—	0	—	ns
Chip deselection to output in high-Z	t_{CHZ}*1	0	10	0	12	0	15	ns
Chip disable to output in high-Z	t_{OHZ}*1	0	10	0	10	0	10	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip selection to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	12	—	15	—	25	ns

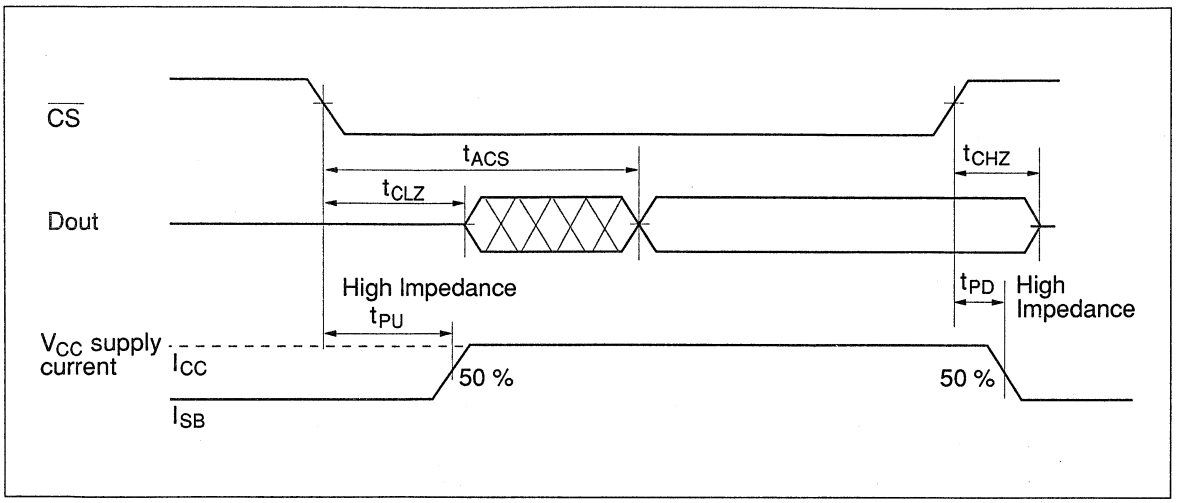
Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *2, *3, *5



Read Timing Waveform (3) *1, *2, *4, *5

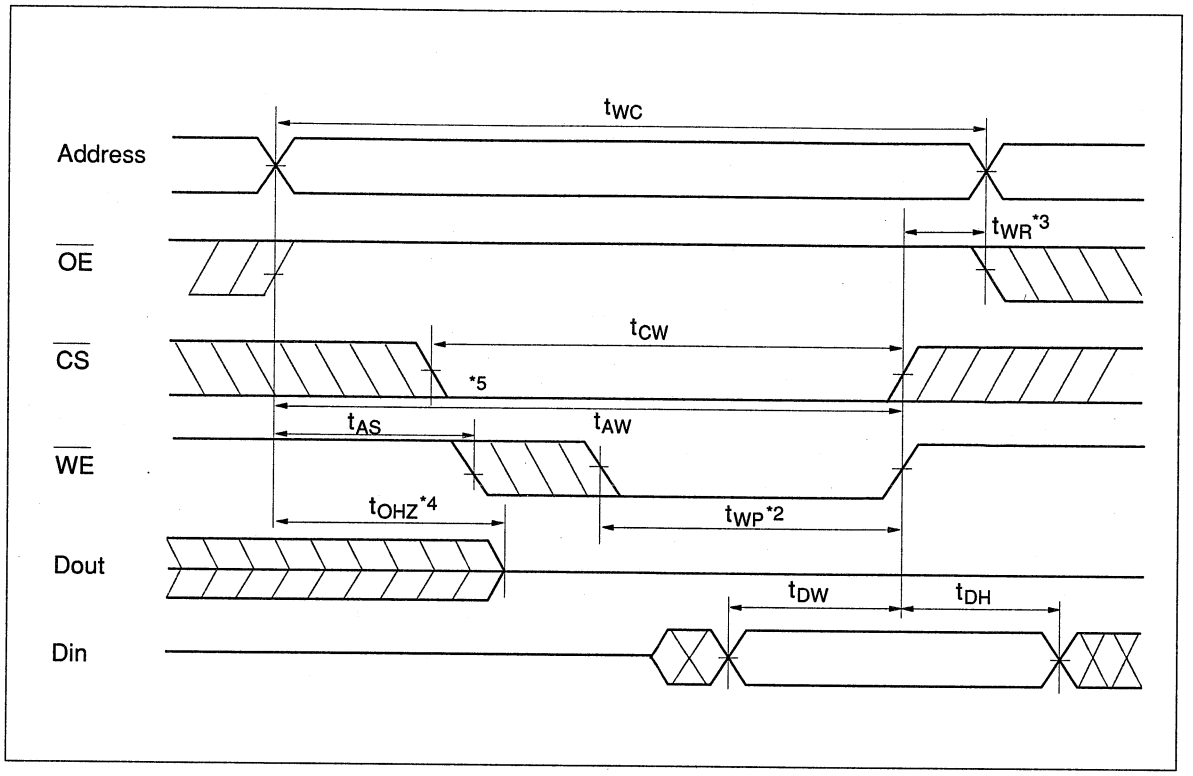


Notes: 1. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
2. $\overline{WE}$ is high for read cycle.
3. Device is continuously selected, $\overline{CS} = V_{IL}$.
4. Address valid prior to or coincident with $\overline{CS}$ transition low.
5. $\overline{OE} = V_{IL}$.

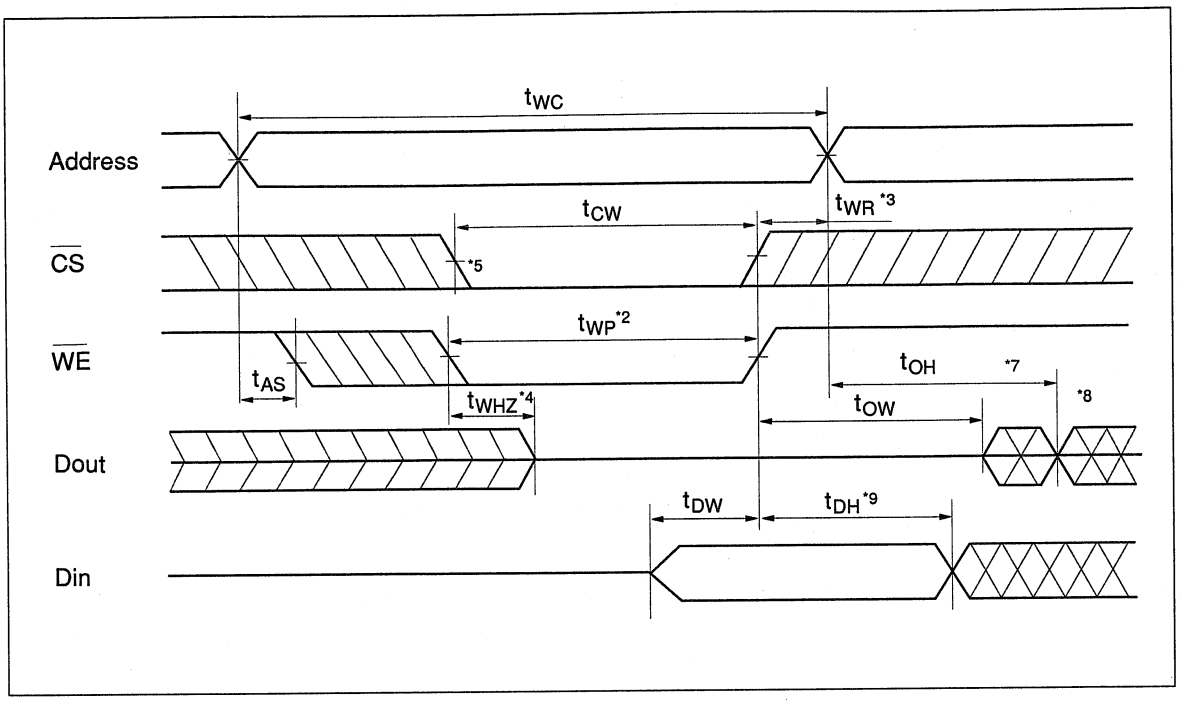
Write Cycle

		HM624256A-20		HM624256A-25		HM624256A-35		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time	t_{WC}	20	—	25	—	35	—	ns
Chip selection to end of write	t_{CW}	15	—	17	—	25	—	ns
Address valid to end of write	t_{AW}	16	—	20	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	15	—	17	—	25	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Output disable to output in high-Z*1	t_{OHZ}	0	10	0	10	0	10	ns
Write to output in high-Z *1	t_{WHZ}	0	12	0	15	0	15	ns
Data to write time overlap	t_{DW}	12	—	15	—	20	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Output active from end of write*1	t_{OW}	0	—	0	—	0	—	ns

Write Timing Waveform (1)



Write Timing Waveform (2) *6



Notes:
1. Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
7. Dout is the same phase of write data of this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

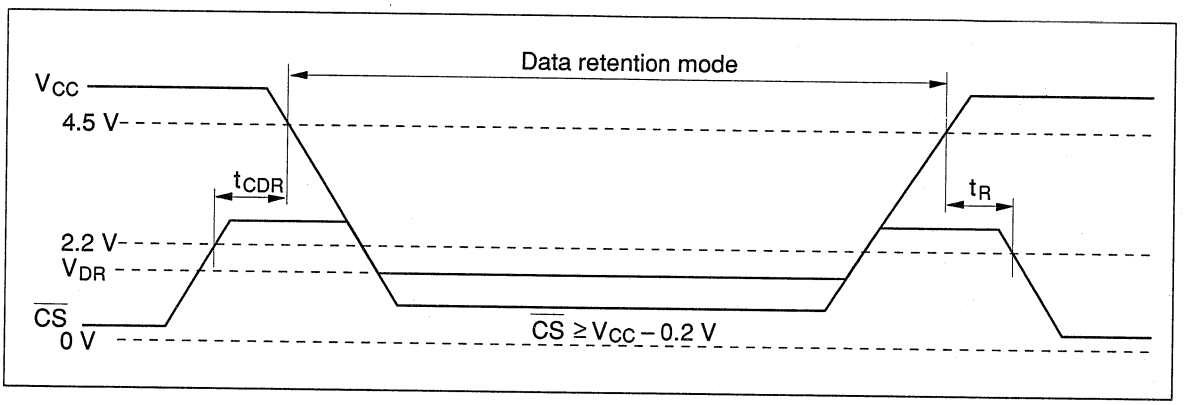
Low V_{CC} Date Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, Vin $\geq V_{CC} - 0.2$ V or 0 V $\leq$ Vin $\leq$ 0.2 V
Data retention current	I_{CCDR}	—	2	50*1	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

Note: 1. V_{CC} = 3.0 V.

Low V_{CC} Data Retention Timing Waveform



HM624257 Series

262144-Word × 4-Bit High Speed CMOS Static RAM

The Hitachi HM624257 is a high speed 1M Static RAM organized as 256-kword x 4-bit. It realizes high speed access time (35/45 ns) and low power consumption, employing the advanced CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM624257, packaged in a 400-mil plastic SOJ is available for high density mounting.

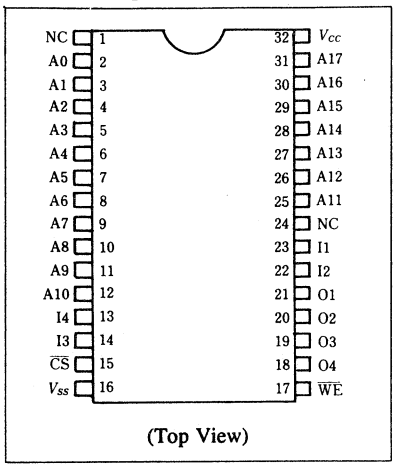
Features

- Single 5 V supply and high density 32 pin package (SOJ)
- High speed
  - Access time: 35 ns/45 ns (max)
- Low power dissipation
  - Active mode: 350 mW (typ)
  - Standby mode: 100 µW (typ)
- Completely static memory required
  - No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible: All inputs and outputs

Ordering Information

Type No.	Access Time	Package
HM624257JP-35	35 ns	400-mil
HM624257JP-45	45 ns	32-pin
HM624257LJP-35	35 ns	plastic SOJ
HM624257LJP-45	45 ns	(CP-32D)

Pin Arrangement

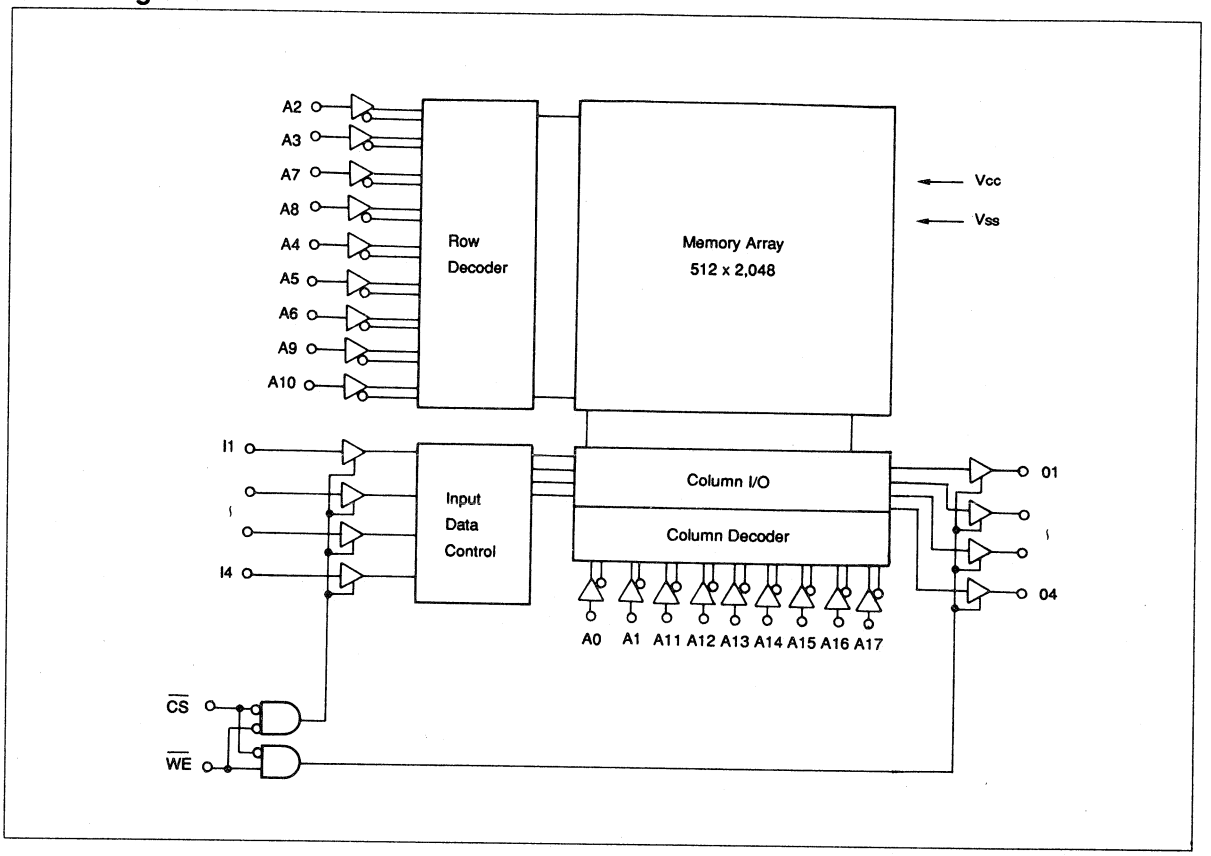


(Top View)

Pin Description

Pin Name	Function
A0 – A17	Address
I1 – I4	Data input
O1 – O4	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	Vin	–0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–10 to +85	°C

Note: *1. Vin min = –2.0V for pulse width ≤ 10 ns.

Function Table

$\overline{CS}$	$\overline{WE}$	Mode	Vcc Current	Dout Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	Icc	Dout	Read cycle (1)–(2)
L	L	Write	Icc	High-Z	Write cycle (1)–(2)

Note: ×; H or L

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: *1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min	Typ*1	Max	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	µA	V_{CC} = Max Vin = Vss to Vcc
Output leakage current	$\|I_{LO}\|$	—	—	2.0	µA	$\overline{CS}$ = V_{IH} Vout = Vss to Vcc
Operating power supply current	I_{CC}	—	70	120	mA	$\overline{CS}$ = V_{IL}, Iout = 0 mA, min cycle
Standby power supply current	I_{SB}	—	30	60	mA	$\overline{CS}$ = V_{IH}, min cycle
Standby power supply current (1)	I_{SB1}	—	0.02	2.0	mA	$\overline{CS}$ ≥ Vcc –0.2 V
	I_{SB1}*2	—	—	200*2	µA	0 V ≤ Vin ≤ 0.2 V or Vin ≥ Vcc –0.2 V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4.0 mA

Notes: *1. Typical limits are at V_{CC} = 5.0 V, Ta = 25°C and specified loading.
*2. LJP-version

Capacitance (Ta = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	Cin	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	11	pF	Vout = 0 V

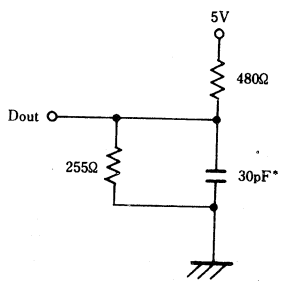
Note: This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

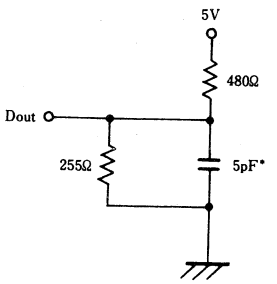
Test Conditions

Input pulse levels:	Vss to 3.0 V
Input rise and fall times:	5 ns
Input and output timing reference levels:	1.5 V
Output load:	See figures

Output Load (A)



Output Load (B)
(for t_{CHZ}, t_{CLZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ})



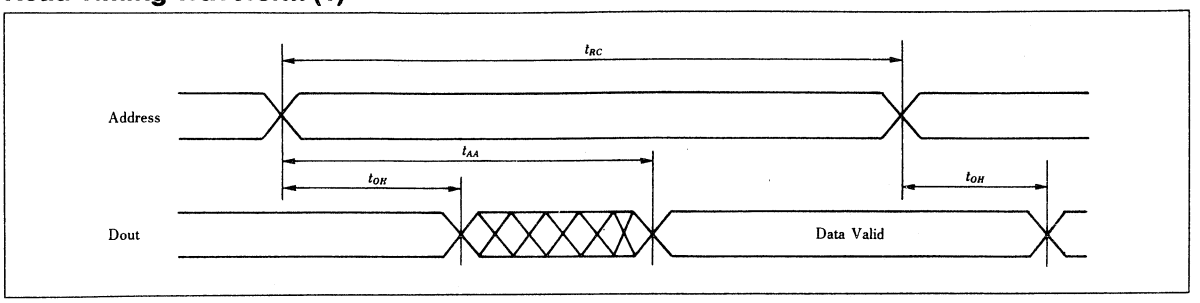
Note: * Including scope & Jig.

Read Cycle

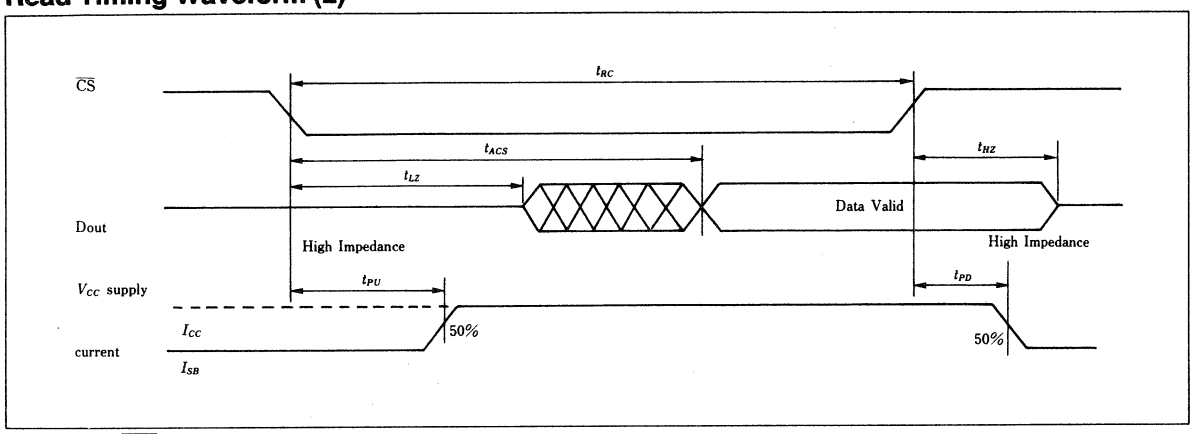
Item	Symbol	HM624257-35		HM624257-45		Unit
		Min	Max	Min	Max	
Read cycle time	t_{RC}	35	—	45	—	ns
Address access time	t_{AA}	—	35	—	45	ns
Chip select access time	t_{ACS}	—	35	—	45	ns
Output hold from address change	t_{OH}	5	—	5	—	ns
Chip selection to output in Low-Z	t_{LZ}*1	5	—	5	—	ns
Chip deselection to output in High-Z	t_{HZ}*1	0	20	0	20	ns
Chip selection to power up time	t_{PU}	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	30	—	30	ns

Note: *1. Transition is measured ±200 mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

Read Timing Waveform (1) *1 *2



Read Timing Waveform (2) *1 *3



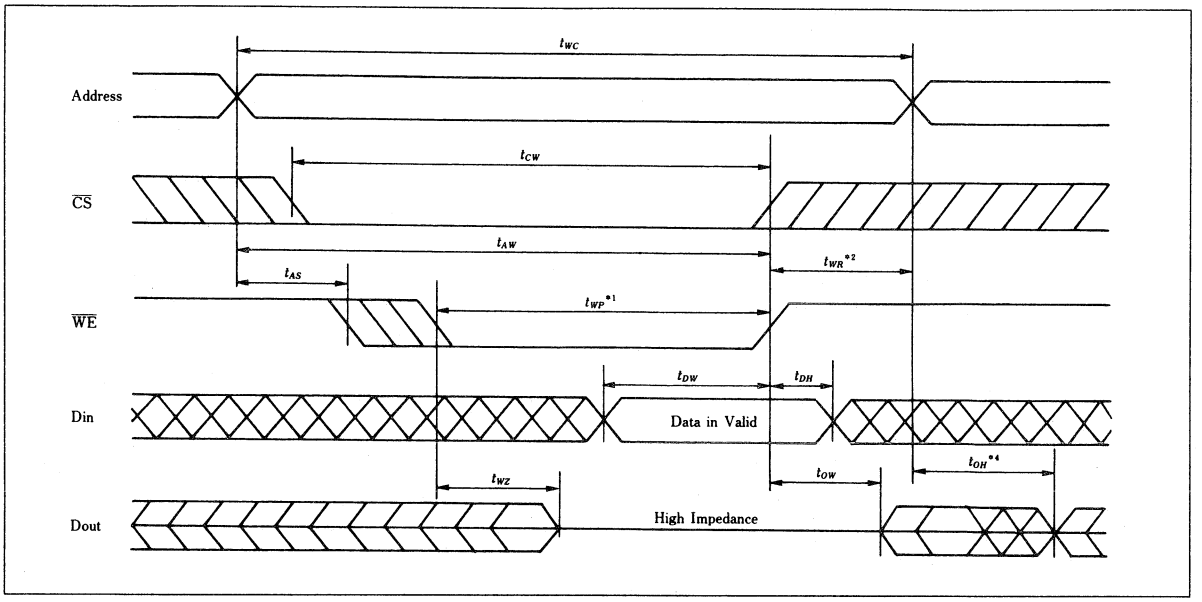
Notes: *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address valid prior to or coincident with $\overline{CS}$ transition Low.

Write Cycle

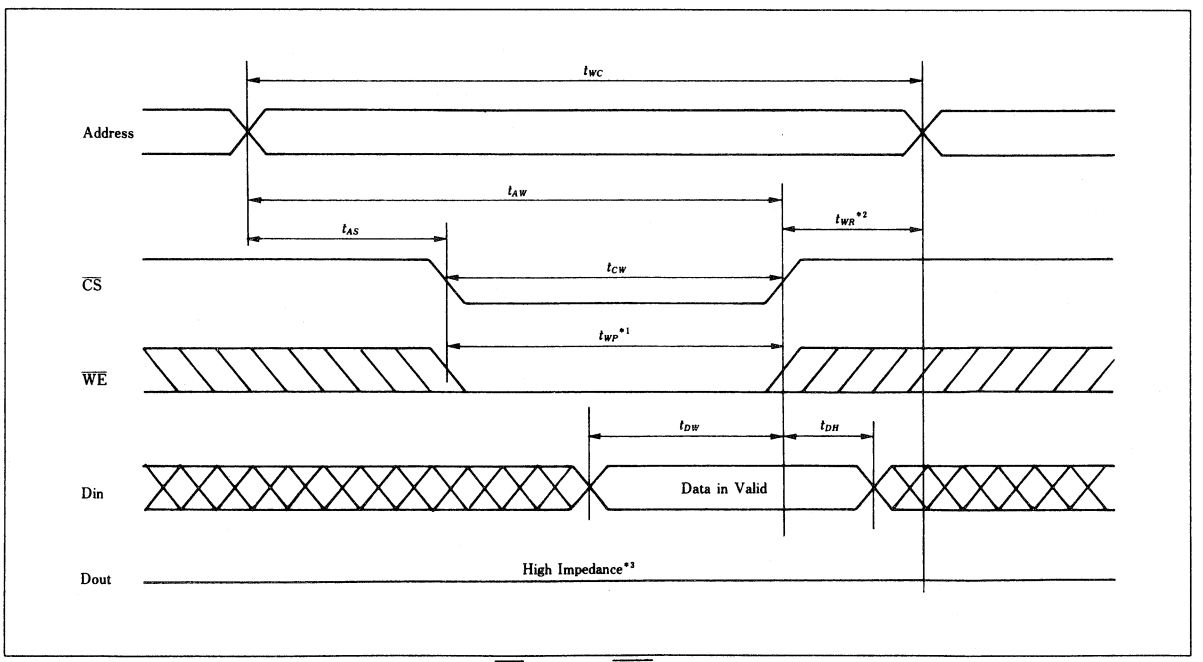
Item	Symbol	HM624257-35		HM624257-45		Unit
		Min	Max	Min	Max	
Write cycle time	t_{WC}	35	—	45	—	ns
Chip selection to end of write	t_{CW}	30	—	40	—	ns
Address valid to end of write	t_{AW}	30	—	40	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	25	—	30	—	ns
Write recovery time	t_{WR}	3	—	3	—	ns
Data valid to end of write	t_{DW}	20	—	25	—	ns
Data hold time	t_{DH}	3	—	3	—	ns
Write enabled to output in High-Z	t_{WZ}*1	0	15	0	20	ns
Output active from end of write	t_{OW}*1	5	—	5	—	ns

Note: *1. Transistion is measured ± 200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes: *1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

*3. If the $\overline{CS}$ low Transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.

*4. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

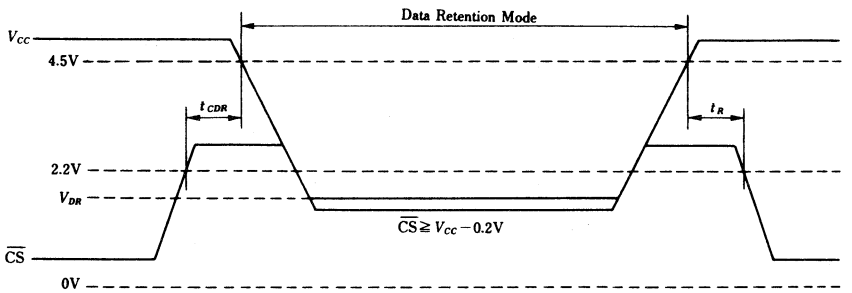
Low Vcc Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

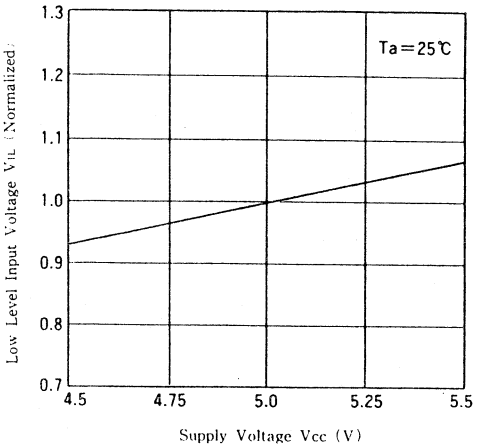
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Vcc for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V,
Data retention current	I_{CCDR}	—	2	100*1	µA	Vin ≥ Vcc – 0.2 V or
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	0 V ≤ Vin ≤ 0.2 V
Operation recovery time	t_R	5	—	—	ms	

Note: *1. Vcc = 3.0V.

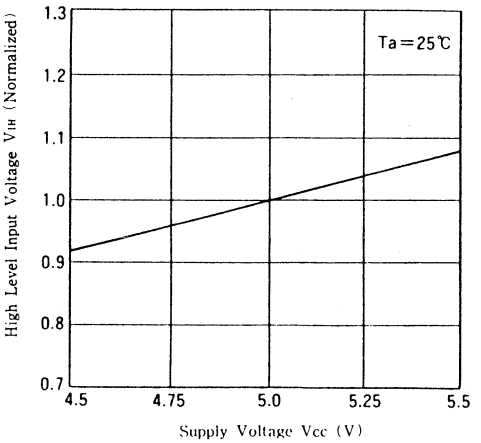
Low Vcc Data Retention Timing Waveform



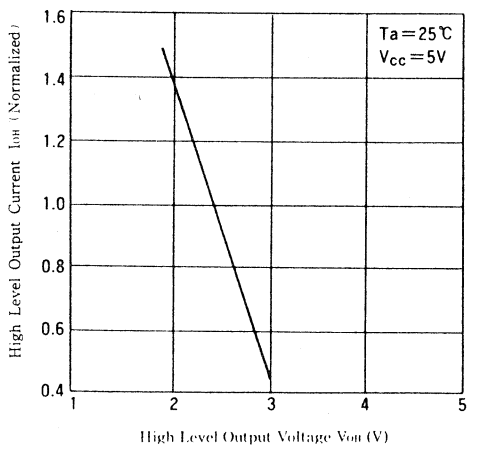
LOW LEVEL INPUT VOLTAGE VS. SUPPLY VOLTAGE



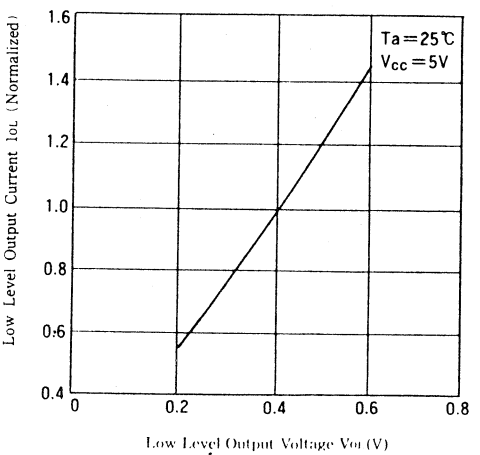
HIGH LEVEL INPUT VOLTAGE VS. SUPPLY VOLTAGE



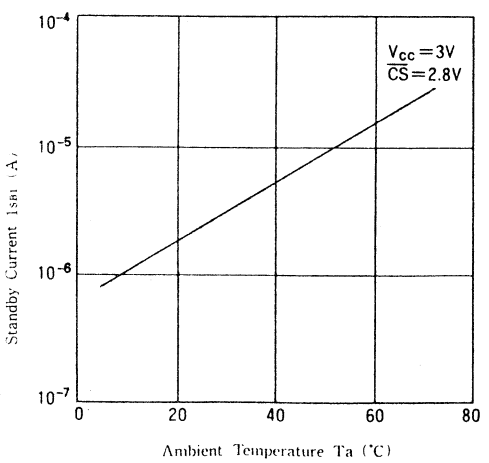
HIGH LEVEL OUTPUT CURRENT VS. HIGH LEVEL OUTPUT VOLTAGE



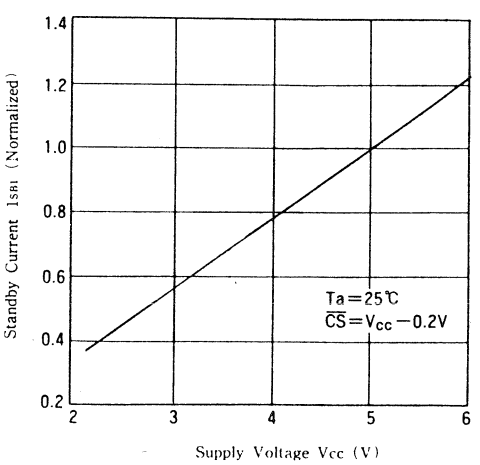
LOW LEVEL OUTPUT CURRENT VS. LOW LEVEL OUTPUT VOLTAGE



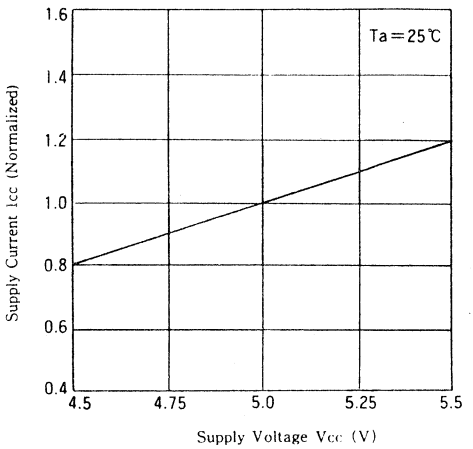
STANDBY CURRENT VS. AMBIENT TEMPERATURE



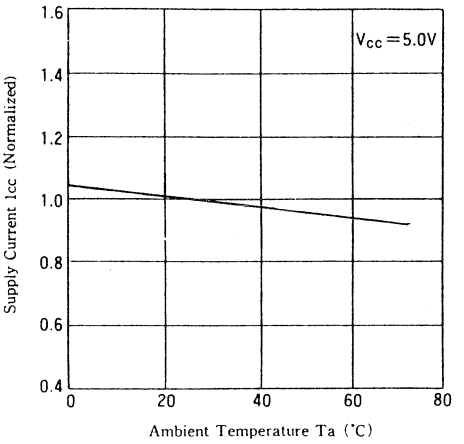
STANDBY CURRENT VS. SUPPLY VOLTAGE



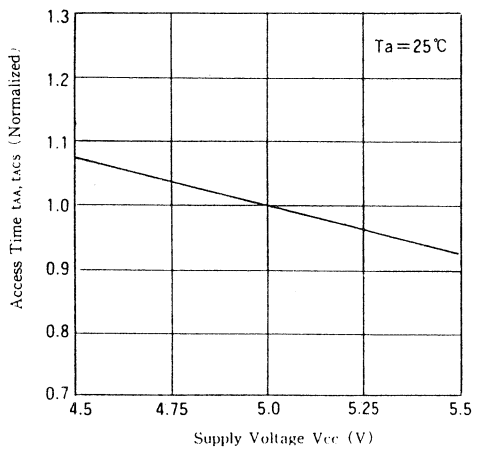
SUPPLY CURRENT VS. SUPPLY VOLTAGE



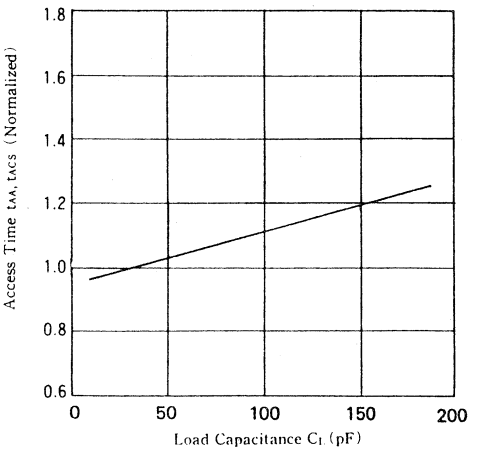
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



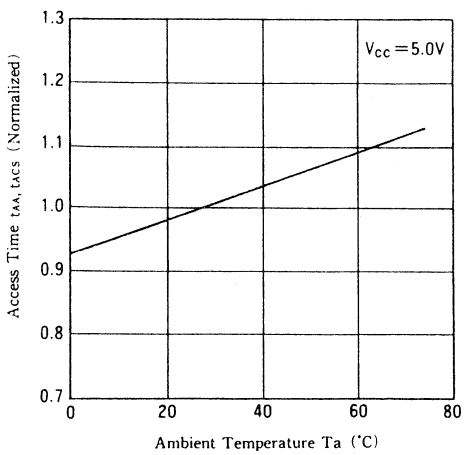
ACCESS TIME VS. SUPPLY VOLTAGE



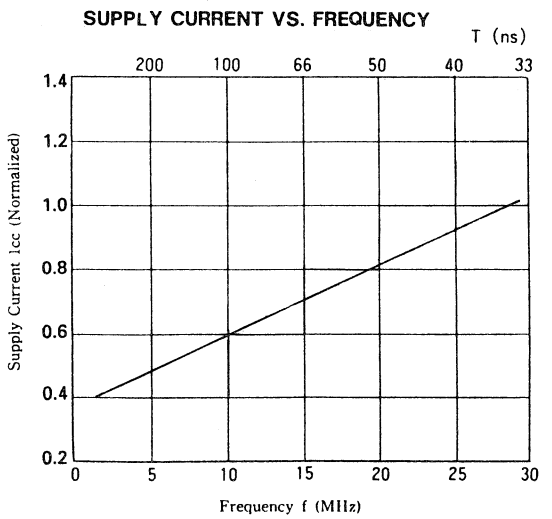
ACCESS TIME VS. LOAD CAPACITANCE



ACCESS TIME VS. AMBIENT TEMPERATURE



SUPPLY CURRENT VS. FREQUENCY



HM624257A Series — Preliminary

262,144-word × 4-bit High Speed CMOS Static RAM

The Hitachi HM624257A is a high speed 1 M Static RAM organized as 256-kword × 4-bit. It realizes high speed access time (20/25/35 ns) and low power consumption, employing the advanced CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM624257A, packaged in a 400-mil plastic SOJ is available for high density mounting.

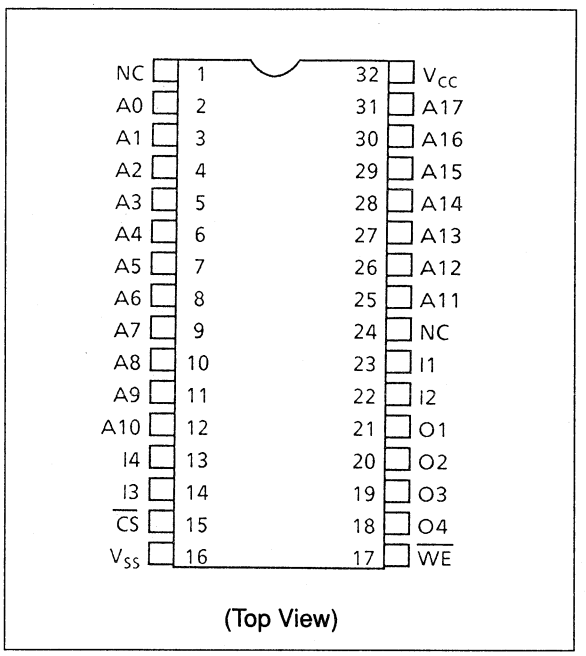
Features

- Single 5 V supply and high density 32-pin package (DIP)
- High speed
  Access time: 20/25/35 ns (maximum)
- Low power dissipation
  Active mode: 350 mW (typical)
  Standby mode: 100 µW (typical)
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible
  All inputs and outputs

Ordering Information

Type No.	Access time	Package
HM624257AJP-20	20 ns	400-mil 32-pin plastic SOJ (CP-32D)
HM624257AJP-25	25 ns	
HM624257AJP-35	35 ns	
HM624257ALJP-20	20 ns	
HM624257ALJP-25	25 ns	
HM624257ALJP-35	35 ns	

Pin Arrangement



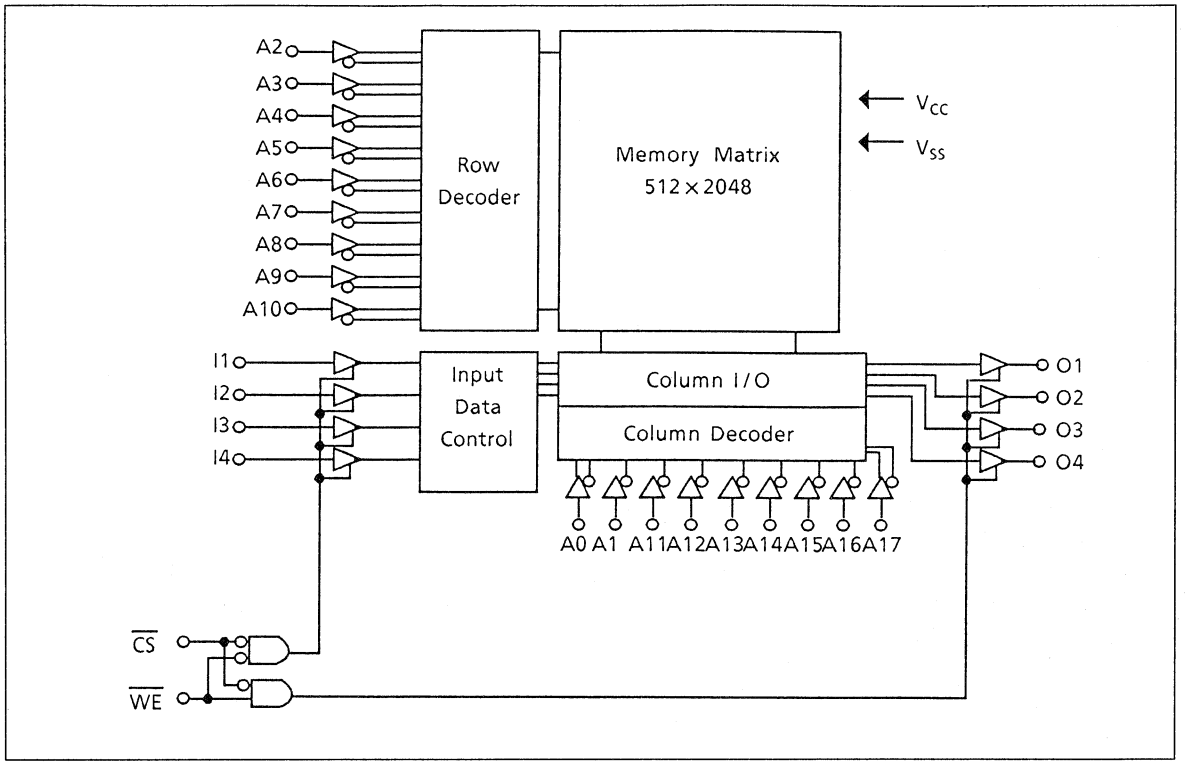
(Top View)

Pin Description

Pin name	Function
A0 – A17	Address
I1 – I4	Data input
O1 – O4	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	Vin	–0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–10 to +85	°C

Note: 1. Vin min = –2.0 V for pulse width ≤ 10 ns.

Function Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} current	Dout pin	Ref. cycle
H	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	I_{CC}	Dout	Read cycle (1) – (2)
L	L	Write	I_{CC}	High-Z	Write cycle (1) – (2)

Note: X : H or L

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: 1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM624257A–20			HM624257A–25/35				
Parameter	Symbol	Min	Typ*1	Max	Min	Typ*1	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	—	—	2.0	µA	V_{CC} = max Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	2.0	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current	I_{CC}	—	—	150	—	—	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, min cycle
Standby power supply current	I_{SB}	—	—	60	—	—	40	mA	$\overline{CS}$ = V_{IH}, min cycle
Standby power supply current (1)	I_{SB1}	—	0.02	2.0	—	0.02	2.0	mA	$\overline{CS}$ ≥ V_{CC} –0.2 V 0 V ≤ Vin ≤ 0.2 V or Vin ≥ V_{CC} –0.2V
	I_{SB1}*2	—	—	100*2	—	—	100*2	µA	
Output low voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH} = –4 mA

Notes: 1. Typical limits are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.
2. LJP version

Capacitance (Ta = 25°C, f = 1 MHz)

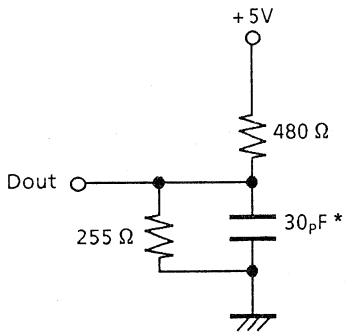
Parameter	Symbol	Min	Max	Unit	Test conditions
Input capacitance	Cin	—	5	pF	Vin = 0 V
Output capacitance	Cont	—	8	pF	Vout = 0 V

Note: 1. This parameter is sampled and not 100% tested.

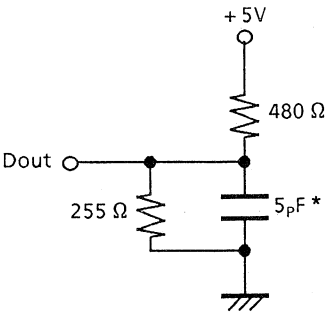
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0 V to 3.0 V
- Input rise and fall times: 4 ns
- Input timing reference levels: 1.5 V
- Output timing reference levels: 1.5 V
- Output load: See figures



Output Load (A)
* Including scope & jig



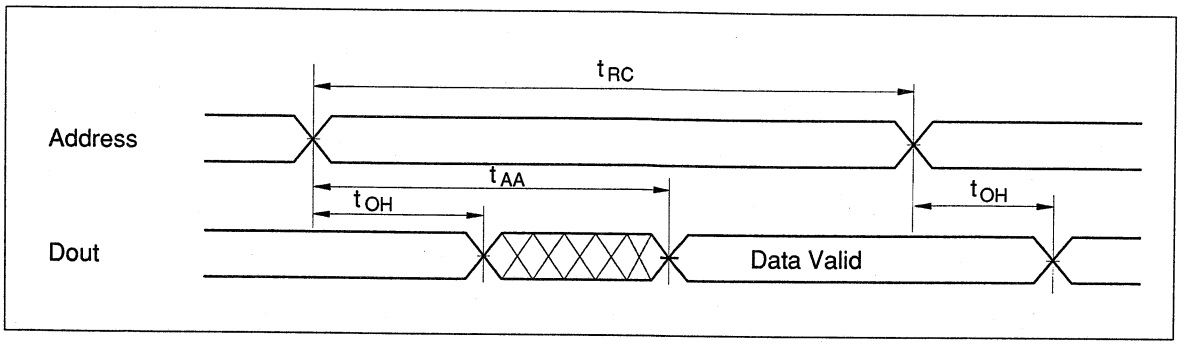
Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW})

Read Cycle

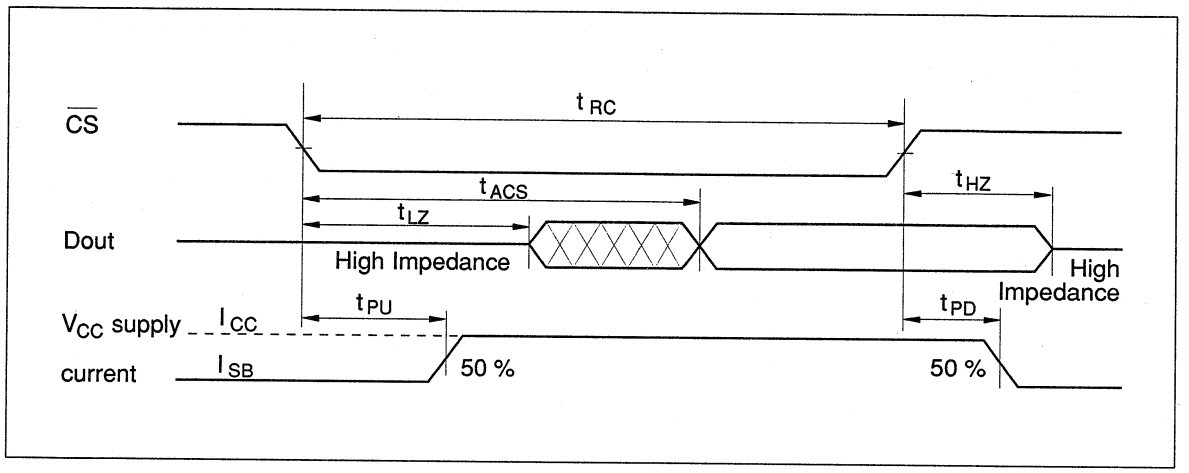
		HM624257A-20		HM624257A-25		HM624257A-35		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	20	—	25	—	35	—	ns
Address access time	t_{AA}	—	20	—	25	—	35	ns
Chip select access time	t_{ACS}	—	20	—	25	—	35	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip selection to output in low-Z	t_{LZ}*1	5	—	5	—	5	—	ns
Chip deselection to output in high-Z	t_{HZ}*1	0	10	0	12	0	15	ns
Chip selection to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	12	—	15	—	25	ns

Notes: 1. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *3



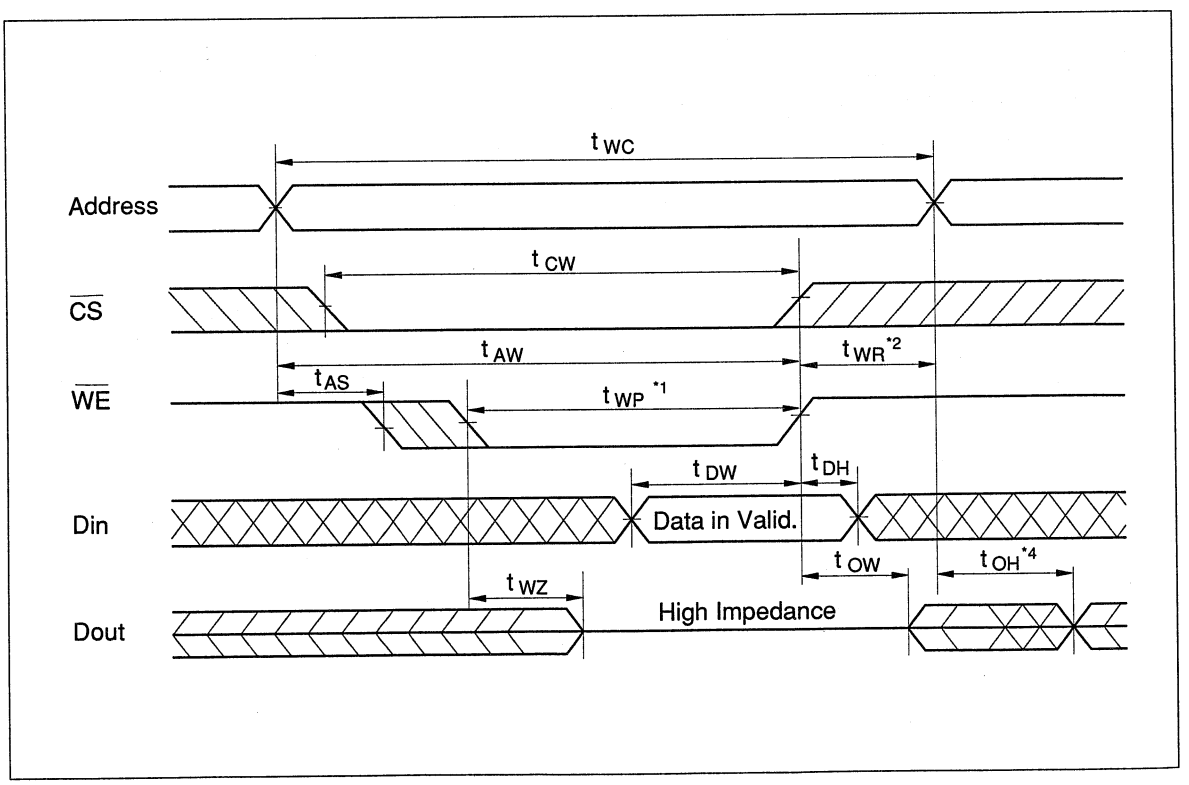
Notes: 1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition Low.

Write Cycle

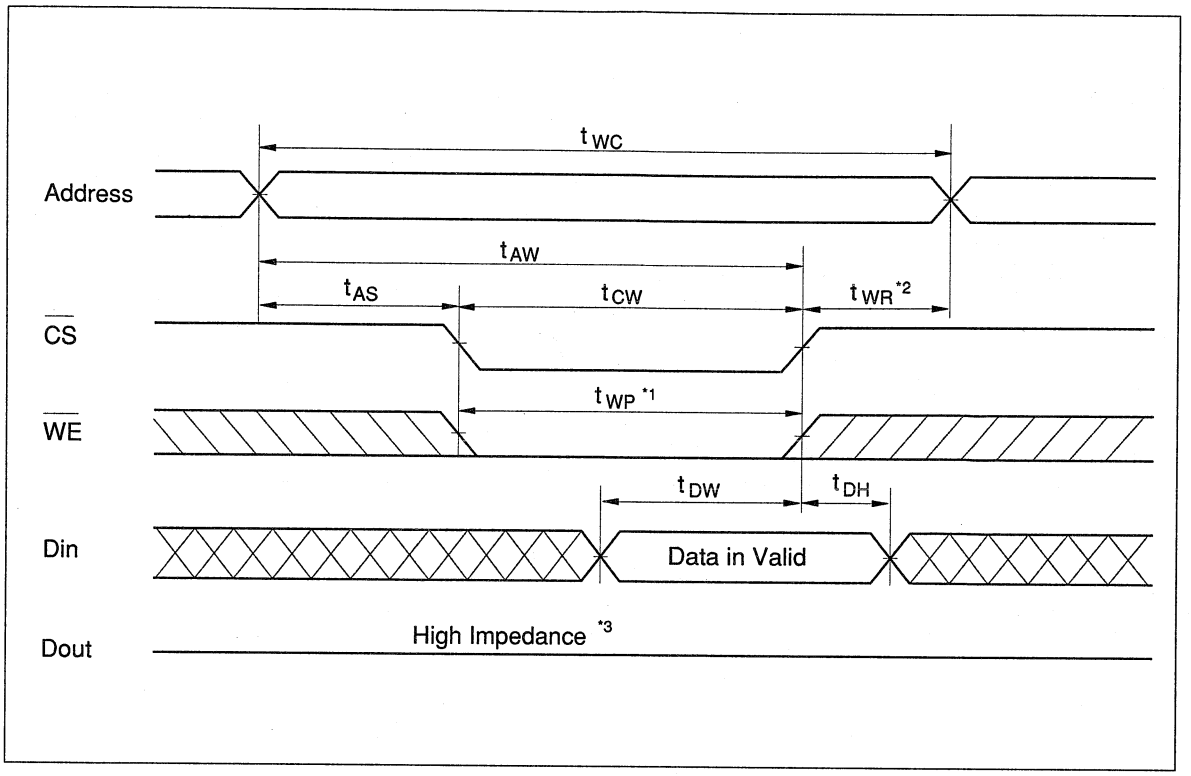
Parameter	Symbol	HM624257A-20		HM624257A-25		HM624257A-35		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	t_{WC}	20	—	25	—	35	—	ns
Chip selection to end of write	t_{CW}	15	—	17	—	25	—	ns
Address valid to end of write	t_{AW}	16	—	20	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	15	—	17	—	25	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Data valid to end of write	t_{DW}	12	—	15	—	20	—	ns
Data hold time	t_{DH}	0	—	0	—	0	—	ns
Write enabled to output in high-Z	t_{WZ}*1	0	12	0	15	0	15	ns
Output active from end of write	t_{OW}*1	0	—	0	—	0	—	ns

Note: 1. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes:
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
4. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

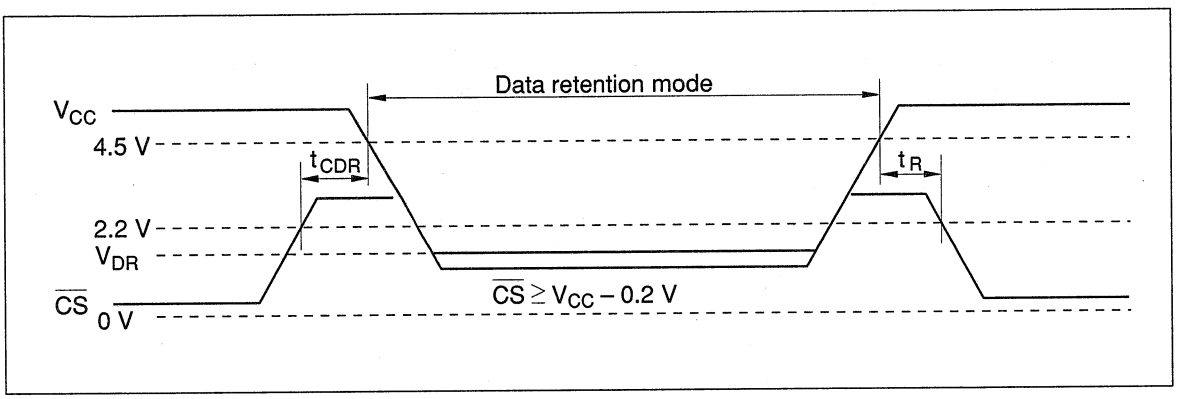
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC}$ –0.2 V, Vin ≥ V_{CC} –0.2 V or 0 V ≤ Vin ≤ 0.2 V
Data retention current	I_{CCDR}	—	2	50*1	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

Note: 1. V_{CC} = 3.0 V

Low V_{CC} data Retention Timing Waveform



HM621100A Series

1048576-word × 1-bit High Speed CMOS Static RAM

The Hitachi HM621100A is a high speed 1M Static RAM organized as 1048576-word × 1-bit. It realizes high speed access time (20/25/35 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.
The HM621100A, packaged in a 400-mil plastic SOJ is available for high density mounting.

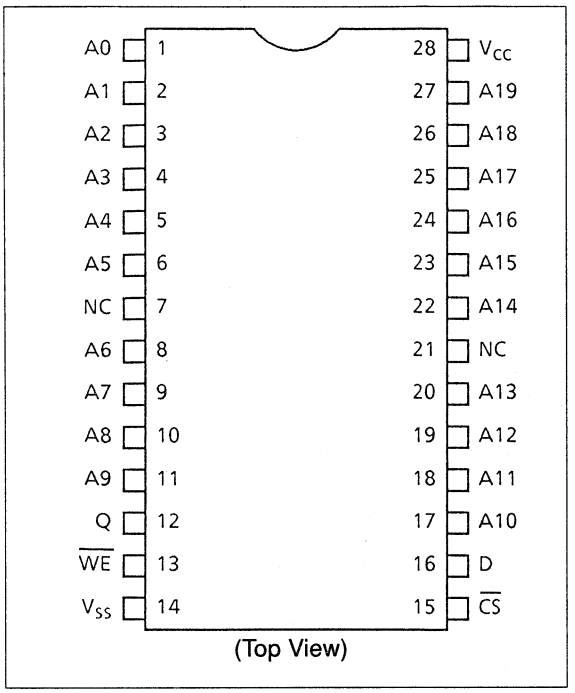
Features

- Single 5 V supply and high density 28-pin package (DIP and SOJ)
- High speed
  Access time: 20 ns/25 ns/35 ns (maximum)
- Low power dissipation
  Active mode: 350 mW (typical)
  Standby mode: 100 µW (typical)
- Completely static memory required
  No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible
  All inputs and outputs

Ordering Information

Type No.	Access time	Package
HM621100AP-20	20 ns	400-mil 28-pin plastic DIP (DP-28C)
HM621100AP-25	25 ns	
HM621100AP-35	35 ns	
HM621100ALP-20	20 ns	
HM621100ALP-25	25 ns	
HM621100ALP-35	35 ns	
HM621100AJP-20	20 ns	400-mil 28-pin plastic SOJ (CP-28D)
HM621100AJP-25	25 ns	
HM621100AJP-35	35 ns	
HM621100ALJP-20	20 ns	
HM621100ALJP-25	25 ns	
HM621100ALJP-35	35 ns	

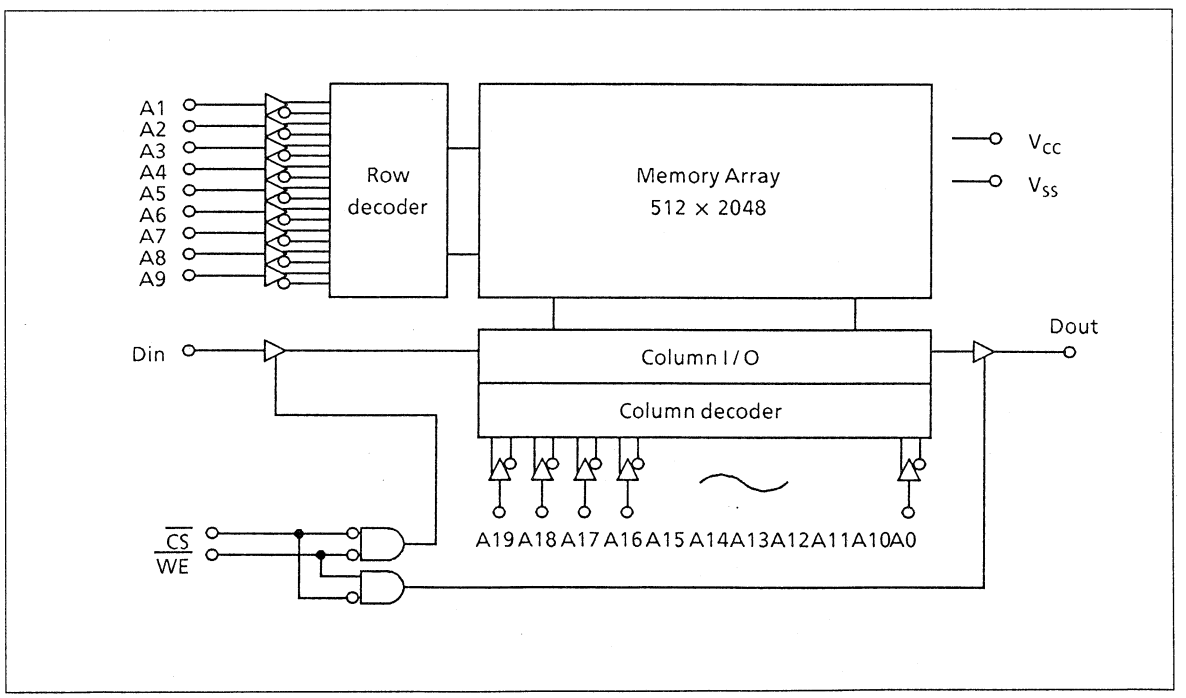
Pin Arrangement (DIP and SOJ)



Pin Description

Pin Name	Function
A0 – A19	Address
D	Input
Q	Output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} current	Output pin	Ref. cycle
H	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	I_{CC}	Dout	Read cycle
L	L	Write	I_{CC}	High-Z	Write cycle

Note: 1. X : H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	Vin	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C

Note: 1. Vin min = −2.0 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	−0.5*1	—	0.8	V

Note: 1. V_{IL} min = −2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM621100A-20			HM621100A-25/35				
Parameter	**Symbol**	**Min**	**Typ*1**	**Max**	**Min**	**Typ*1**	**Max**	**Unit**	**Test conditions**
Input leakage current	$\|I_{LI}\|$	—	—	2.0	—	—	2.0	µA	V_{CC} = max Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	2.0	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current	I_{CC}	—	—	150	—	—	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, min cycle
Standby power supply current	I_{SB}	—	—	60	—	—	40	mA	$\overline{CS}$ = V_{IH}, min cycle
Standby power supply current (1)	I_{SB1}*2	—	0.02	2.0	—	0.02	2.0	mA	$\overline{CS}$ ≥ V_{CC} –0.2 V 0 V ≤ Vin ≤ 0.2 V or Vin ≥ V_{CC} –0.2 V
	I_{SB1}*3	—	—	100	—	—	100	µA	
Output low voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH} = –4 mA

Notes: 1. Typical limits are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.
2. P and JP version.
3. LP and LJP version.

Capacitance (Ta = 25°C, f = 1 MHz)

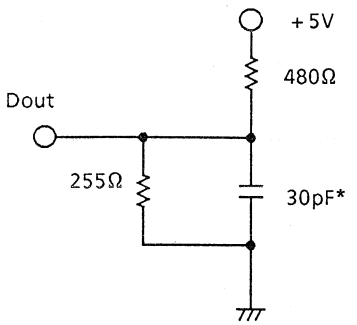
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test conditions**
Input capacitance	Cin	—	5*2	pF	Vin = 0 V
			6*3		
Output capacitance	Cout	—	8	pF	Vout = 0 V

Note: 1. This parameter is sampled and not 100% tested.
2. SOJ package.
3. DIP package.

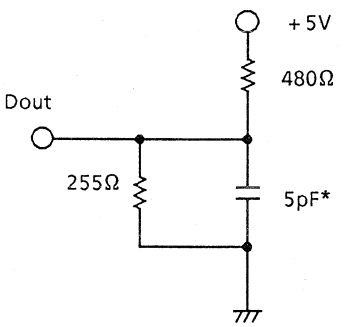
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0 V to 3.0 V
- Input rise and fall times: 4 ns
- Input timing reference levels: 1.5 V
- Output timing reference levels: 1.5 V
- Output load: See figures



Output Load (A)
* Including scope & jig

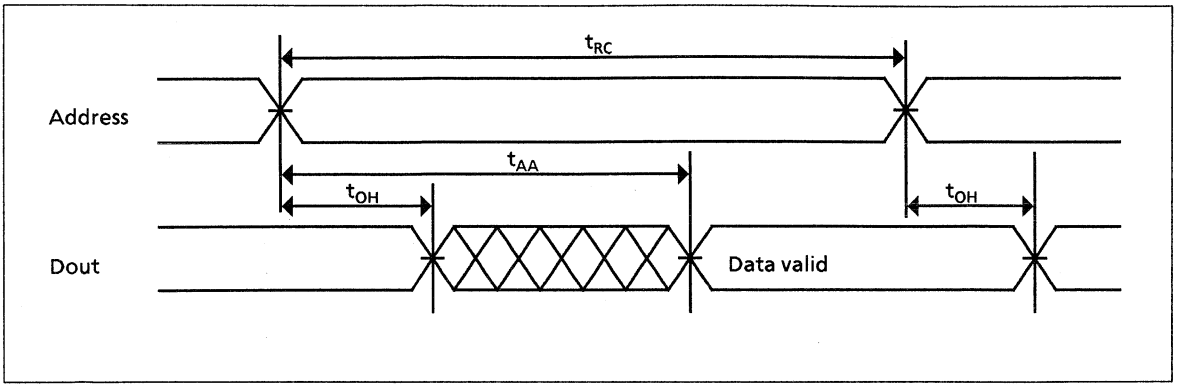


Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW})

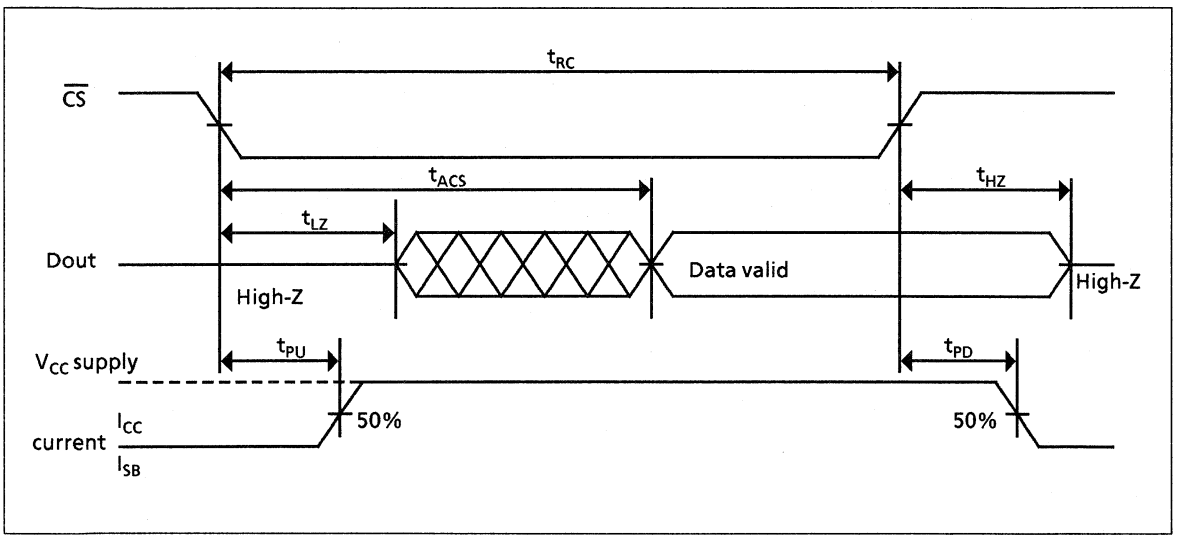
Read Cycle

		HM621100A-20		HM621100A-25		HM621100A-35		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	20	—	25	—	35	—	ns
Address access time	t_{AA}	—	20	—	25	—	35	ns
Chip select access time	t_{ACS}	—	20	—	25	—	35	ns
Chip selection to output in low-Z	t_{LZ}*1	5	—	5	—	5	—	ns
Chip deselection to output in high-Z	t_{HZ}*1	0	10	0	12	0	15	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip selection to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	12	—	15	—	25	ns

Read Timing Waveform (1) *2, *3



Read Timing Waveform (2) *2, *4

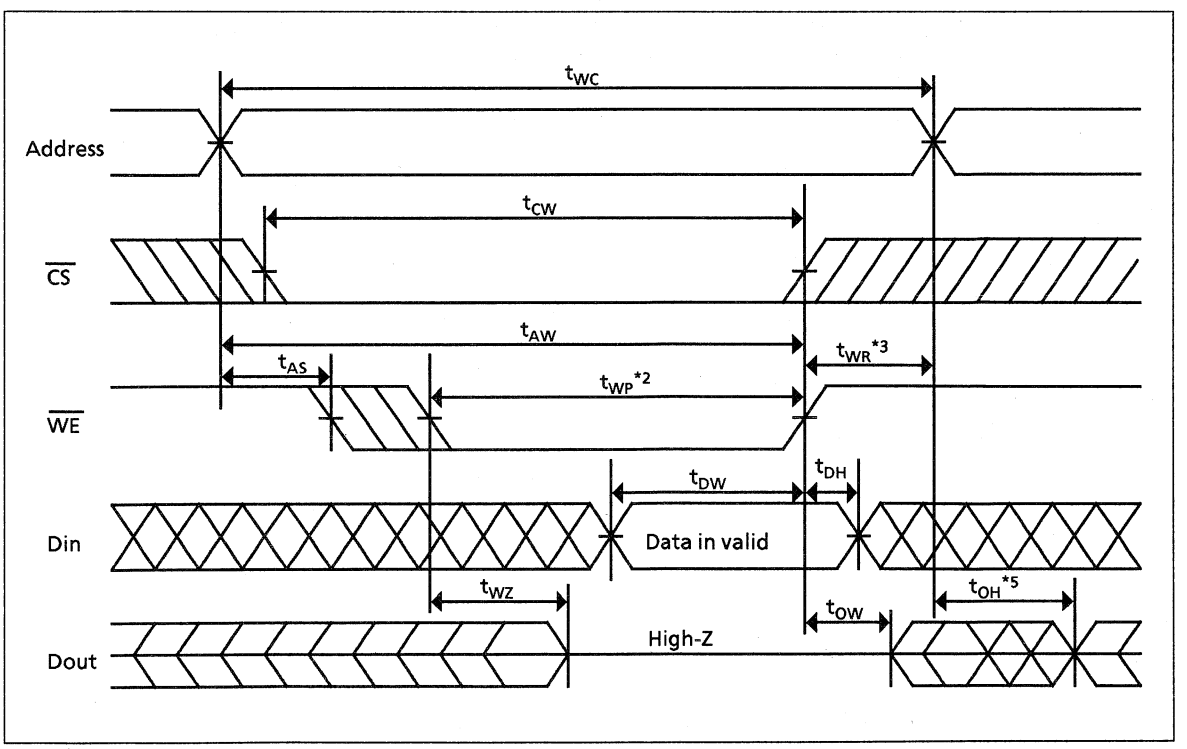


Notes: 1. Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.
2. $\overline{WE}$ is high for read cycle.
3. Device is continuously selected, $\overline{CS} = V_{IL}$.
4. Address valid prior to or coincident with $\overline{CS}$ transition low.

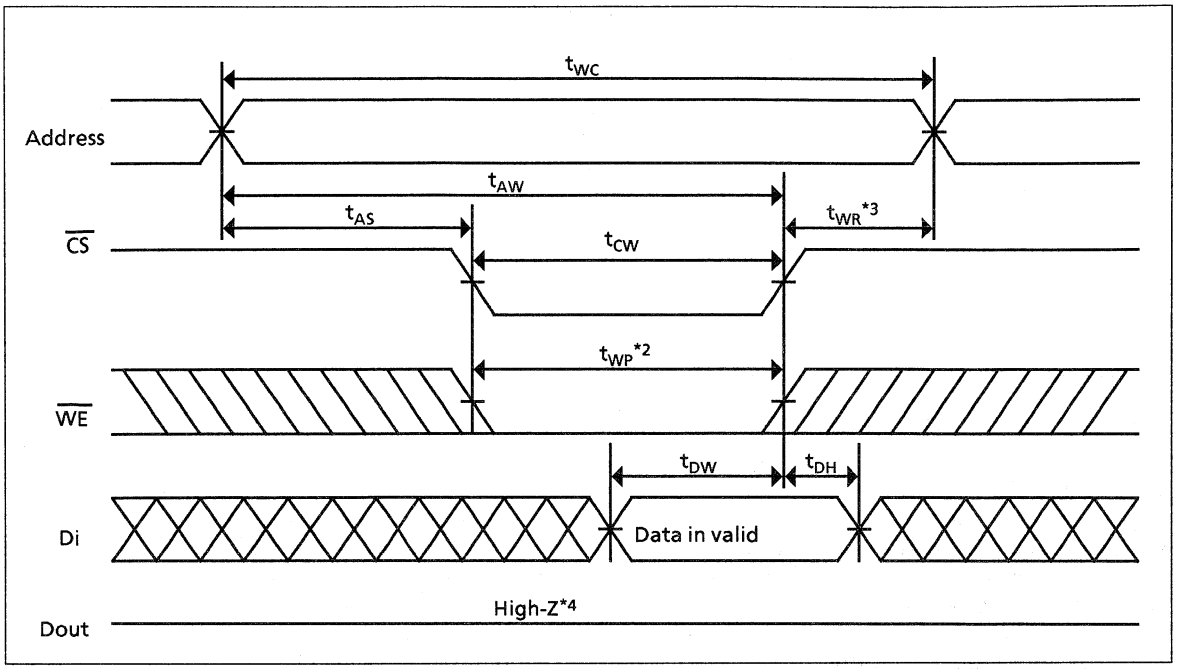
Write Cycle

Parameter	Symbol	HM621100A-20		HM621100A-25		HM621100A-35		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	t_{WC}	20	—	25	—	35	—	ns
Chip selection to end of write	t_{CW}	15	—	17	—	25	—	ns
Address valid to end of write	t_{AW}	16	—	20	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	15	—	17	—	25	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Write to output in high-Z	t_{WZ}*1	0	12	0	15	0	15	ns
Data to write time overlap	t_{DW}	12	—	15	—	20	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*1	0	—	0	—	0	—	ns

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes:
1. Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

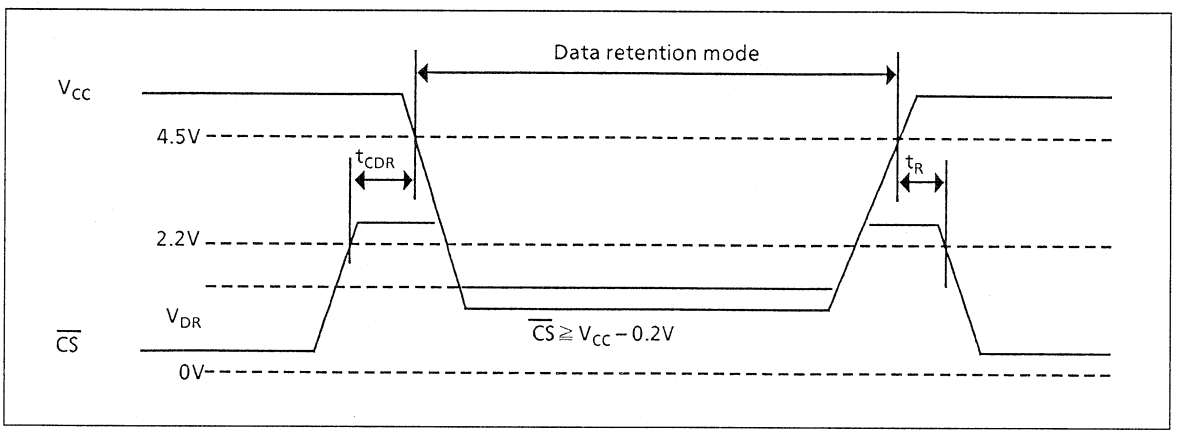
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

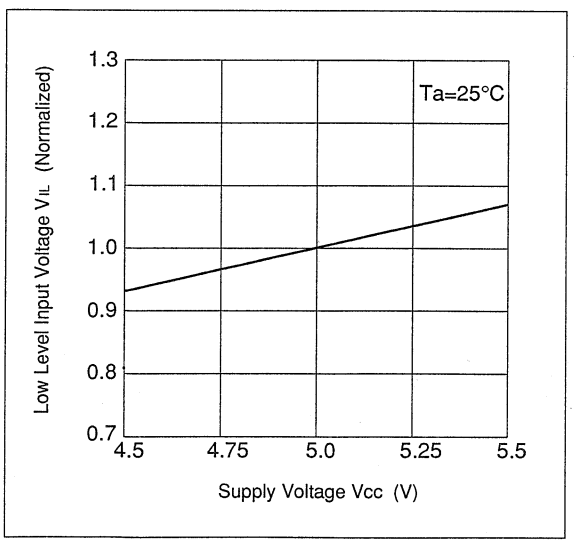
This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, Vin $\geq V_{CC} - 0.2$ V or 0 V $\leq$ Vin $\leq$ 0.2 V
Data retention current	I_{CCDR}	—	2	50*1	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

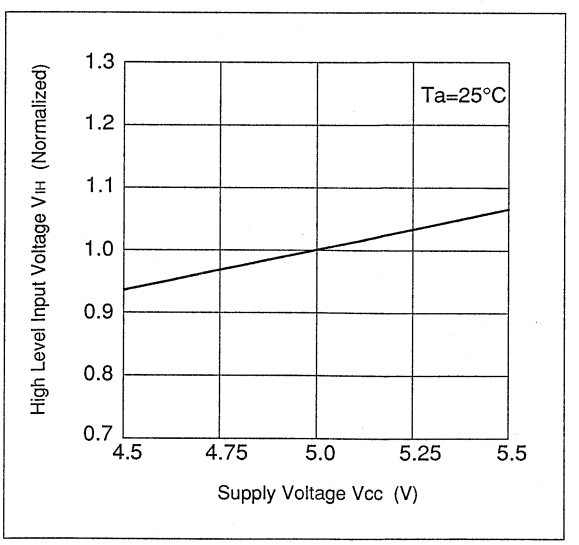
Note: 1. V_{CC} = 3.0 V.

Low V_{CC} Data Retention Timing Waveform

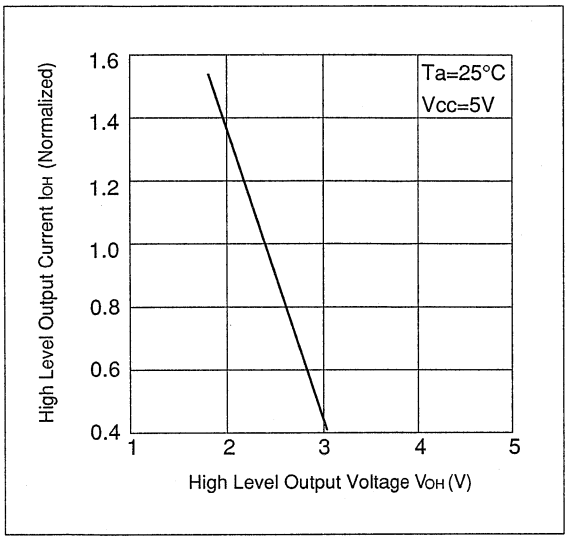




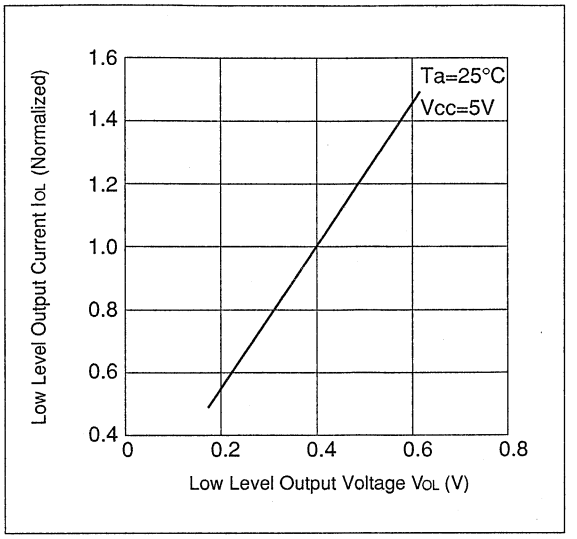
Low Level Input Voltage vs. Supply Voltage



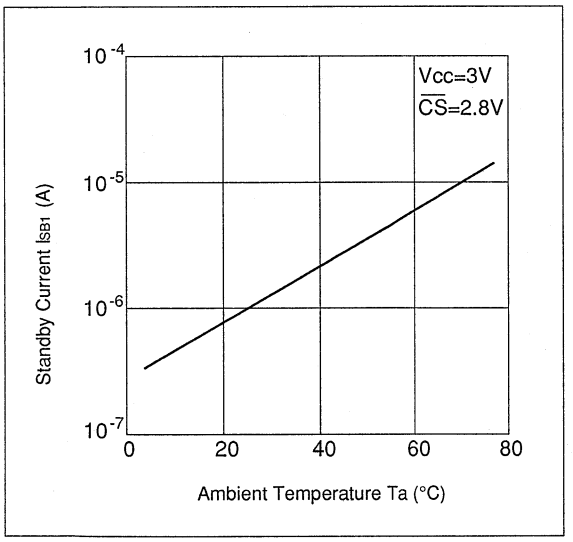
High Level Input Voltage vs. Supply Voltage



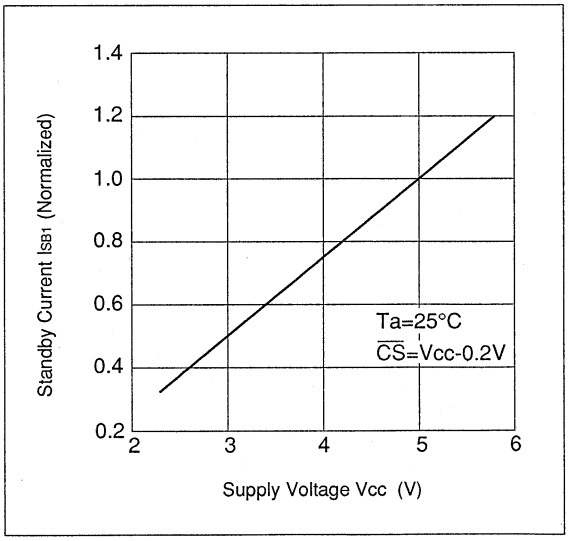
High Level Output Current vs. High Level Output Voltage



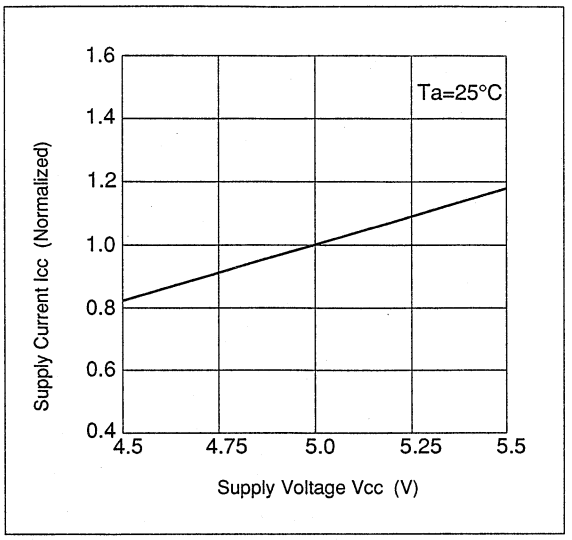
Low Level Output Current vs. Low Level Output Voltage



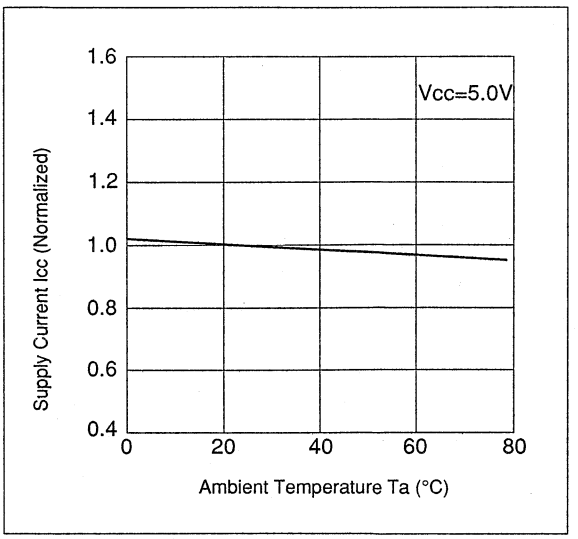
Standby Current vs. Ambient Temperature



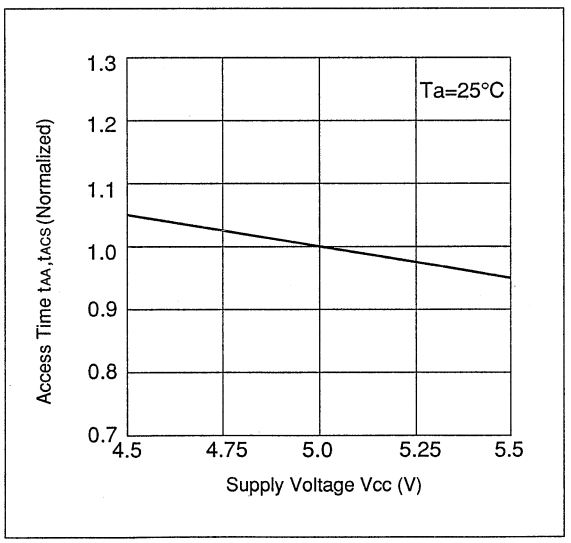
Standby Current vs. Supply Voltage



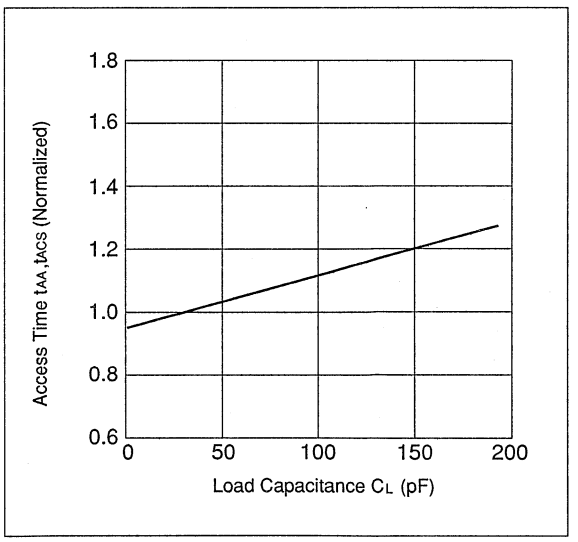
Supply Current vs. Supply Voltage



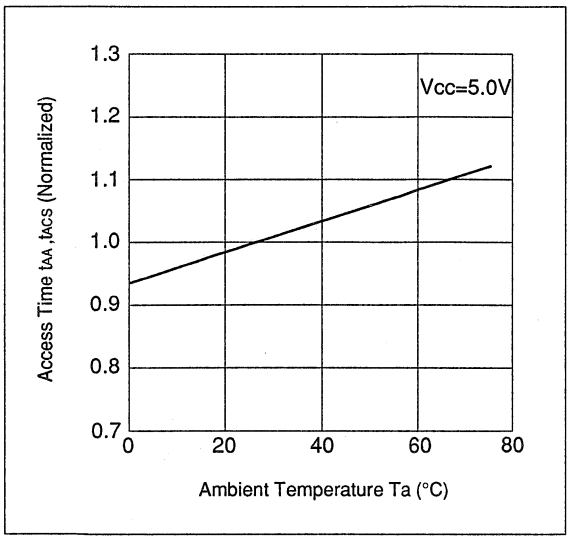
Supply Current vs. Ambient Temperature



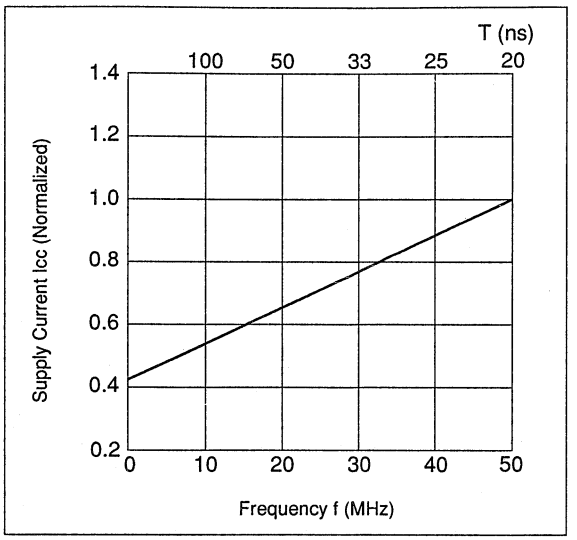
Access Time vs. Supply Voltage



Access Time vs. Load Capacitance



Access Time vs. Ambient Temperature



Supply Current vs. Frequency

HM628512 Series

524288-word × 8-bit High Speed CMOS Static RAM

The Hitachi HM628512 is a 4M-bit static RAM organized 512-kword × 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.5 µm Hi-CMOS process technology. The device, packaged in a 525-mil SOP (foot print pitch width) or 400 mil TSOP TYPE II or 600-mil plastic DIP, is available for high density mounting. LP-version is suitable for battery back up system.

Features

- High speed: Fast access time 55/70/85/100 ns (max)
- Low power
  Standby: 10 µW (typ) (L/L-SL version)
  Operation: 75 mW/MHz (typ)
- Single 5 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation (L/L-SL version)

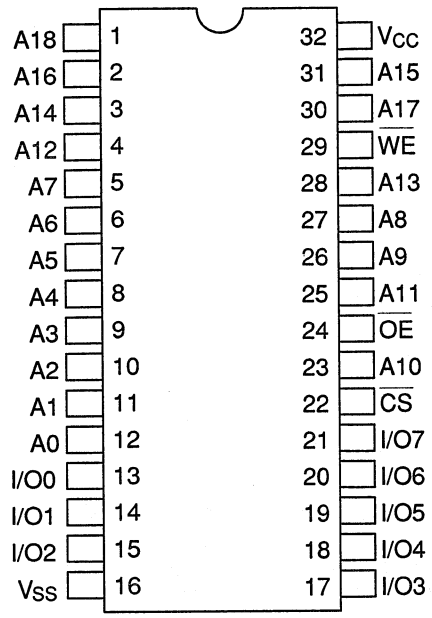
Ordering Information

Type No.	Access time	Package
HM628512P-5	55 ns	600-mil 32-pin plastic DIP (DP-32)
HM628512P-7	70 ns	
HM628512P-8	85 ns	
HM628512P-10	100 ns	
HM628512LP-5	55 ns	
HM628512LP-7	70 ns	
HM628512LP-8	85 ns	
HM628512LP-10	100 ns	
HM628512LP-5SL	55 ns	
HM628512LP-7SL	70 ns	
HM628512LP-8SL	85 ns	
HM628512LP-10SL	100 ns	
HM628512FP-5	55 ns	525-mil 32-pin plastic SOP (FP-32D)
HM628512FP-7	70 ns	
HM628512FP-8	85 ns	
HM628512FP-10	100 ns	
HM628512LFP-5	55 ns	
HM628512LFP-7	70 ns	
HM628512LFP-8	85 ns	
HM628512LFP-10	100 ns	
HM628512LFP-5SL	55 ns	
HM628512LFP-7SL	70 ns	
HM628512LFP-8SL	85 ns	
HM628512LFP-10SL	100 ns	
HM628512LTT-5*1	55 ns	400-mil 32-pin TSOP II (TTP-32D)
HM628512LTT-7*1	70 ns	
HM628512LTT-8*1	85 ns	
HM628512LTT-10*1	100 ns	
HM628512LTT-5SL*1	55 ns	
HM628512LTT-7SL*1	70 ns	
HM628512LTT-8SL*1	85 ns	
HM628512LTT-10SL*1	100 ns	
HM628512LRR-5*1	55 ns	400-mil 32-pin TSOP II reverse (TTP-32DR)
HM628512LRR-7*1	70 ns	
HM628512LRR-8*1	85 ns	
HM628512LRR-10*1	100 ns	
HM628512LRR-5SL*1	55 ns	
HM628512LRR-7SL*1	70 ns	
HM628512LRR-8SL*1	85 ns	
HM628512LRR-10SL*1	100 ns	

Note: 1. Preliminary

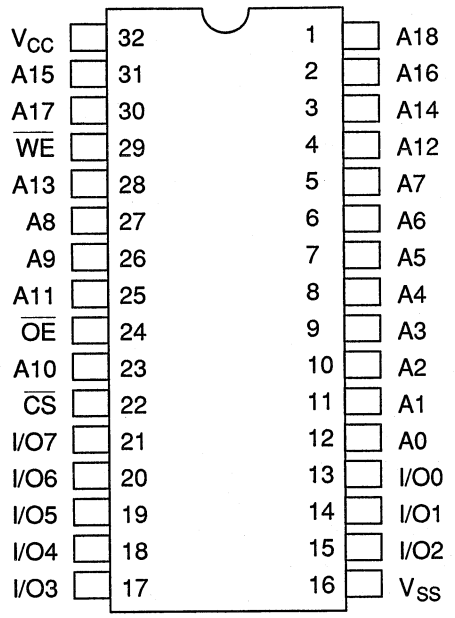
Pin Arrangement

HM628512P/FP/TT Series



(Top View)

HM628512RR Series

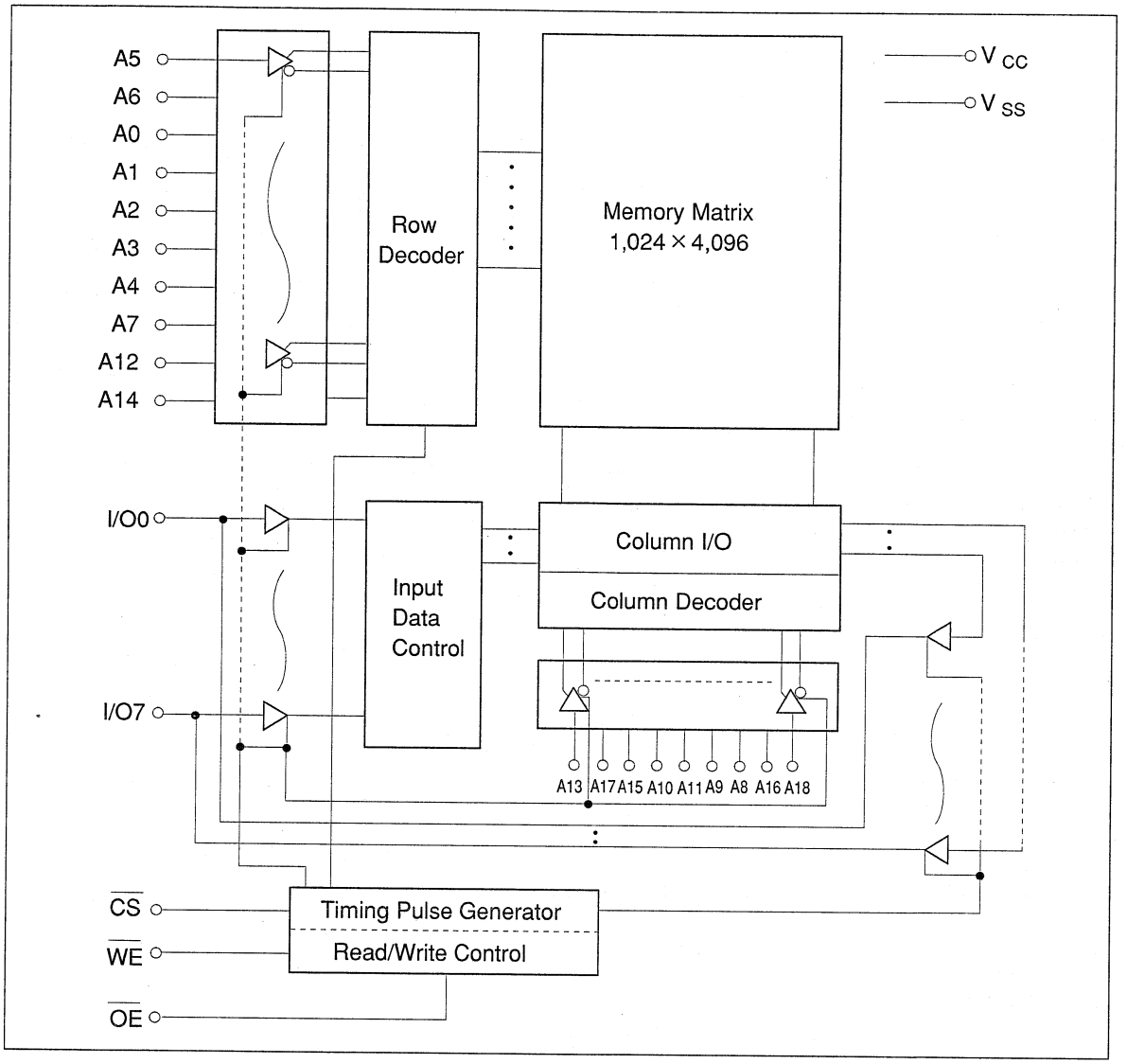


(Top View)

Pin Description

Symbol	Function
A0 – A18	Address
I/O0 – I/O7	Input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Function Table

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	Mode	V_{CC} current	Dout pin	Ref. cycle
X	H	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
H	L	H	Output disable	I_{CC}	High-Z	—
H	L	L	Read	I_{CC}	Dout	Read cycle
L	L	H	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: X: H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5[*1] to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Note: 1. −3.0 V for pulse half-width ≤ 30 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	−0.3[*1]	—	0.8	V

Note: 1. −3.0 V for pulse half-width ≤ 30 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10% , V_{SS} = 0 V)

Item		Symbol	Min	Typ*1	Max	Unit	Test conditions
Input leakage current		$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}
Output leakage current		$\|I_{LO}\|$	—	—	1	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current: DC		I_{CCREAD}	—	10	25	mA	$\overline{CS}$ = V_{IL}, $\overline{WE}$ = V_{IH}, others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA
		$I_{CCWRITE}$	—	18	35	mA	$\overline{CS}$ = V_{IL}, $\overline{WE}$ = V_{IL}, others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA
Operating power supply current	–5	I_{CC1}	—	55	100	mA	Min cycle, duty = 100% $\overline{CS}$ = V_{IL}, others = V_{IH}/V_{IL} $I_{I/O}$ = 0 mA
	–7		—	55	90	mA	
	–8/10		—	55	80	mA	
		I_{CC2}	—	15	35	mA	Cycle time = 1 µs, duty = 100% $I_{I/O}$ = 0 mA, $\overline{CS}$ ≤ 0.2 V V_{IH} ≥ V_{CC} –0.2 V, V_{IL} ≤ 0.2 V
Standby power supply current: DC		I_{SB}	—	1	3	mA	$\overline{CS}$ = V_{IH}
Standby power supply current (1): DC		I_{SB1}	—	0.02	2	mA	Vin ≥ 0 V, $\overline{CS}$ ≥ V_{CC} –0.2 V
			—	2*2	100*2	µA	
			—	2*3	50*3	µA	
Output low voltage		V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage		V_{OH}	2.4	—	—	V	I_{OH} = –1.0 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.
2. This characteristics is guaranteed only for L-version.
3. This characteristics is guaranteed only for L-SL version.

Capacitance (Ta = 25°C, f = 1 MHz)*1

Item	Symbol	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

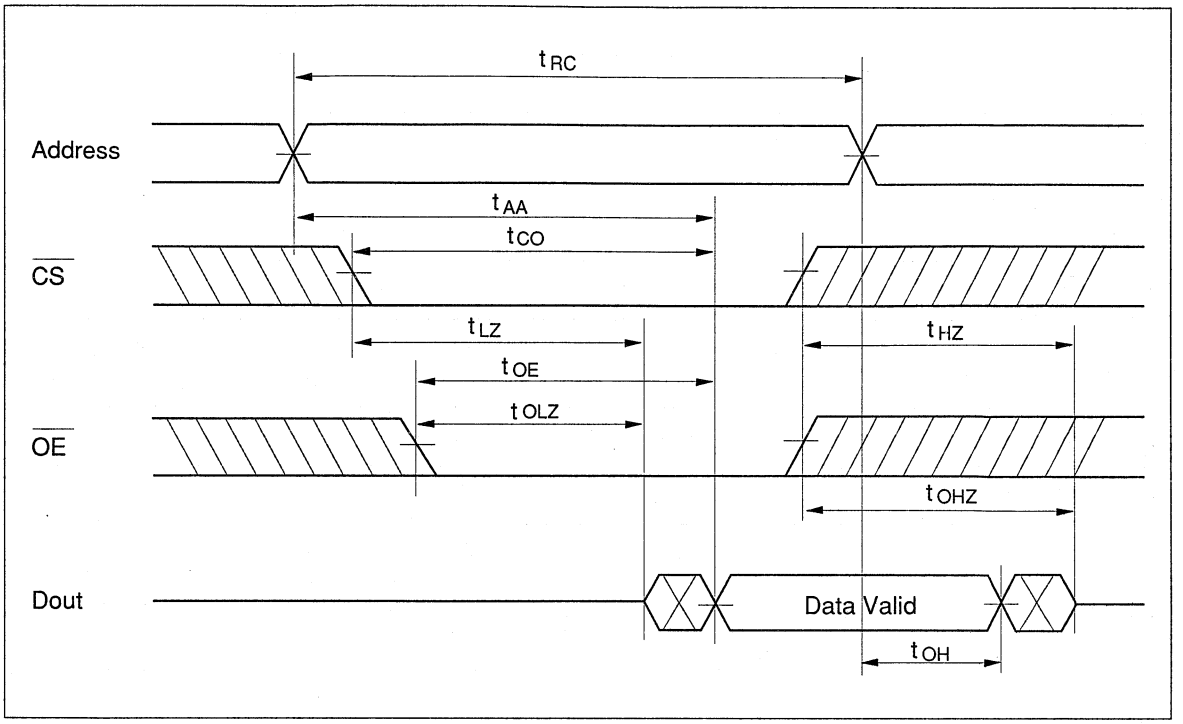
Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input and output timing reference levels: 1.5 V
- Input rise and fall times: 5 ns
- Output load: 1 TTL Gate + C_L (100 pF) (Including scope & jig)

Read Cycle

		HM628512-5		HM628512-7		HM628512-8		HM628512-10			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	55	—	70	—	85	—	100	—	ns	
Address access time	t_{AA}	—	55	—	70	—	85	—	100	ns	
Chip select access time	t_{CO}	—	55	—	70	—	85	—	100	ns	
Output enable to output valid	t_{OE}	—	25	—	35	—	45	—	50	ns	
Chip selection to output in low-Z	t_{LZ}	5	—	10	—	10	—	10	—	ns	1, 2, 3
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	5	—	5	—	ns	1, 2, 3
Chip deselection to output in high-Z	t_{HZ}	0	20	0	25	0	30	0	35	ns	1, 2, 3
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	0	30	0	35	ns	1, 2, 3
Output hold from address change	t_{OH}	10	—	10	—	10	—	10	—	ns	

Read Timing Waveform*4

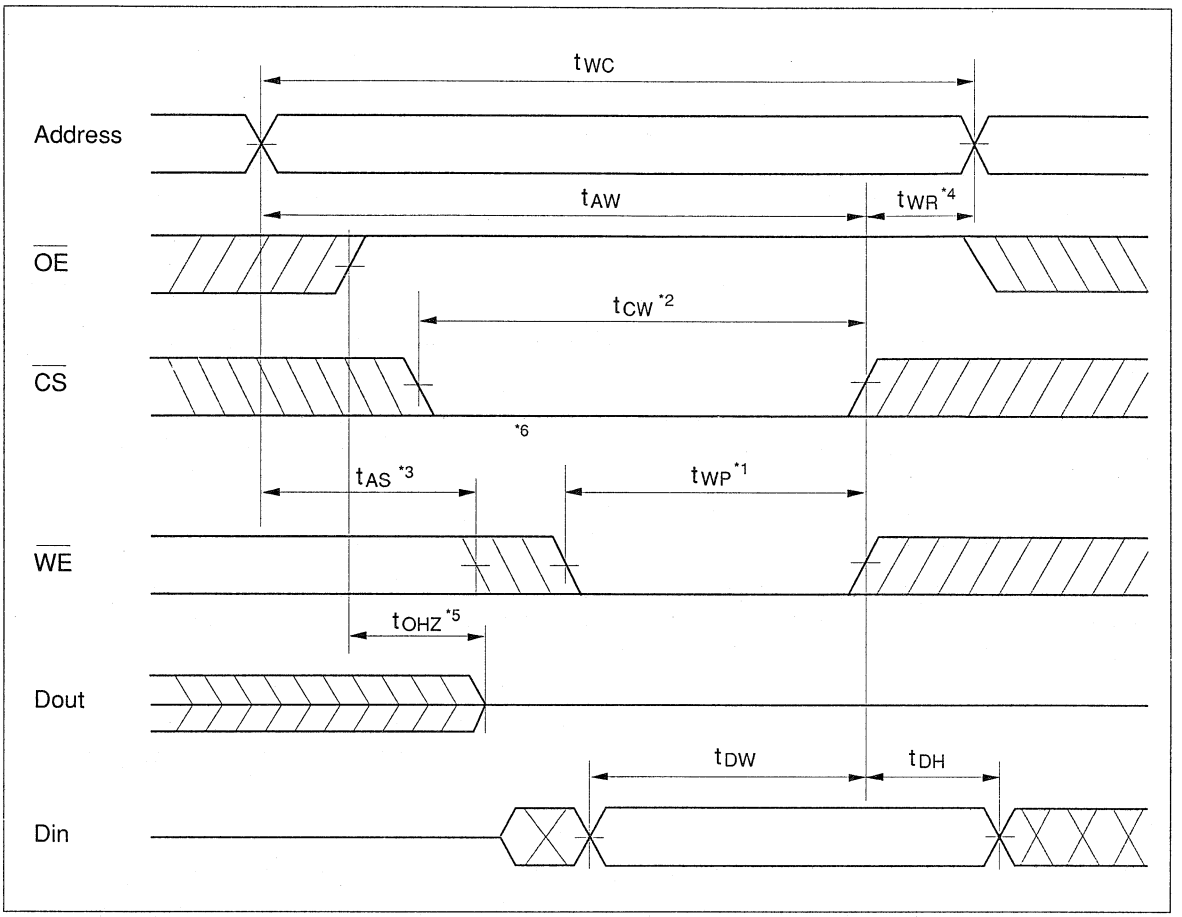


Notes:
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
3. This parameter is sampled and not 100% tested.
4. $\overline{WE}$ is high for read cycle.

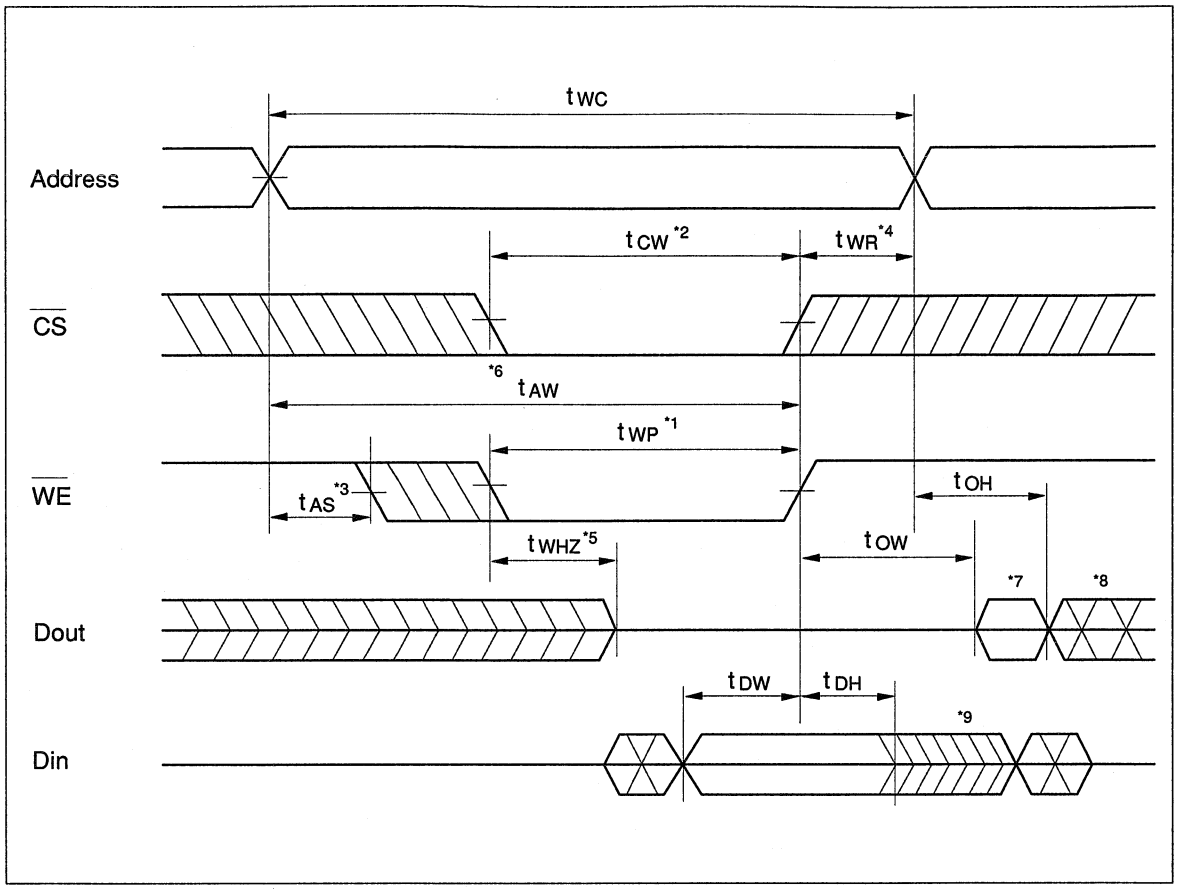
Write Cycle

Item	Symbol	HM628512-5		HM628512-7		HM628512-8		HM628512-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	55	—	70	—	85	—	100	—	ns	
Chip selection to end of write	t_{CW}	50	—	60	—	75	—	80	—	ns	
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address valid to end of write	t_{AW}	50	—	60	—	75	—	80	—	ns	
Write pulse width	t_{WP}	40	—	50	—	55	—	60	—	ns	
Write recovery time	t_{WR}	5	—	5	—	5	—	5	—	ns	
$\overline{WE}$ to output in high-Z	t_{WHZ}	0	20	0	25	0	30	0	35	ns	10
Data to write time overlap	t_{DW}	25	—	30	—	35	—	40	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	5	—	5	—	ns	10

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Write Timing Waveform (2) ($\overline{OE}$ Low Fixed)



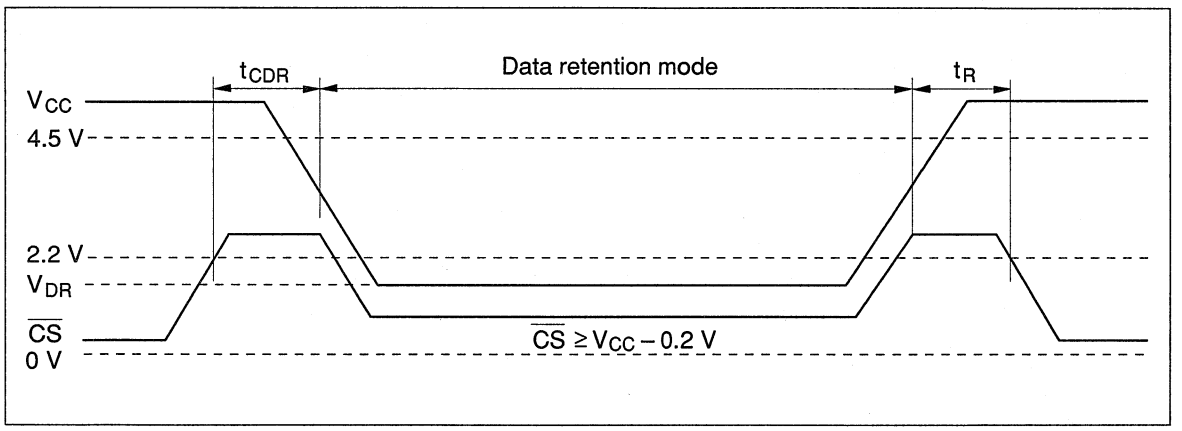
Notes:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CS}$ going low or $\overline{WE}$ going low. A write ends at the earlier transition of $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earlier of $\overline{WE}$ or $\overline{CS}$ going high to the end of write cycle.
5. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
6. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output remain in a high impedance state.
7. Dout is the same phase of the write data of this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
10. This parameter is sampled and not 100% tested.

Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L/L-SL version.

Item	Symbol	Min	Typ	Max	Unit	Test conditions*3
V_{CC} for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC}$ –0.2 V, Vin ≥ 0 V
Data retention current	I_{CCDR}	—	1	50*1	µA	V_{CC} = 3.0 V, Vin ≥ 0 V, $\overline{CS} \geq V_{CC}$ –0.2 V
		—	1	15*2	µA	
Chip select to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	5	—	—	ms	

Low V_{CC} Data Retention Timing Waveform ($\overline{CS}$ Controlled)



Notes: 1. For L-version and 20 µA max. at Ta = 0 to 40°C.
2. For SL-version and 3 µA max. at Ta = 0 to 40°C.
3. $\overline{CS}$ controls address buffer, $\overline{WE}$ buffer, $\overline{OE}$ buffer, and Din buffer. In data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

HM621400 Series — Under development

4,194,304-word × 1-bit High Speed CMOS Static RAM

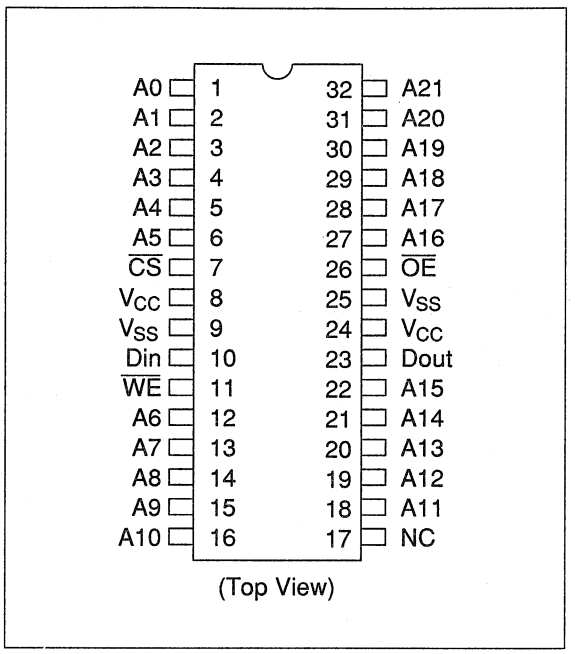
Features

- High speed:
  - Fast access time: 25/30/35/45 ns (max) (P-version)
    30/35/45 ns (max) (LP-version)
- Single 5 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- TTL compatible – All inputs and outputs
- Thin plastic package for high density mounting

Ordering Informations

Type No.	Access time	Package
HM621400JP-25	25 ns	400 mil 32-pin SOJ (CP-32DB)
HM621400JP-30	30 ns	
HM621400JP-35	35 ns	
HM621400JP-45	45 ns	
HM621400JLP-30	30 ns	
HM621400JLP-35	35 ns	
HM621400JLP-45	45 ns	
HM621400P-25	25 ns	400 mil 32-pin TSOP (II) (TTP-32DA)
HM621400P-30	30 ns	
HM621400P-35	35 ns	
HM621400P-45	45 ns	
HM621400LP-30	30 ns	
HM621400LP-35	35 ns	
HM621400LP-45	45 ns	

Pin Arrangement



(Top View)

Pin Description

Pin name	Function
A0 – A21	Address input
Din	Data input
Dout	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

HM624100 Series — Under development

1,048,576-word × 4-bit High Speed CMOS Static RAM

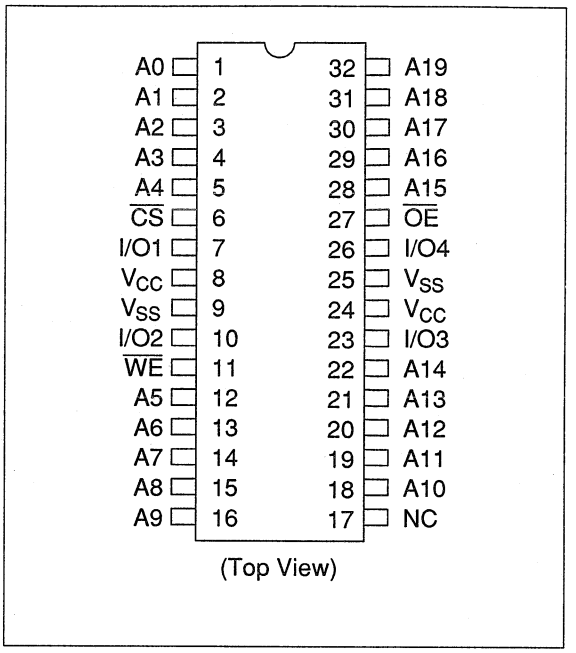
Features

- High speed:
  - Fast access time: 25/30/35/45 ns (max) (P-version)
    30/35/45 ns (max) (LP-version)
- Single 5 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- TTL compatible – All inputs and outputs
- Thin plastic package for high density mounting

Ordering Informations

Type No.	Access time	Package
HM624100JP-25	25 ns	400 mil 32-pin SOJ (CP-32DB)
HM624100JP-30	30 ns	
HM624100JP-35	35 ns	
HM624100JP-45	45 ns	
HM624100JLP-30	30 ns	
HM624100JLP-35	35 ns	
HM624100JLP-45	45 ns	
HM624100P-25	25 ns	400 mil 32-pin TSOP (II) (TTP-32DA)
HM624100P-30	30 ns	
HM624100P-35	35 ns	
HM624100P-45	45 ns	
HM624100LP-30	30 ns	
HM624100LP-35	35 ns	
HM624100LP-45	45 ns	

Pin Arrangement



(Top View)

Pin Description

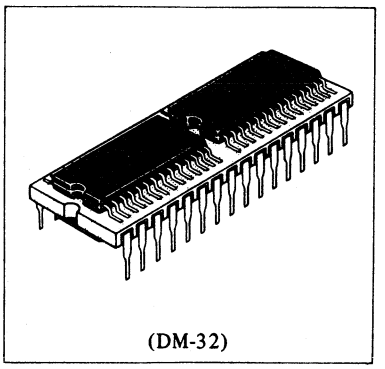
Pin name	Function
A0 – A19	Address input
I/O1 – I/O4	Data input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Static RAM Module

HM66203 Series

131072-word x 8-bit High Density CMOS Static RAM Module



(DM-32)

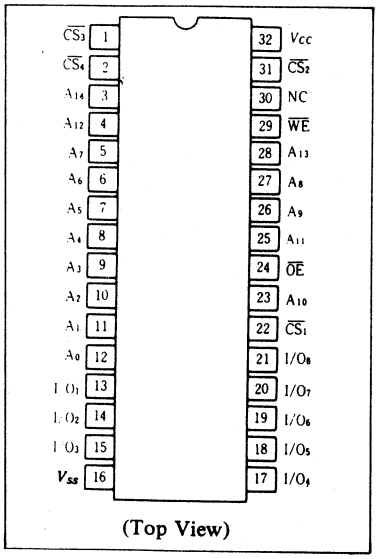
Features

- High Density Industry Standard 32 Pin DIP Mounting 4pcs of 256k Static RAM (SOP; HM62256FP/LFP).
- Single +5V Supply.
- High speed: Fast Access Time 100/120/150ns max.
- Equal Access and Cycle Time.
- Completely Static RAM: No Clock or Timing Strobe Required.
- Low Power
  - Standby: 40μW typ. (L-version)
  - Operation: 50mW typ. (f = 1MHz)
- Capability of Battery Back-up Operation (L-version).
- Common Data Input and Output, Three State Outputs.
- Directly TTL Compatible: All Inputs and Outputs.

Ordering Information

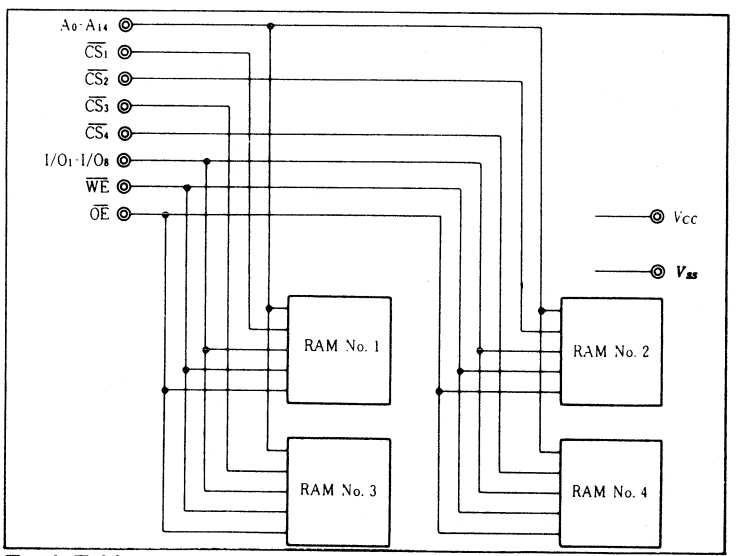
Type No.	Access Time	Package
HM66203-10	100ns	600 mil 32 pin DIP
HM66203-12	120ns	
HM66203-15	150ns	
HM66203L-10	100ns	
HM66203L-12	120ns	
HM66203L-15	150ns	

Pin Arrangement



(Top View)

Functional Block Diagram



Pin Description

Pin Name	Function
A0–A14	Address
I/O1–I/O8	Input/output
$\overline{CS1}$–$\overline{CS4}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Truth Table

Mode	$\overline{CSi}$	$\overline{WE}$	$\overline{OE}$	I/O	Current	Note
Not Selected (Power Down)	H*1	X	X	High-Z	I_{SB}, I_{SB1}	
Read	L*2	H	L	D_{out}	I_{CC}	Read Cycle (1) to (3)
Write	L*2	L	H	D_{in}	I_{CC}	Write Cycle (1)
	L*2	L	L	D_{in}	I_{CC}	Write Cycle (2)

Note) *1. X: Don't Care (H or L); i = 1, 2, 3, 4 All chips are not selected.
*2. $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$ and $\overline{CS4}$ pins are used for chip decoding.
Only one chip should be selected.
Two or more chips must not be selected at one time.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

Note) *1. −3.0V for pulse width ≦ 50ns

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	–	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 50ns

DC and Operating Characteristics (T_a = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	min.	typ. *1	max.	Unit	Notes
Input Leakage Current	$\|I_{LI}\|$	V_{IN} = V_{SS} to V_{CC}	–	–	8	μA	
		V_{IN} = V_{SS} to 3.5V	–	–	2	μA	
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS_n}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}	–	–	8	μA	*2
		$\overline{CS_n}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to 3.5V	–	–	2		
Operating Power Supply Current: DC	I_{CC}	$\overline{CSN}$ = V_{IL} $I_{I/O}$ = 0mA	–	10	25	mA	*3
Average Operating Power Supply Current (1)	I_{CC1}	MIN. cycle duty = 100% $I_{I/O}$ = 0mA	–	42	80	mA	HM66203/L −10
			–	37	80		HM66203/L −12
			–	35	80		HM66203/L −15
Average Operating Power Supply Current (2)	I_{CC2}	$\overline{CSN}$ = V_{IL} V_{IH} = V_{CC} V_{IL} = 0V $I_{I/O}$ = 0mA f = 1MHz	–	10	15	mA	*3
Standby Power Supply Current: DC	I_{SB}	$\overline{CSn}$ = V_{IH}	–	2	12	mA	*2
Standby Power Supply Current (1): DC	I_{SB1}	$\overline{CS_n}$ ≧ V_{CC} − 0.2V	–	8	400	μA	HM66203L Series
		0V ≦ V_{IN}	–	0.16	8	mA	HM66203 Series
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V	
Output High Voltage	V_{OH}	I_{OH} = −1.0mA	2.4	–	–	V	

Note) *1. Typical values are at V_{CC} = 5.0V, T_a = +25°C and specified loading.
*2. $\overline{CSn}$; All chips are not selected.
*3. $\overline{CSN}$ pins are used for chip decoding. Only one chip should be selected. Two or more chips must not be selected at one time.

Capacitance (T_a = 25°C, f = 1.0MHz)

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	–	–	45	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	–	50	pF

Note) This parameter is sampled and not 100% tested.

AC Characteristics (T_a = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

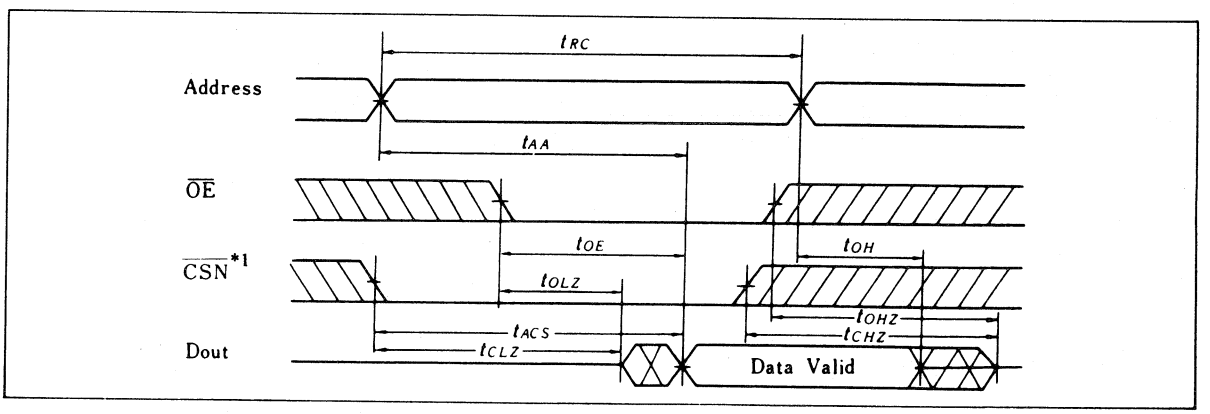
AC Test Conditions

- Input pulse levels . . . . . 0.8V to 2.4V
- Input rise and fall times 5ns
- Input and Output timing reference level 1.5V
- Output load . . . . . 1 TTL Gate and C_L (100pF) (Including scope & jig)

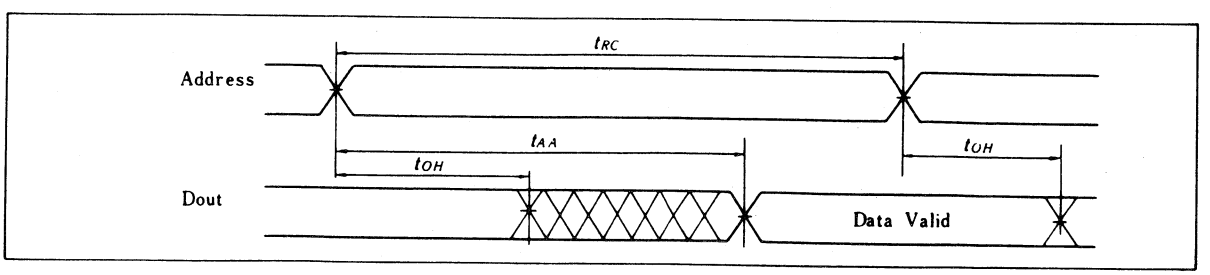
Read Cycle

Parameter	Symbol	HM66203-10		HM66203-12		HM66203-15		Unit
		min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	100	–	120	–	150	–	ns
Address Access Time	t_{AA}	–	100	–	120	–	150	ns
Chip Select Access Time	t_{ACS}	–	100	–	120	–	150	ns
Output Enable to Output Valid	t_{OE}	–	50	–	60	–	70	ns
Output Hold from Address Change	t_{OH}	10	–	10	–	10	–	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	–	10	–	10	–	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	35	0	40	0	50	ns
Output Disable to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns

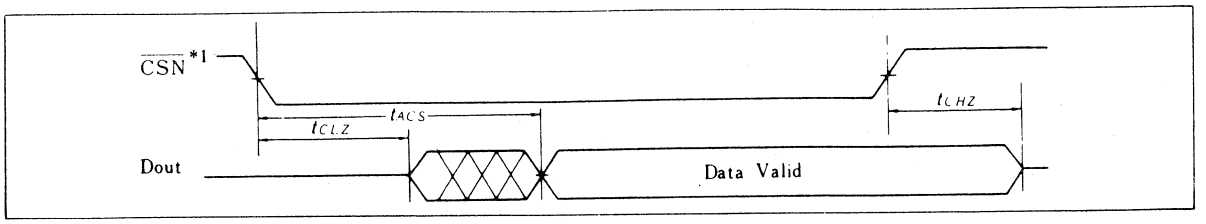
Timing Waveform of Read Cycle No. 1 *2



Timing Waveform of Read Cycle No. 2 *1,*2,*3,*5



Timing Waveform of Read Cycle No. 3 *2,*4,*5

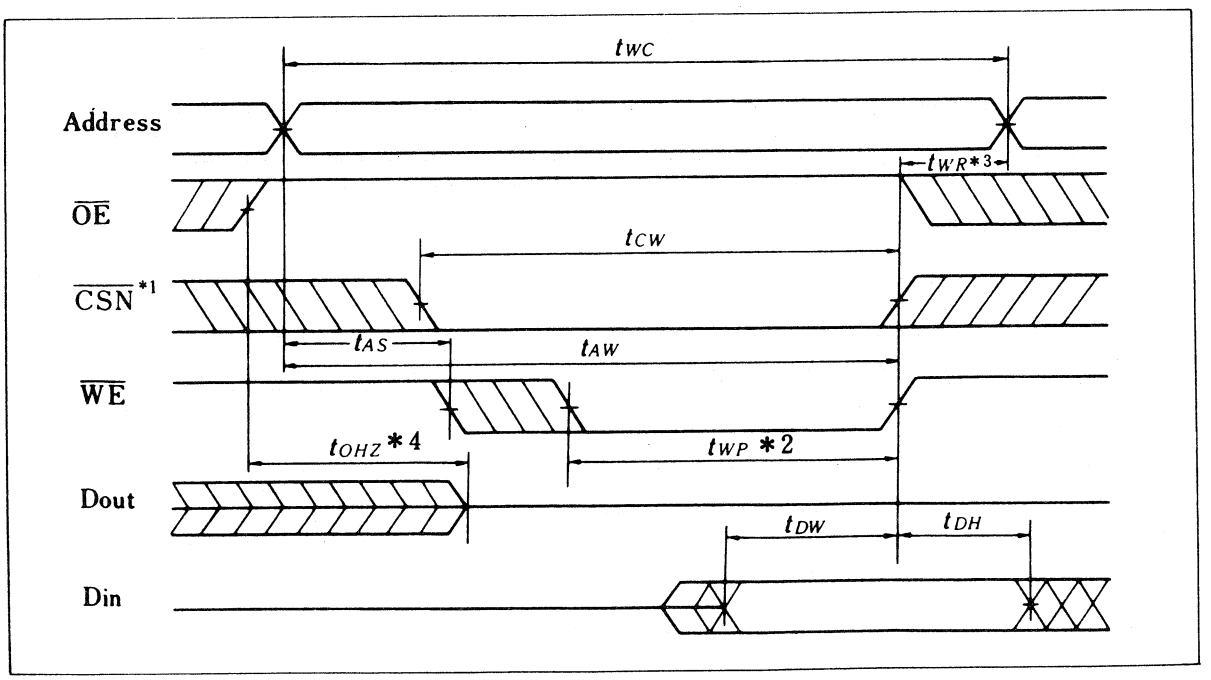


Note) *1. $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$ and $\overline{CS4}$ pins are used for chip decoding. Only one chip should be selected. Two or more chips must not be selected at one time.
*2. $\overline{WE}$ is high for read cycle.
*3. Device is continuously selected, $\overline{CSN} = V_{IL}$.
*4. Address should be valid prior to or coincident with $\overline{CSN}$ transition low.
*5. $\overline{OE} = V_{IL}$

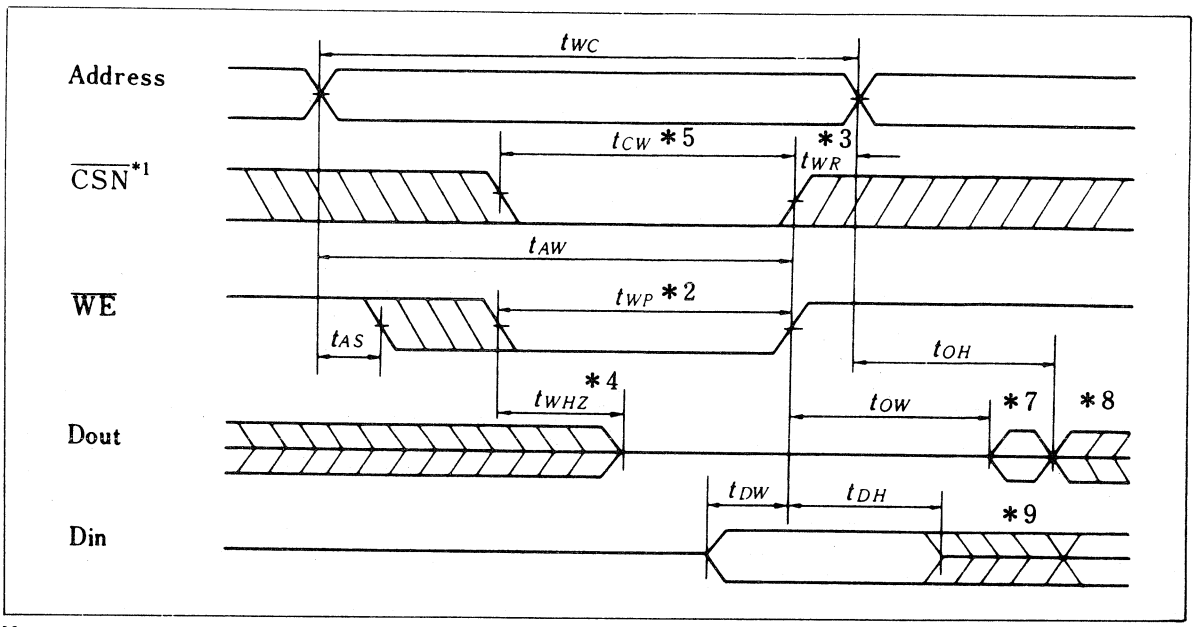
Write Cycle

Parameter	Symbol	HM66203-10		HM66203-12		HM66203-15		Unit
		min.	max.	min.	max.	min.	max.	
Write Cycle Time	t_{WC}	100	–	120	–	150	–	ns
Chip Selection to End of Write	t_{CW}	90	–	100	–	120	–	ns
Address Valid to End of Write	t_{AW}	90	–	100	–	120	–	ns
Address Set Up Time	t_{AS}	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	75	–	90	–	110	–	ns
Write Recovery Time	t_{WR}	10	–	0	–	0	–	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	–	50	–	60	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	ns

Timing Waveform of Write Cycle (1) ($\overline{OE}$ Clock)



Timing Waveform of Write Cycle (2) ($\overline{OE}$ Low Fixed)*6



Notes)
*1. $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$ and $\overline{CS4}$ pins are used for chip decoding. Only one chip should be selected. Two or more chips must not be selected at one time.
*2. A write occurs during the overlap (t_{WP}) of a low $\overline{CSN}$ and a low $\overline{WE}$.
*3. t_{WR} is measured from the earlier of $\overline{CSN}$ or $\overline{WE}$ going high to the end or write cycle.
*4. During this period, I/O pins are in the output state. The input signals out of phase must not be applied.
*5. If the $\overline{CSN}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, output remain in a high impedance state.
*6. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
*7. Dout should be held in phase of the written data during this write cycle.
*8. Dout is the read data of next address.
*9. If $\overline{CSN}$ is low during this period, I/O pins are in the output state. The input signals which are opposite to the output level should not be applied to I/O pins.

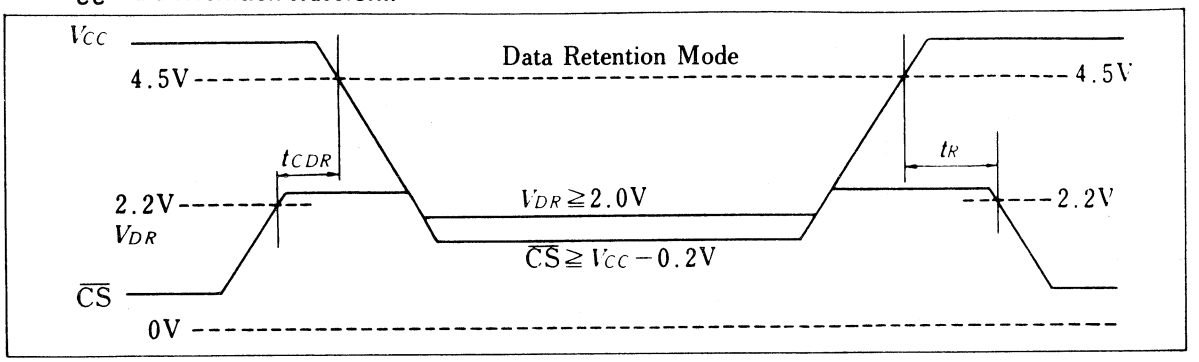
Low V_{CC} Data Retention Characteristics (T_a = 0°C to +70°C)

(Data retention characteristics is guaranteed only for HM66203L Series.)

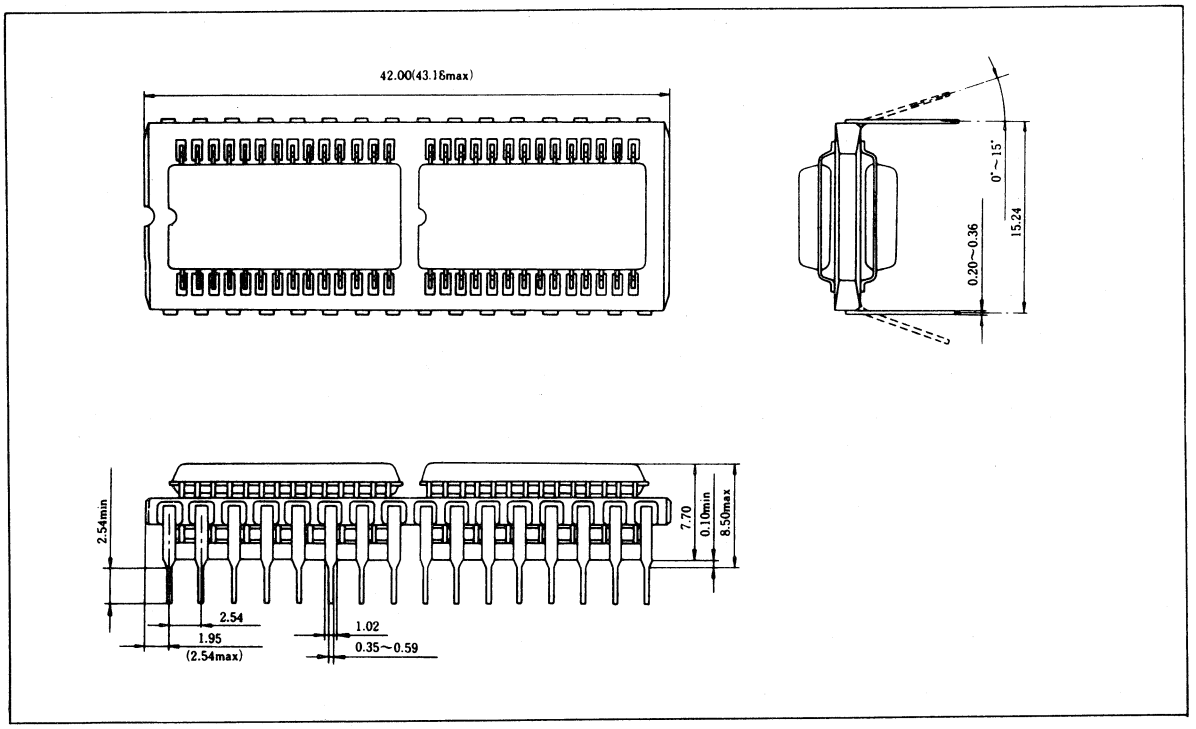
Parameter	Symbol	min.	typ.	max.	Unit	Test Conditions
V_{CC} for Data Retention	V_{DR}	2.0	–	–	V	$\overline{CSn} \geqq V_{CC} - 0.2V$
Data Retention Current	I_{CCDR}	–	–	200	μA	V_{CC} = 3.0V $\overline{CSn} \geqq 2.8V$*2, $0V \leqq V_{IN}$
Chip Deselect to Data Retention Time	t_{CDR}	0	–	–	ns	See Retention Waveform
Operation Recovery Time	t_R	[1] t_{RC}*1	–	–	ns	

Note) *1. t_{RC} = Read Cycle Time.
*2. $\overline{CSn}$: All chips are not selected.

Low V_{CC} Data Retention Waveform



Package Dimension (Unit: mm)



HM66204 Series

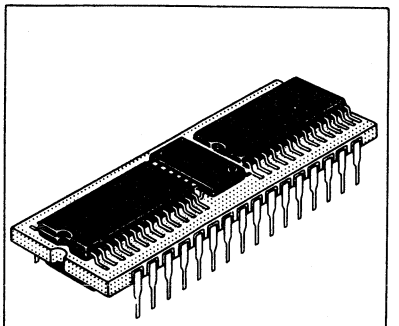
131072-word x 8-bit High Density CMOS Static RAM Module

The HM66204 is a high density 1 M-bit static RAM module consisted of 4 pieces of HM62256FP/LFP products (SOP type 256k static RAM) and a HD74HC138FP equivalent product (SOP type CMOS decoder logic).

An outline of the HM66204 is the standard 600 mil width 32 pin dual-in-line package. Its pin arrangement is completely compatible with 1 M-bit monolithic static RAM.

The HM66204 offers the features of low power and high speed by using high speed CMOS devices. And, the HM66204 makes high density mounting possible with no surface mount technology.

These features make the HM66204 ideally suited for high density compacted memory systems.

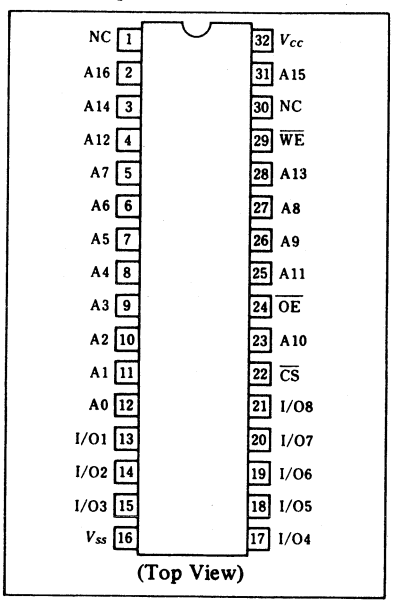


(DM-32A)

Features

- High density 32 pin DIP
  - Mounting 4 pcs. of 256k static RAM (SOP; HM62256FP/LFP) and CMOS decoder logic (SOP; HD74HC138FP equivalent)
- Pin compatible with 1M monolithic static RAM
- High speed
  - Fast access time 120 ns/150 ns (maximum)
- Equal access and cycle time
- Completely static RAM
  - No clock or timing strobe required
- Low power standby and low power operation
  - Standby 40 μW (typical) (L-version)
  - Operation 50 mW (typical) (f = 1 MHz)
- Common data input and output, three state outputs
- Capable of battery backup operation (L-version)

Pin Arrangement



(Top View)

Ordering Information

Part No.	Access Time	Package
HM66204-12	120 ns	600-mil 32-pin DIP
HM66204-15	150 ns	
HM66204L-12	120 ns	
HM66204L-15	150 ns	

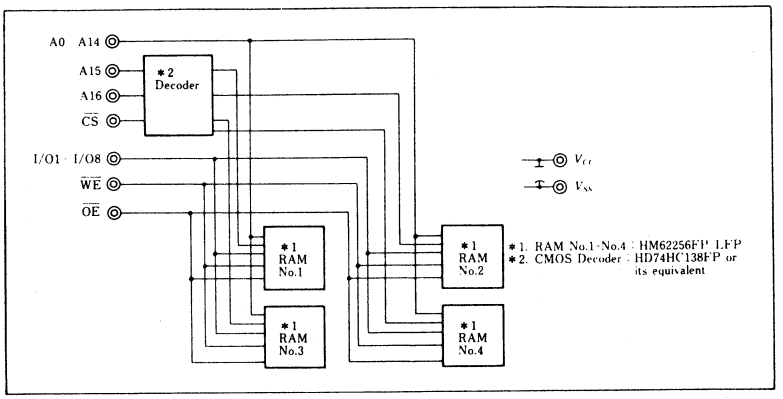
Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C
Power dissipation	P_T	1.0	W

Pin Description

Pin Name	Function
A0 - A16	Address
I/O1 - I/O8	Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

Block Diagram



Mode Selection

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	Current	Note
Not selected (Power down)	H	×	×	High-Z	I_{SB}, I_{SB1}	
Read	L	H	L	Dout	I_{CC}	Read cycle (1) – (3)
Write	L	L	H	Din	I_{CC}	Write cycle (1)
	L	L	L	Din	I_{CC}	Write cycle (2)

Note) × = Don't care (H or L)

Electrical Characteristics

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input high (logic 1) Voltage	V_{IH}	3.85*1	–	6.0	V	A15, A16, $\overline{CS}$
		2.2	–	6.0	V	Others except A15, A16, $\overline{CS}$
Input low (logic 0) Voltage	V_{IL}	–0.5	–	0.8	V	

Note) *1. V_{IH} min is determined by V_{CC} × 0.7.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test Conditions	Notes
Input leakage current	$\|I_{LI}\|$	–	–	8	μA	V_{in} = V_{SS} to V_{CC}	
		–	–	2	μA	V_{in} = V_{SS} to 3.5V	
Output leakage current	$\|I_{LO}\|$	–	–	8	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}	
		–	–	2	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to 3.5V	
Operating power supply current: DC	I_{CC}	–	10	25	mA	$\overline{CS}$ = V_{IL} $I_{I/O}$ = 0mA	
Average operating power supply current (1)	I_{CC1}	–	37	80	mA	MIN. cycle duty = 100%	–12
		–	35	80		$I_{I/O}$ = 0mA	–15
Average operating power supply current (2)	I_{CC2}	–	10	15	mA	$\overline{CS}$ = V_{IL}, V_{IH} = V_{CC} V_{IL} = 0V, $I_{I/O}$ = 0mA f = 1MHz	
Standby power supply current: DC	I_{SB}	–	2	12	mA	$\overline{CS}$ = V_{IH}	
Standby power supply current (1): DC	I_{SB1}	–	8	400	μA	$\overline{CS}$ ≥ V_{CC}–0.2V A15•A16 ≥ V_{CC} – 0.2V or 0V ≦ A15•A16 ≦ 0.2V	HM66204L Series
		–	0.16	8	mA		
Output low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 2.1 mA	
Output high voltage	V_{OH}	2.4	–	–	V	I_{OH} = –1.0 mA	

Note) *1. Typical values are at V_{CC} = 5.0V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	–	–	45	pF	Vin = 0V
Input/output capacitance	$C_{I/O}$	–	–	50	pF	$V_{I/O}$ = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

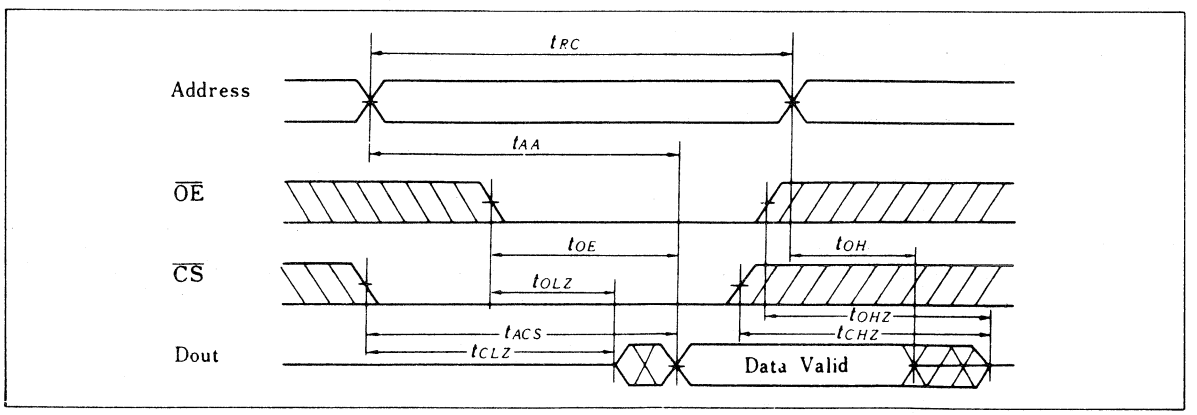
AC Test Conditions

- Input pulse levels:
  0.8V to 4.0V . . . $\overline{CS}$, A15, A16
  0.8V to 2.4V . . . Other pin except $\overline{CS}$, A15, A16
- Input rise and fall times: 5 ns
- Input and output timing reference level: 1.5V
- Output load: 1 TTL Gate and C_L (100pF) (Including scope & jig)

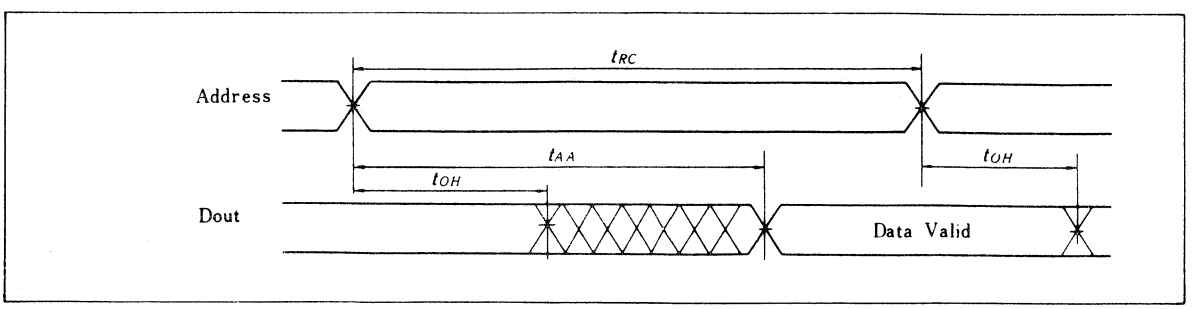
Read Cycle

Parameter	Symbol	HM66204-12		HM66204-15		Unit
		min	max	min	max	
Read cycle time	t_{RC}	120	–	150	–	ns
Address access time	t_{AA}	–	120	–	150	ns
Chip select access time	t_{ACS}	–	120	–	150	ns
Output enable to output valid	t_{OE}	–	60	–	70	ns
Output hold from address change	t_{OH}	10	–	10	–	ns
Chip selection to output in low Z	t_{CLZ}	10	–	10	–	ns
Output enable to output in low Z	t_{OLZ}	5	–	5	–	ns
Chip deselection to output in high Z	t_{CHZ}	0	40	0	50	ns
Output disable to output in high Z	t_{OHZ}	0	40	0	50	ns

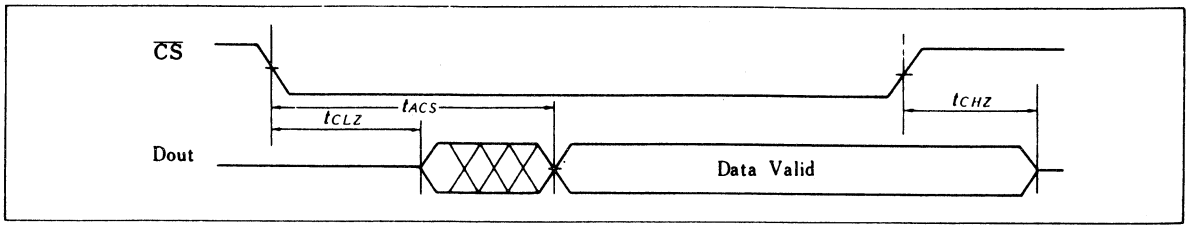
Read Cycle Timing No. 1 *1



Read Cycle Timing No. 2 *1, *2, *4



Read Cycle Timing No. 3 *1, *3, *4

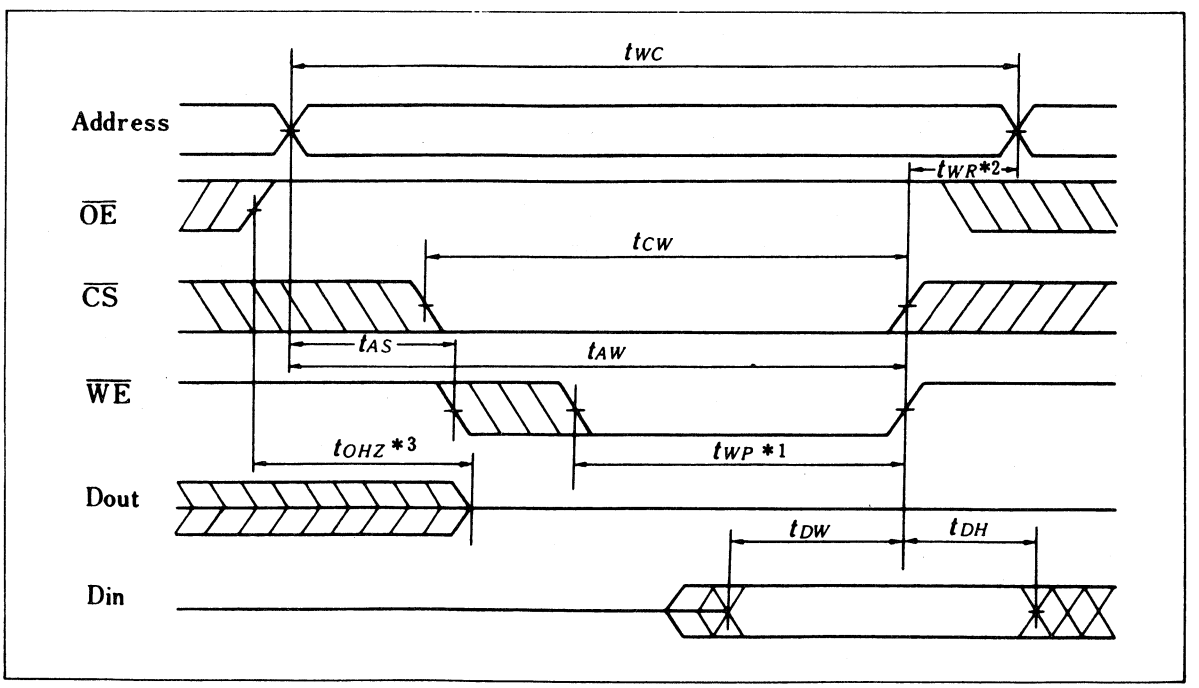


Notes) *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address should be valid prior to or coincident with $\overline{CS}$ transition low.
*4. $\overline{OE}$ = V_{IL}.

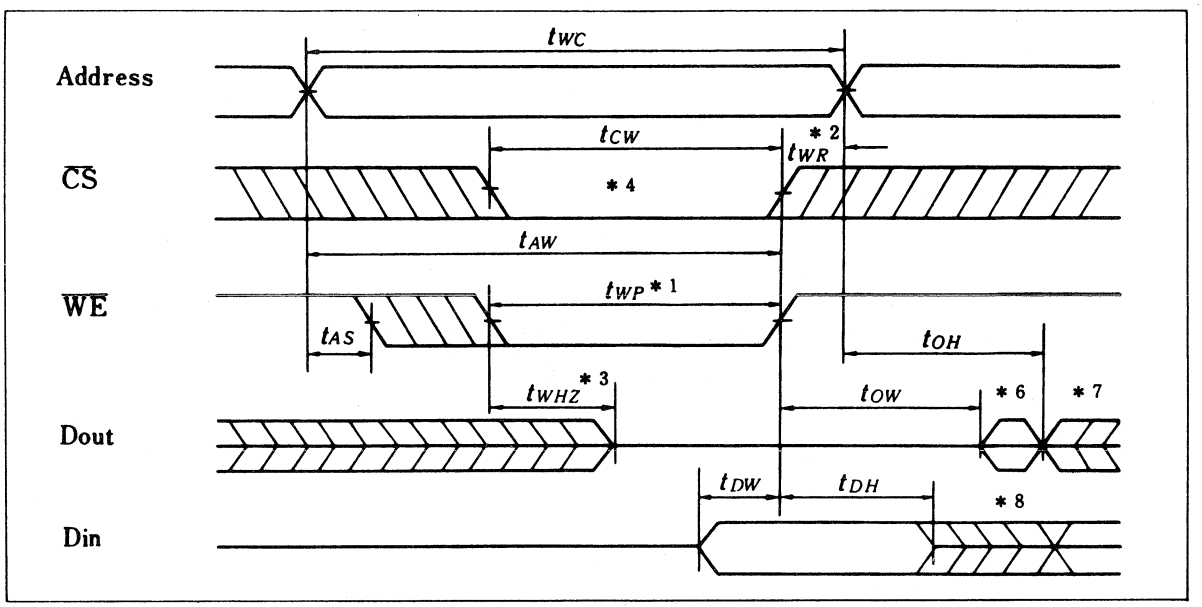
Write Cycle

Parameter	Symbol	HM66204-12		HM66204-15		Unit
		min	max	min	max	
Write cycle time	t_{WC}	120	–	150	–	ns
Chip selection to end of write	t_{CW}	100	–	120	–	ns
Address valid to end of write	t_{AW}	100	–	120	–	ns
Address setup time	t_{AS}	0	–	0	–	ns
Write pulse width	t_{WP}	90	–	110	–	ns
Write recovery time	t_{WR}	5	–	5	–	ns
Write to output in high Z	t_{WHZ}	0	40	0	50	ns
Data to write time overlap	t_{DW}	50	–	60	–	ns
Data hold from write time	t_{DH}	0	–	0	–	ns
Output disable to output in high Z	t_{OHZ}	0	40	0	50	ns
Output active from end of write	t_{OW}	5	–	5	–	ns

Write Cycle Timing No. 1 ($\overline{OE}$ Clock)



Write Cycle Timing No. 2*5 ($\overline{OE}$ Low Fixed)



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state.
The input signals of opposite phase to the outputs must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
*5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
*6. D_{out} should be held in phase of the written data during this write cycle.
*7. D_{out} is the read data of next address.
*8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The input signals which are opposite to the output level should not be applied to I/O pins.

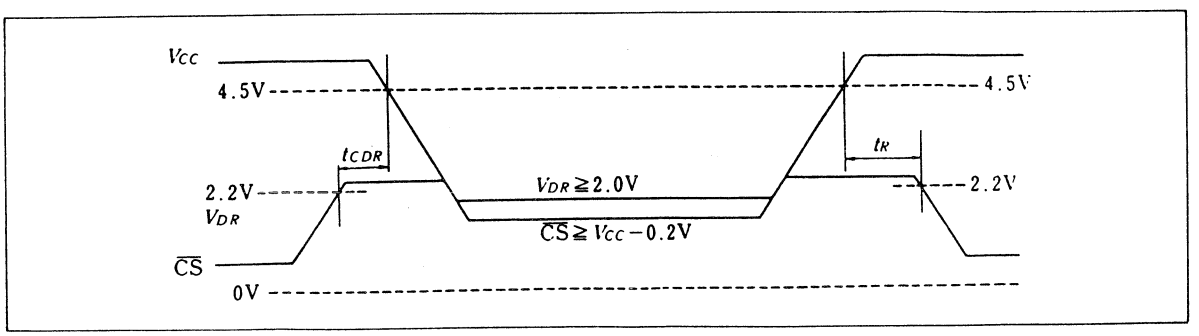
Low V_{CC} Data Retention Characteristics (Ta = 0°C to +70°C)

Data retention characteristics is guaranteed only for L version.

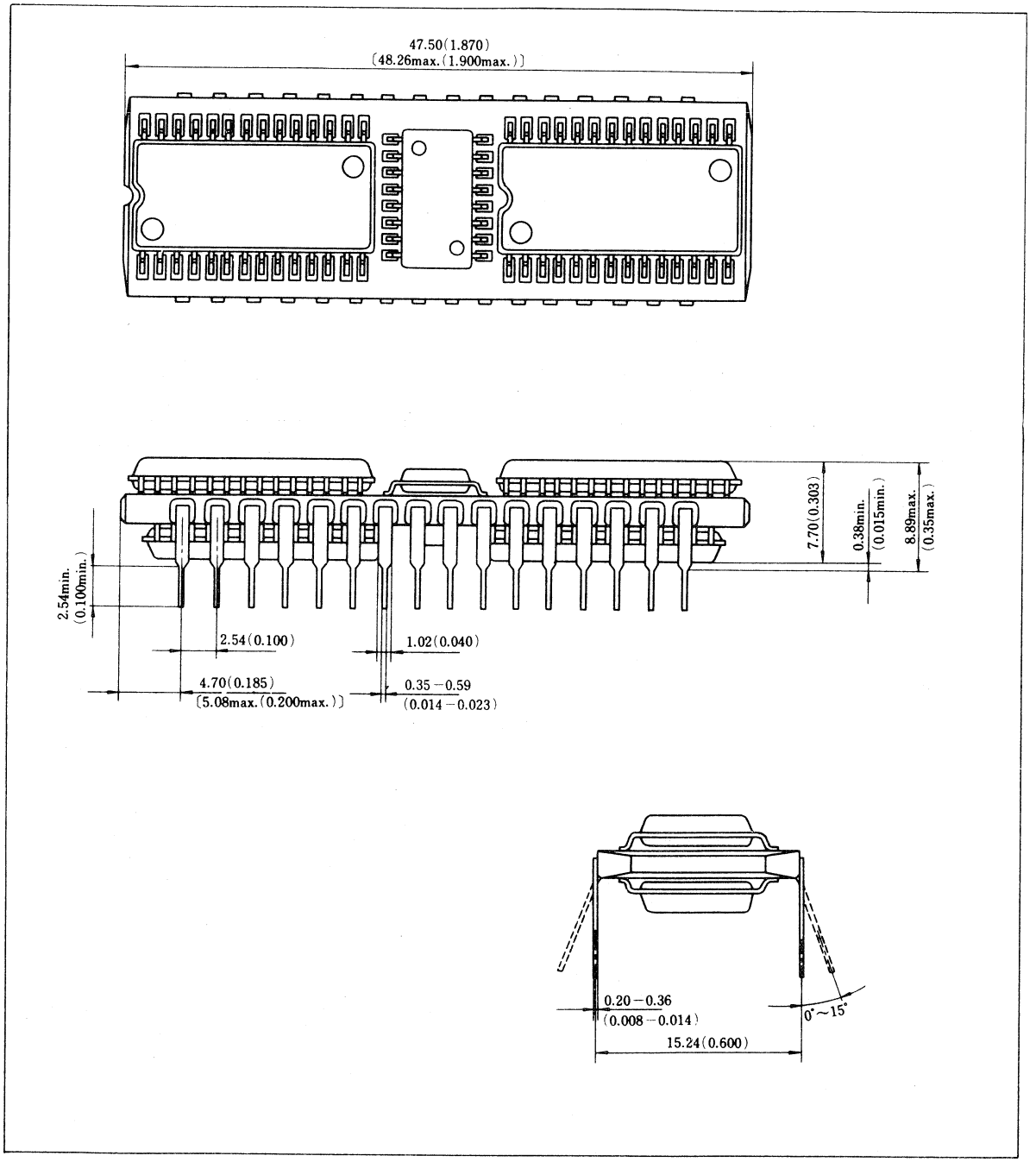
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for data retention	V_{DR}	2.0	–	–	V	$\overline{CS} \geq V_{CC}$ -0.2V A15, A16 $\geq V_{CC}$ -0.2V or A15, A16 $\leq$ 0.2V
Data retention current	I_{CCDR}	–	–	200	µA	V_{CC} = 3.0V, $\overline{CS} \geq$ 2.8V A15·A16 $\geq$ 2.8V or 0V $\leqq$ A15·A16 $\leqq$ 0.2V
Chip deselect to data retention time	t_{CDR}	0	–	–	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*1	–	–	ns	

Note) *1. t_{RC} = Read Cycle Time.

Low V_{CC} Data Retention Waveform



Package Dimension; Unit: mm (inch)



HM66205L Series

524,288-word × 8-bit High Density CMOS Static RAM Module

The HM66205L is a high density 4-Mbit static RAM module which consists of 4 pieces HM628128LT products (TSOP type 1M static RAM) and a HD74ACT138FP equivalent product (SOP type CMOS decoder logic).
An outline of the HM66205L is the standard 600-mil width 32-pin dual-in-line package. Its pin arrangement is completely compatible with 4-Mbit monolithic static RAM.
The HM66205L offers the features of low power and high speed by using high speed CMOS devices. And, the HM66205L makes high density mounting possible without surface mount technology.
These features make the HM66205L ideally suited for high density compacted memory systems.

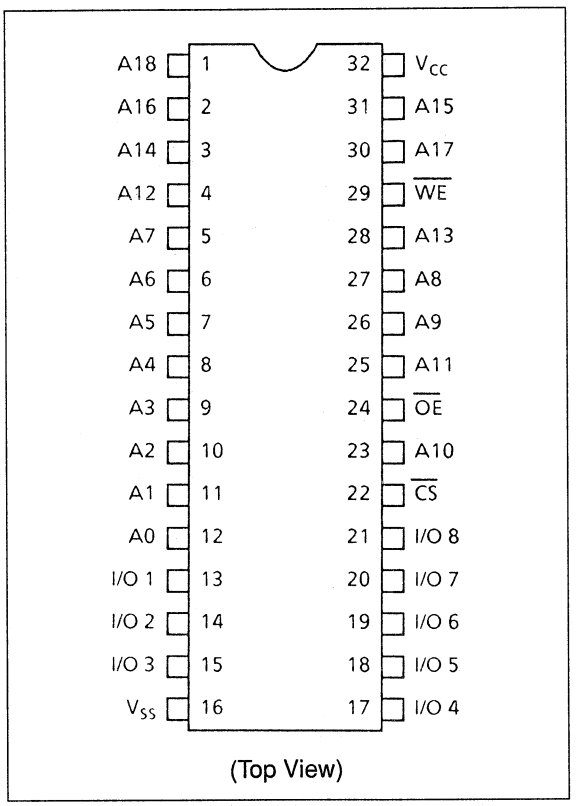
Features

- High density 32-pin DIP
  - Mounting 4 pcs. of 1M static RAM (TSOP; HM628128LT) and CMOS decoder logic (SOP; HD74ACT138FP equivalent)
- Pin compatible with 4M monolithic static RAM
- High speed
  - Fast access time: 85 ns/100 ns/120 ns (max)
- Equal access and cycle time
- Completely static RAM
  - No clock or timing strobe required
- Low power standby and low power operation
  - Standby: 40 µW (typical)
  - Operation: 80 mW (typical)
- Comon data input and output, three state outputs
- Capable of battery backup operation
- Directry TTL compatible: All inputs and outputs

Ordering Information

Type No.	Access time	Package
HM66205L-85	85 ns	600-mil 32-pin DIP
HM66205L-10	100 ns	
HM66205L-12	120 ns	

Pin Arrangement

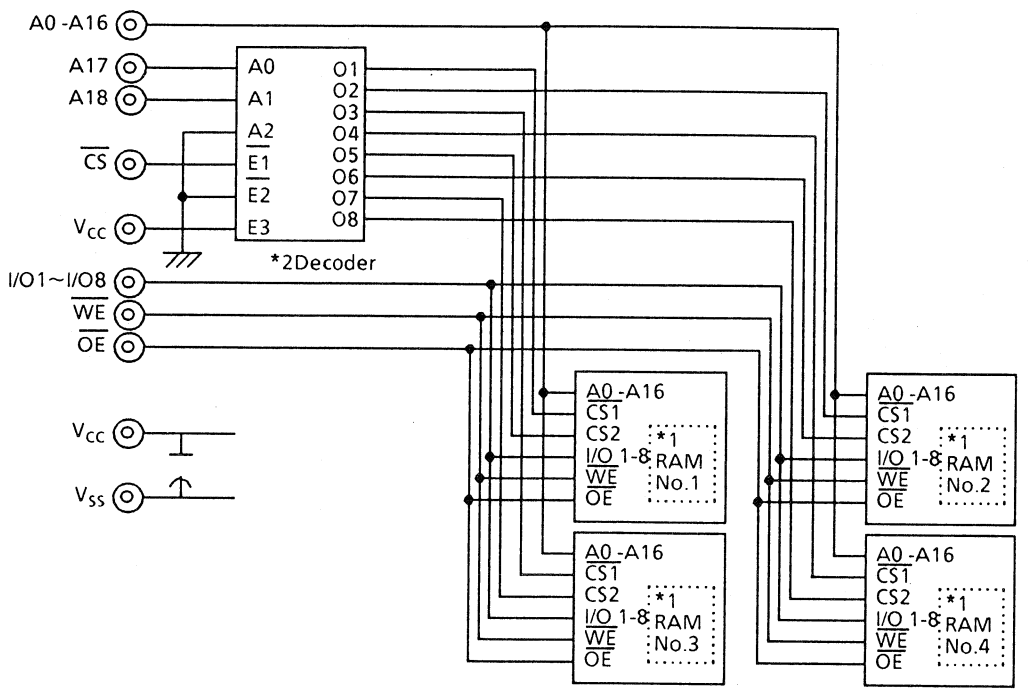


(Top View)

Pin Description

Pin name	Function
A0 – A18	Address
I/O1 – I/O8	Input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Notes: *1. RAM No.1 – No.4: HM628128LT
*2. CMOS Decoder: HD74ACT138FP

Truth Table

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	Current	Ref. cycle
Not selected (Power down)	H	X	X	High-Z	I_{SB}, I_{SB1}	
Read	L	H	L	Dout	I_{CC}	Read cycle (1) – (3)
Write	L	L	H	Din	I_{CC}	Write cycle (1)
	L	L	L	Din	I_{CC}	Write cycle (2)

Note: X = Don't care (H or L)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–10 to +85	°C

Recommended DC Operating Conditions (Ta = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	–0.3[*1]	—	0.8	V

Note: 1. –3.0 V for pulse half-width ≤ 30 ns.

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions
Input leakage currentent	$\|I_{LI}\|$	—	—	8	µA	Vin = V_{SS} to V_{CC}
Output leakage currentent	$\|I_{LO}\|$	—	—	8	µA	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH} or $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current: DC	I_{CC}	—	19	46	mA	$\overline{CS}$ = V_{IL}, others V_{IH}/V_{IL} $I_{I/O}$ = 0 mA
Average operating power supply current (1)	I_{CC1}	—	48	89	mA	Min cycle, duty = 100% $\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, others V_{IH}/V_{IL}
Average operating power supply current (2)	I_{CC2}	—	16	36	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS}$ ≤ 0.2 V, V_{IH} = V_{CC} –0.2 V, V_{IL} ≤ 0.2 V
Standby power supply current: DC	I_{SB}	—	4	12	mA	$\overline{CS}$ = V_{IH}
Standby power supply current (1)	I_{SB1}	—	8	400	µA	Vin ≥ 0 V $\overline{CS}$ = V_{CC} –0.2
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –1.0 mA

Note: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit	Test conditions	Notes
Input capacitance (1)	Cin1	—	45	pF	Vin = 0 V	A0 – A16, $\overline{WE}$, $\overline{OE}$
Input capacitance (2)	Cin2	—	45	pF	Vin = 0 V	A17 – A18, $\overline{CS}$
Input/output capacitance	$C_{I/O}$	—	50	pF	$V_{I/O}$ = 0 V	I/O1 – I/O8

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

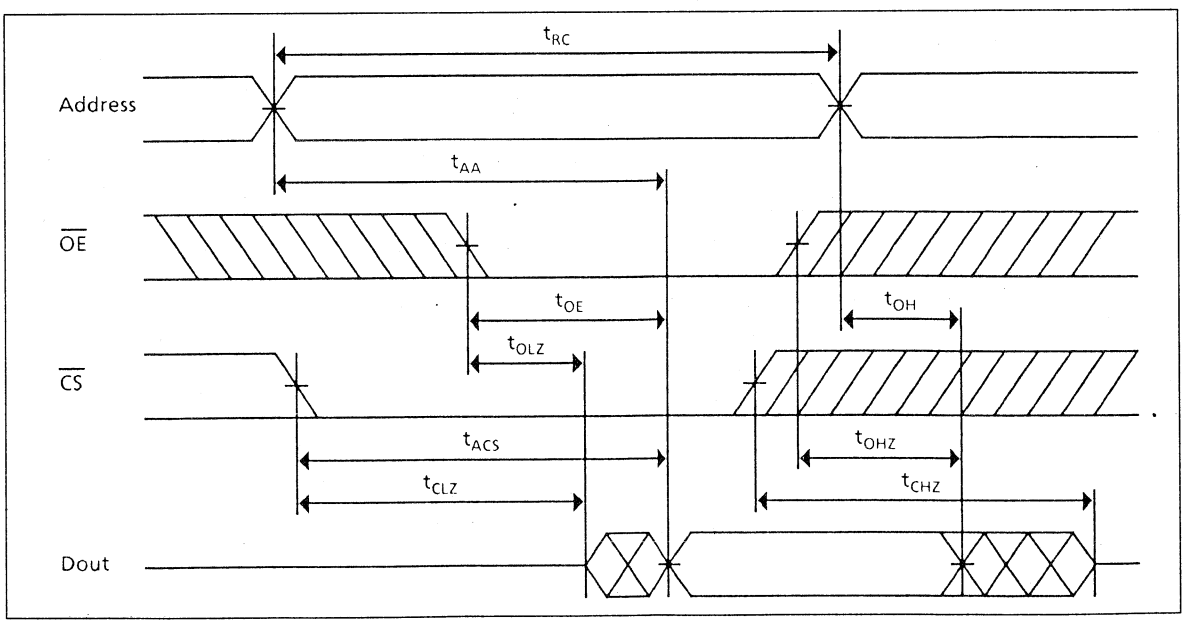
Test Condition

- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall times: 5 ns
- Input and output timing reference level: 1.5 V
- Output load: 1 TTL Gate and CL = 100 pF (Including scope and jig)

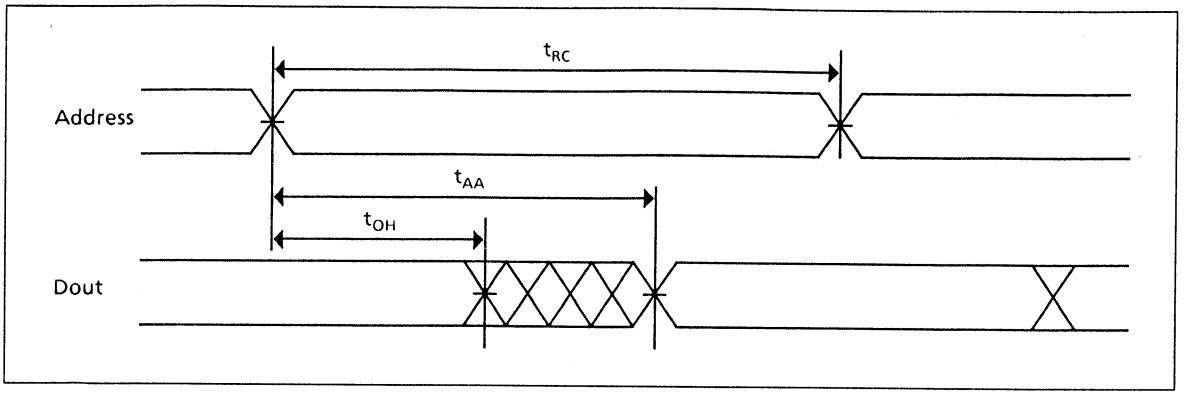
Read Cycle

		HM66205L-85		HM66205L-10		HM66205L-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	85	—	100	—	120	—	ns
Address access time	t_{AA}	—	85	—	100	—	120	ns
Chip select access time	t_{ACS}	—	85	—	100	—	120	ns
Output enable to output valid	t_{OE}	—	45	—	50	—	60	ns
Chip selection to output in low-Z	t_{CLZ}	10	—	10	—	10	—	ns
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	5	—	ns
Chip deselection to output in high-Z	t_{CHZ}	0	30	0	35	0	45	ns
Output disable to output in high-Z	t_{OHZ}	0	30	0	35	0	45	ns
Output hold from address change	t_{OH}	10	—	10	—	10	—	ns

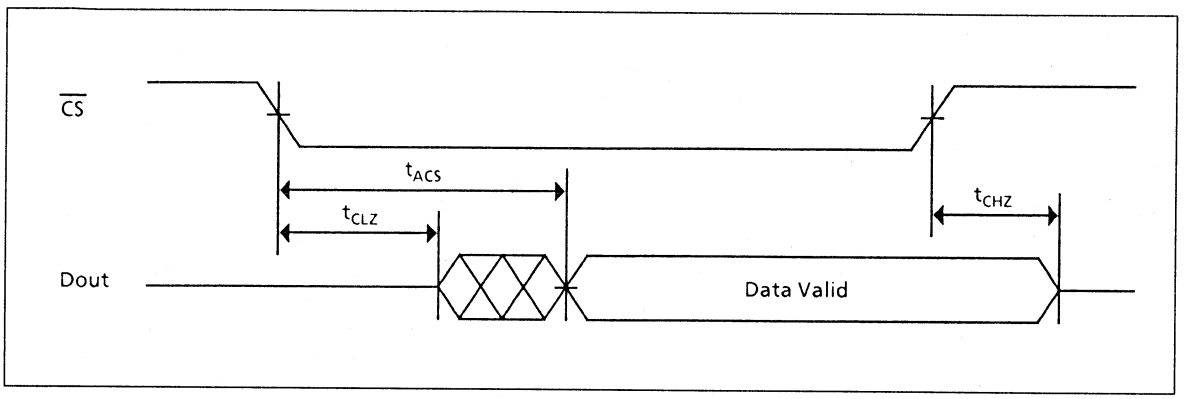
Read Timing Waveform (1) *1



Read Timing Waveform (2) *1, *2, *4



Read Timing Waveform (3) *1, *3, *4

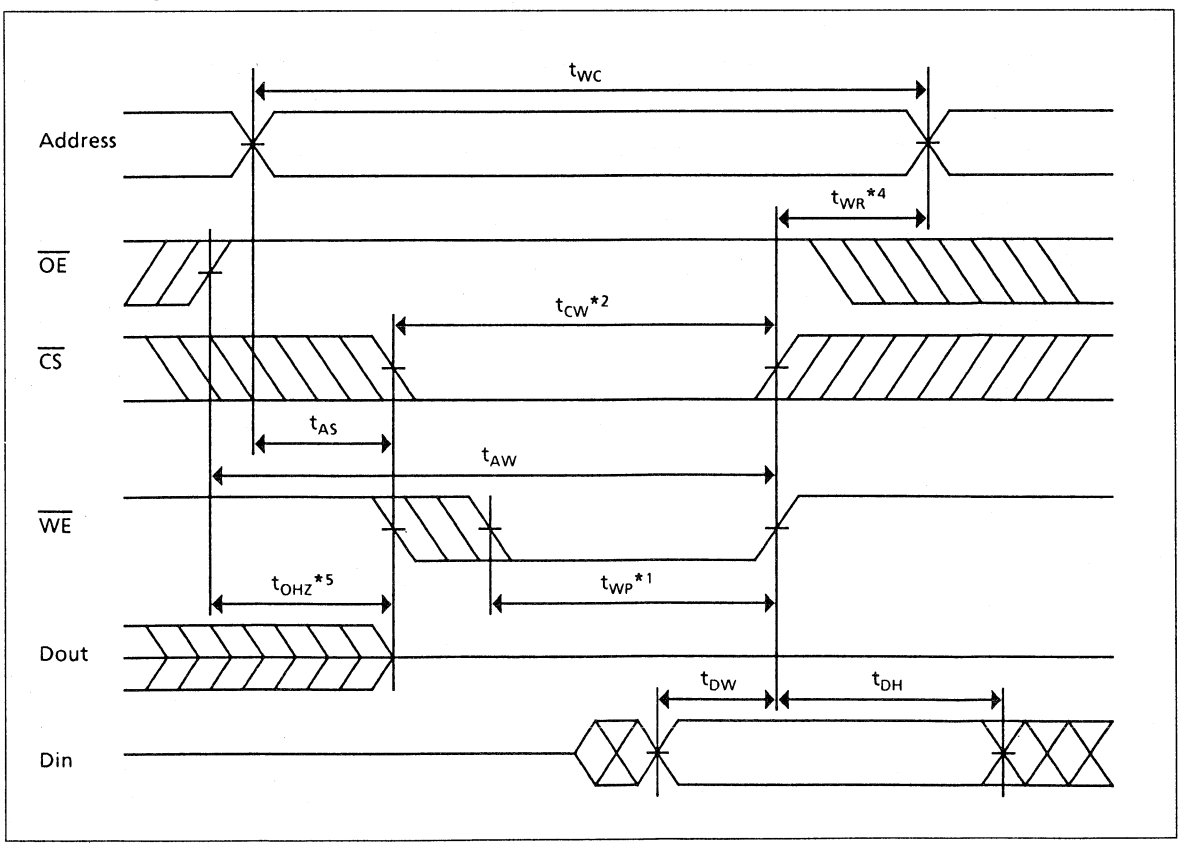


Notes: 1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address should be valid prior to or coinsident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$

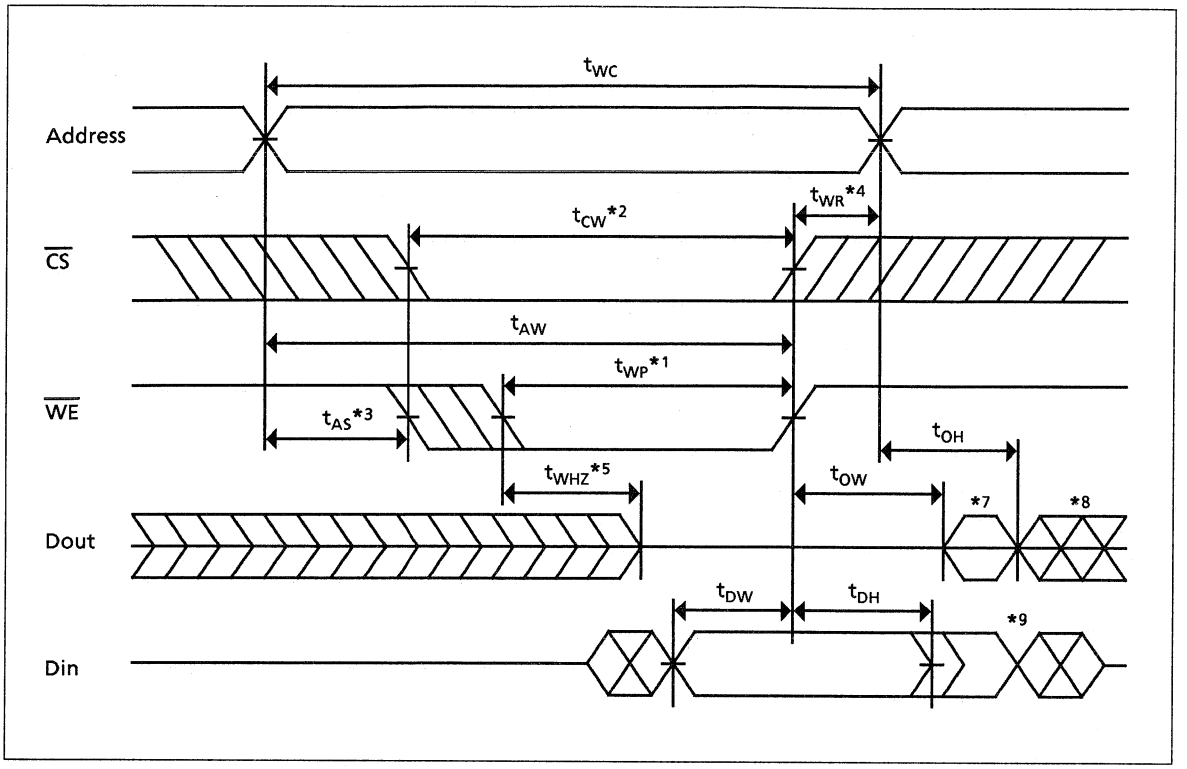
Write Cycle

		HM66205L-85		HM66205L-10		HM66205L-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time	t_{WC}	85	—	100	—	120	—	ns
Chip selection to end of write	t_{CW}	75	—	90	—	100	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Address valid to end of write	t_{AW}	75	—	90	—	100	—	ns
Write pulse width	t_{WP}	65	—	75	—	85	—	ns
Write recovery	t_{WR}	5	—	5	—	10	—	ns
Write to output in high-Z	t_{WHZ}	0	30	0	35	0	40	ns
Data to write time overlap	t_{DW}	35	—	40	—	45	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	5	—	5	—	5	—	ns

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Write Timing Waveform (2) *5 ($\overline{OE}$ Low Fixed)

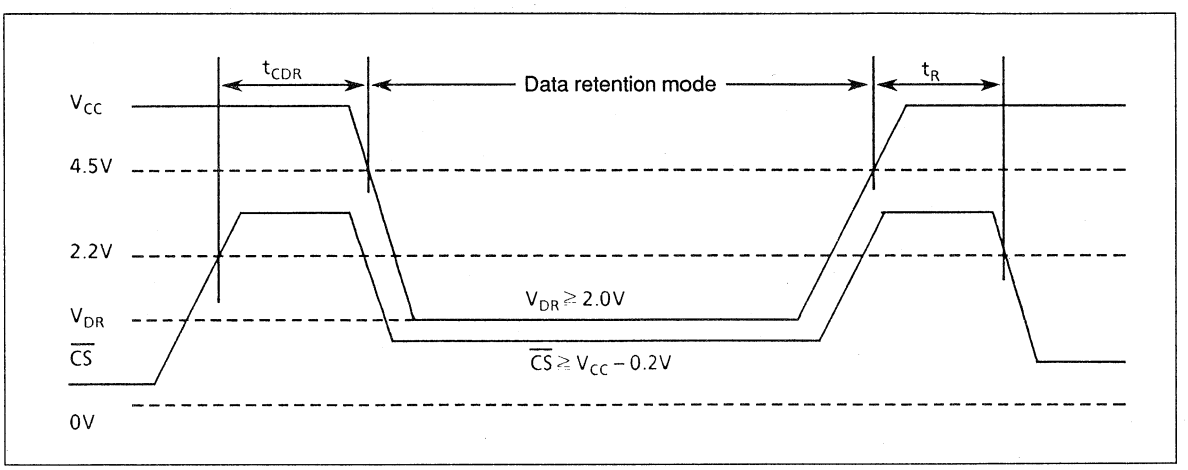


Notes:
1. A write occures during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state.
   The input signals out of phase must not be applied.
4. If the $\overline{CS}$ low transition occures simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$).
6. Dout should be held in the phase of the written data during this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state.
   The input signals which are opposite to the output level should not be applied to I/O pins.

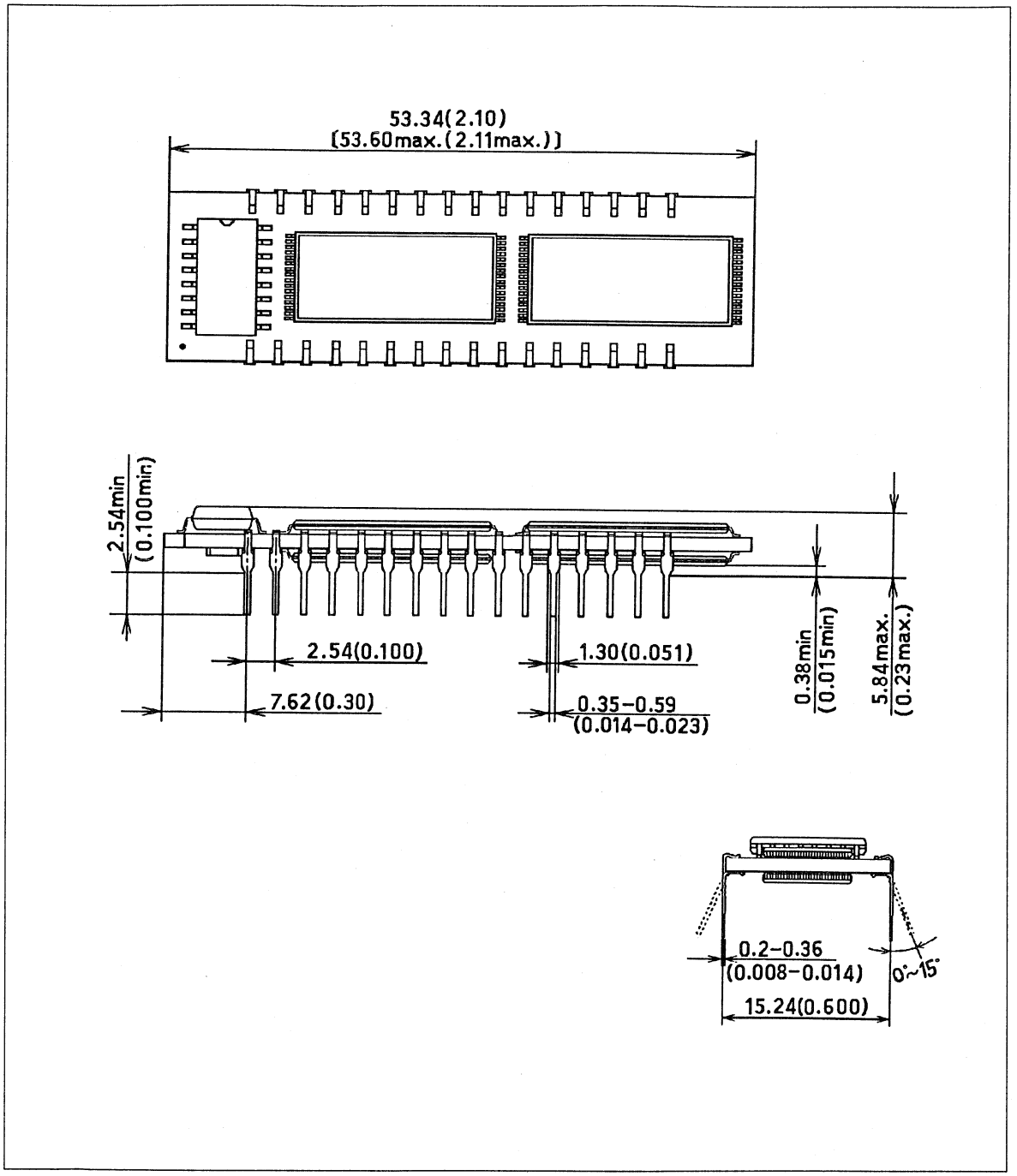
Low V_{CC} Data Retention Characteristics (Ta = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, A17•A18 $\geq V_{CC} - 0.2$ V, Vin $\geq$ 0 V
Data retention current	I_{CCDR}	—	4	200	µA	V_{CC} = 3.0 V, $\overline{CS} \geq V_{CC} - 0.2$ V, Vin $\geq$ 0 V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	5	—	—	ms	

Low V_{CC} Data Retention Waveform



Package Dimension



HB66B1616A Series

16,384-word × 16-bit High Speed Static RAM Module

The HB66B1616A is a high speed 16K × 16 Static RAM module, mounted 4 pieces of 64 Kbit SRAM (HM6289JP) sealed in SOJ package. An outline of the HB66B1616A is 36-pin dual in-line package. Therefore, the HB66B1616A makes high density mounting possible without surface mount technology. The HB66B1616A provides common data inputs and outputs. Its module board has decoupling capacitors to reduce noise.

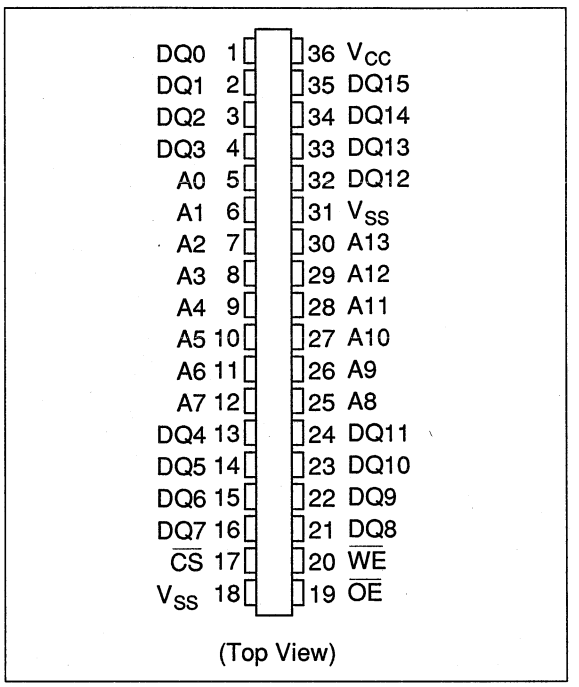
Features

- Single 5 V (± 5%) supply
- High speed
  - Access time: 25 ns/35 ns (max)
- Low power dissipation
  - Active mode: 1200 mW typ
  - Standby mode: 300 mW typ (TTL level)
    0.4 mW typ (CMOS level)
- Equal access and cycle time
- Completely static RAM
  - No clock or timing strobe required
- Directry TTL compatible: All inputs and outputs

Ordering Information

Part No.	Access time	Package
HB66B1616A-25	25 ns	36-pin dual in-line leaded type
HB66B1616A-35	35 ns	

Pin Arrangement

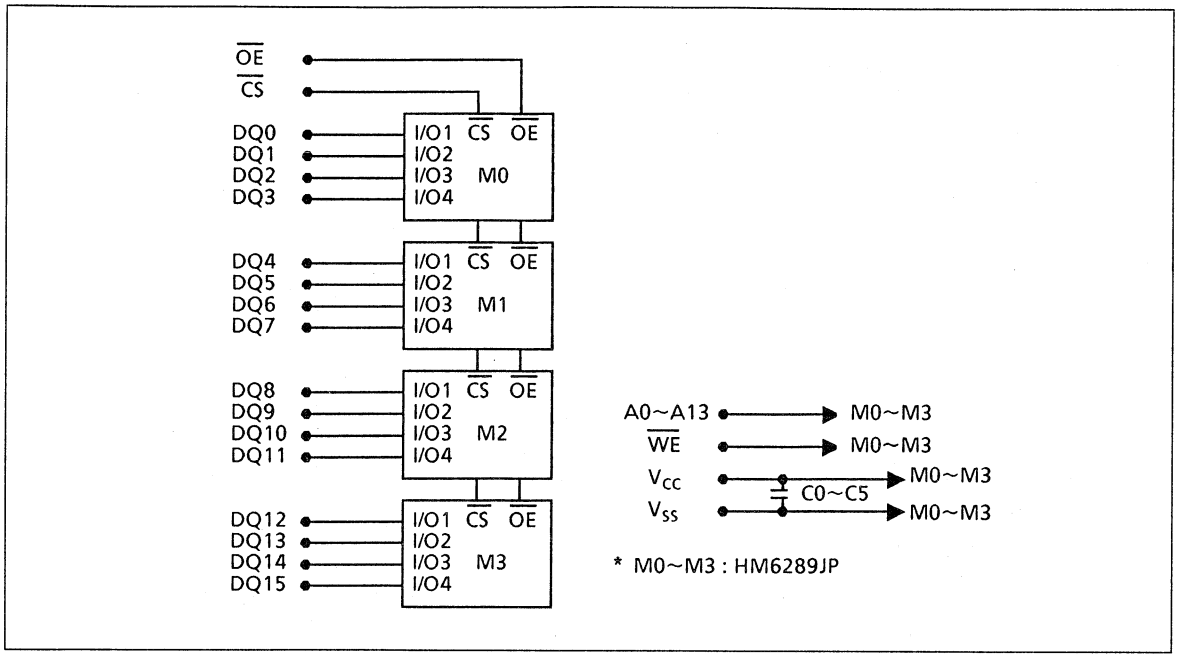


(Top View)

Pin Description

Pin name	Function
A0 – A13	Address input
DQ0 – DQ15	Data-in, Data-out
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply (+5 V)
V_{SS}	Ground

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	Vin	–0.5*1 to +7.0	V
Power dissipation	P_T	4.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–10 to +85	°C

Note: 1. Vin min = –2.0 V for pulse width ≤ 10 ns.

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
H	X	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	I_{CC}	Dout	Read cycle (1) – (3)
L	H	L	Write	I_{CC}	Din	Write cycle (1) – (2)
L	L	L	Write	I_{CC}	Din	Write cycle (3) – (6)

Note: X means don't care.

Recommended DC Operating Conditions (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.0	5.25	V
	V_{SS}	0.0	0.0	0.0	V
Input high (ligic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: 1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test condition	Note
Input leakage current	I_{IL}	–10	—	10	µA	V_{CC} = max Vin = V_{SS} to V_{CC}	
Output leakage current	I_{LO}	–2	—	2	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}	
Operating power supply current	I_{CC}	—	240	480	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA min. cycle	
Standby power supply current	I_{SB}	—	60	120	mA	$\overline{CS}$ = V_{IH} min. cycle	
Standby power supply current (1)	I_{SB1}	—	0.08	8	mA	$\overline{CS}$ = ≥ V_{CC} –0.2 V 0 V ≤ Vin ≤ 0.2 V or Vin ≥ V_{CC} –0.2 V	
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4 mA	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA	

Note: 1. Typical limits are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1 MHz) *1

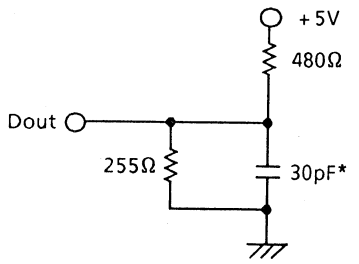
Parameter	Symbol	Min	Max	Unit	Test condition
Input capacitance (Address, $\overline{CS}$, $\overline{OE}$, $\overline{WE}$)	Cin	—	35	pF	Vin = 0 V
Input/output capacitance (DQ)	$C_{I/O}$	—	15	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

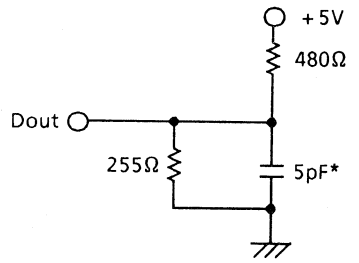
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, unless otherwise noted)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures



Output Load (A)
* Including scope & jig



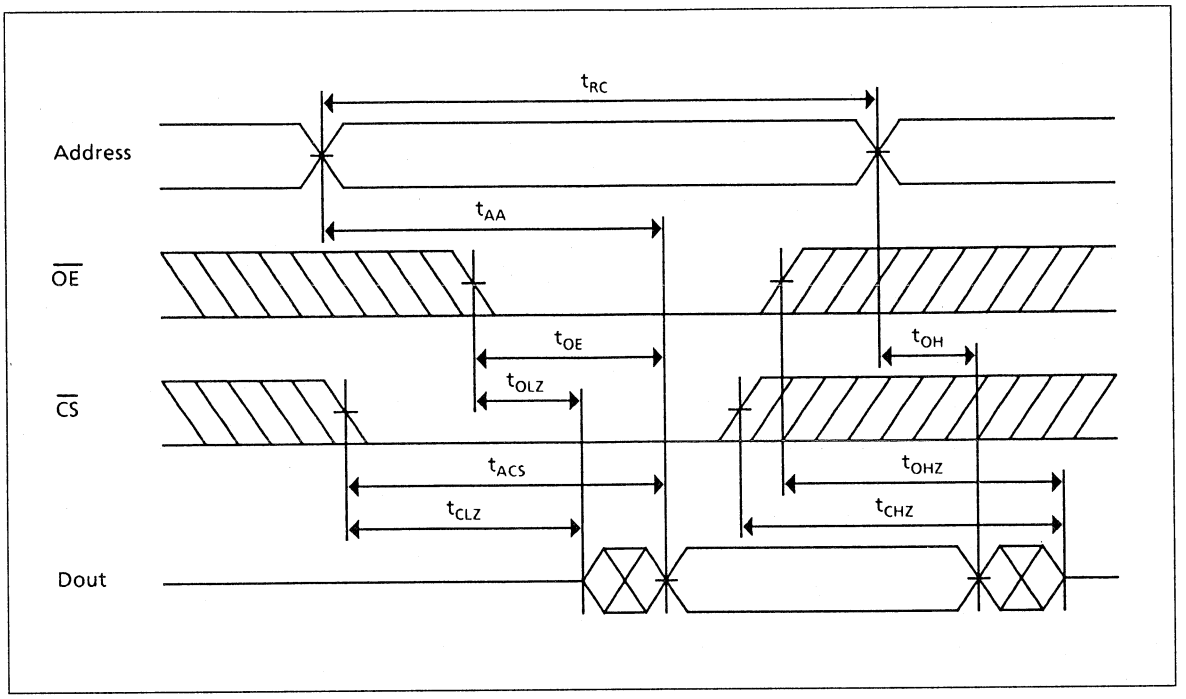
Output Load (B)
(for t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{WHZ}, t_{OW})

Read Cycle

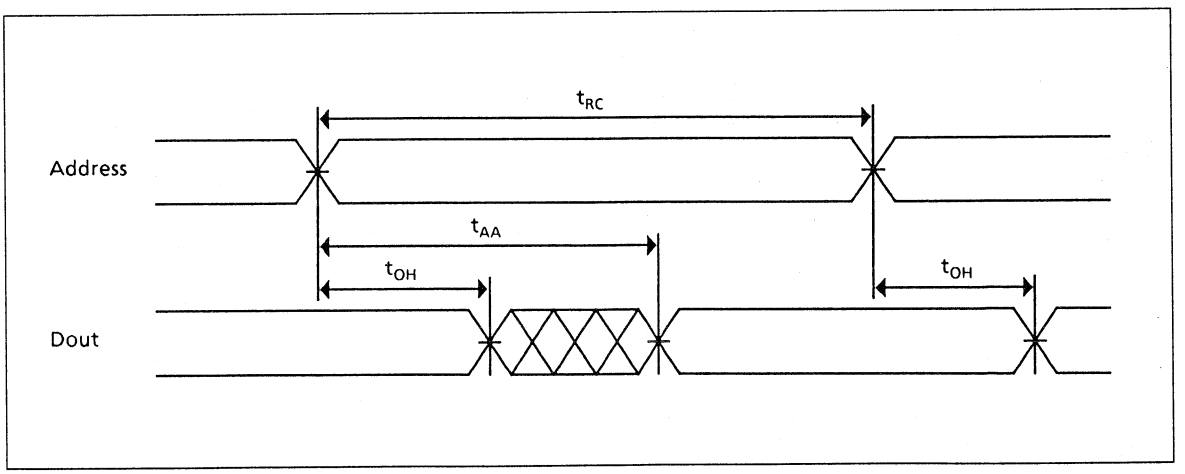
Parameter	Symbol	HB66B1616A-25 Min	HB66B1616A-25 Max	HB66B1616A-35 Min	HB66B1616A-35 Max	Unit
Read cycle time	t_{RC}	25	—	35	—	ns
Address access time	t_{AA}	—	25	—	35	ns
Chip select access time	t_{ACS}	—	25	—	35	ns
Chip selection to output in low-Z	t_{CLZ}*1	5	—	5	—	ns
Output enable to output valid	t_{OE}	—	12	—	15	ns
Output enable to output in low-Z	t_{OLZ}*1	0	—	0	—	ns
Chip deselection to output in high-Z	t_{CHZ}*1	0	12	0	20	ns
Chip disable to output in high-Z	t_{OHZ}*1	0	10	0	10	ns
Output hold from address change	t_{OH}	3	—	5	—	ns
Chip selection to power up time	t_{PU}	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	25	—	30	ns

Note: 1. Output transition is measured ±200 mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tasted.

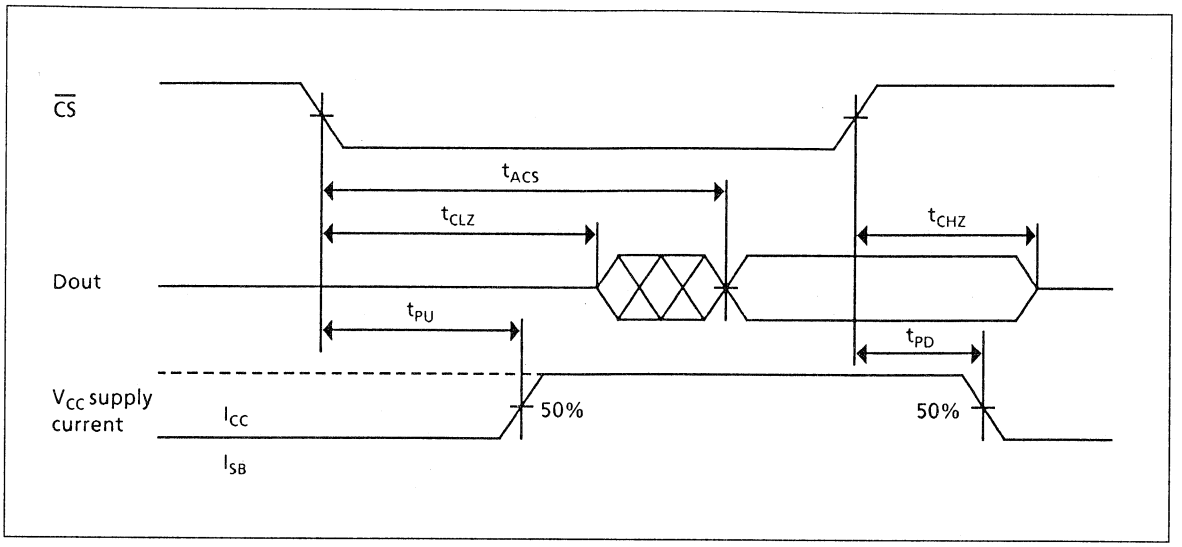
Read Timing Waveform (1) *1



Read Timing Waveform (2) *1, *2, *4



Read Timing Waveform (3) *1, *3, *4



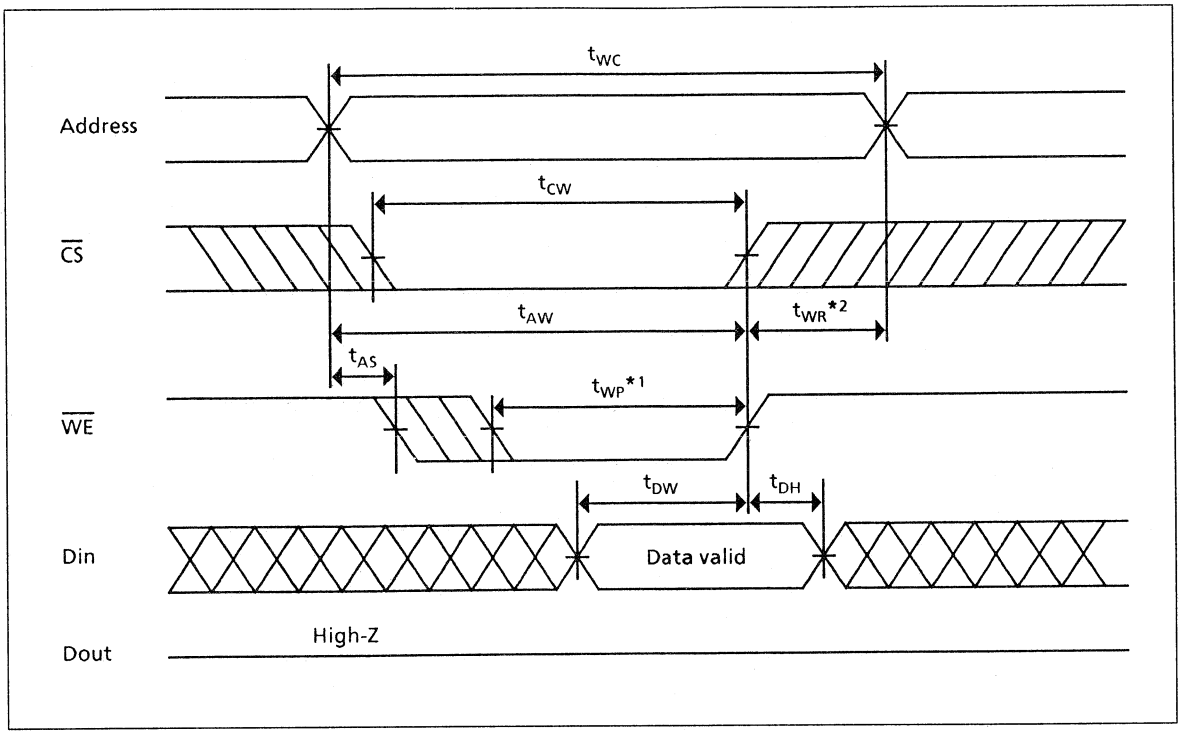
Notes: 1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE}$ = V_{IL}.

Write Cycle

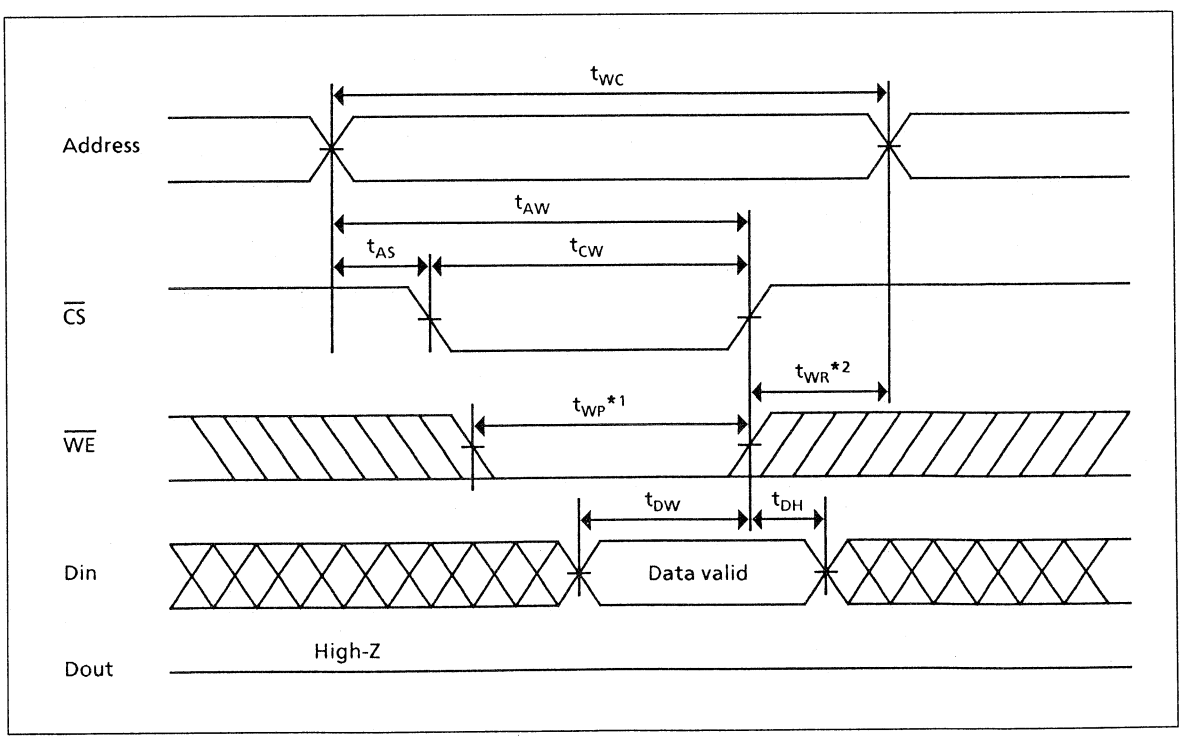
		HB66B1616A-25		HB66B1616A-35		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time	t_{WC}	25	—	35	—	ns
Chip selection to end of write	t_{CW}	20	—	30	—	ns
Address valid to end of write	t_{AW}	20	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	30	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Output disable to output in high-Z	t_{OHZ}*1	0	10	0	10	ns
Write to output in high-Z	t_{WHZ}*1	0	8	0	10	ns
Data to write time overlap	t_{DW}	12	—	20	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Output active from end of write	t_{OW}*1	5	—	5	—	ns

Note: 1. Output transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tasted.

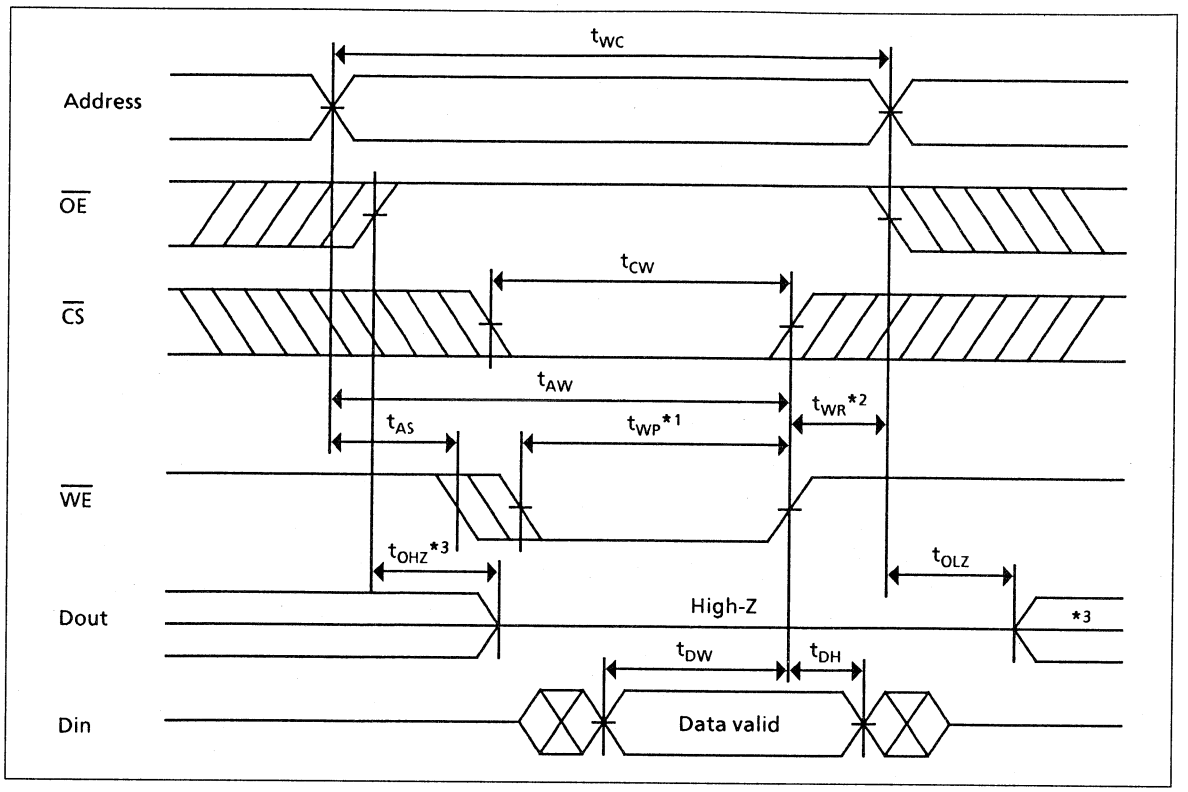
Write Timing Waveform (1) ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



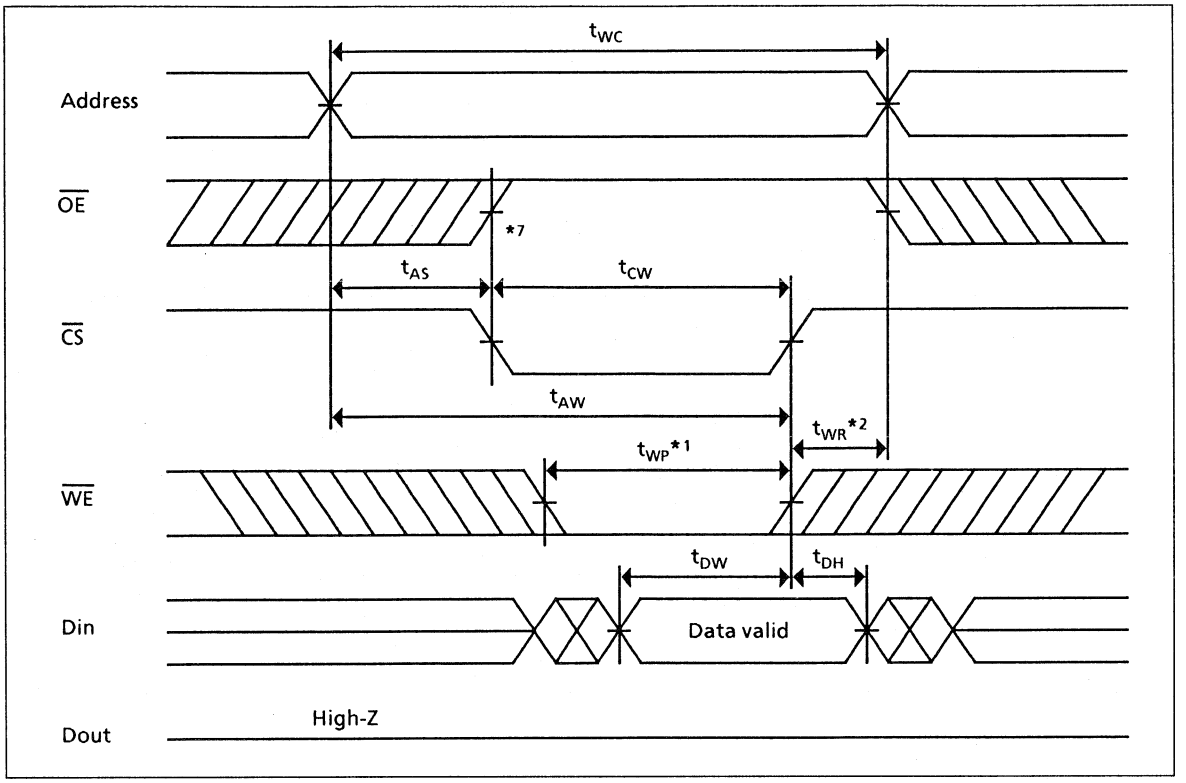
Write Timing Waveform (2) ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



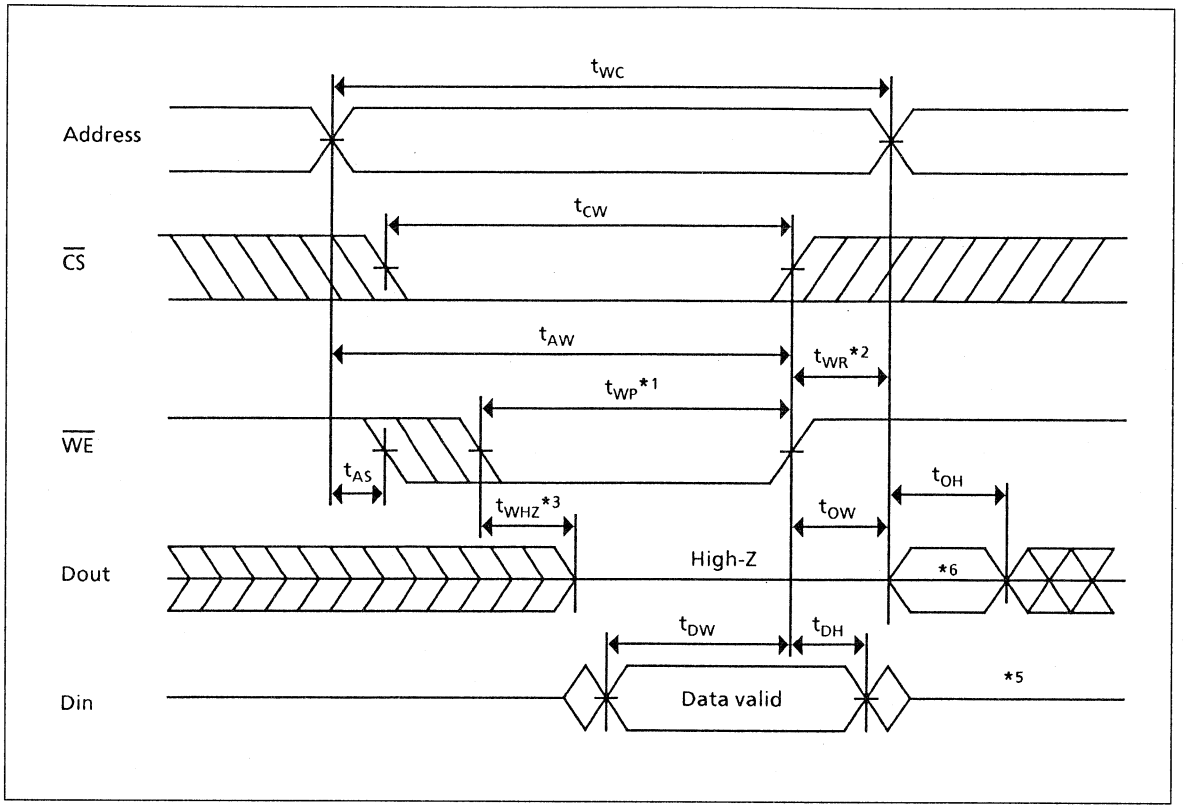
Write Timing Waveform (3) ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



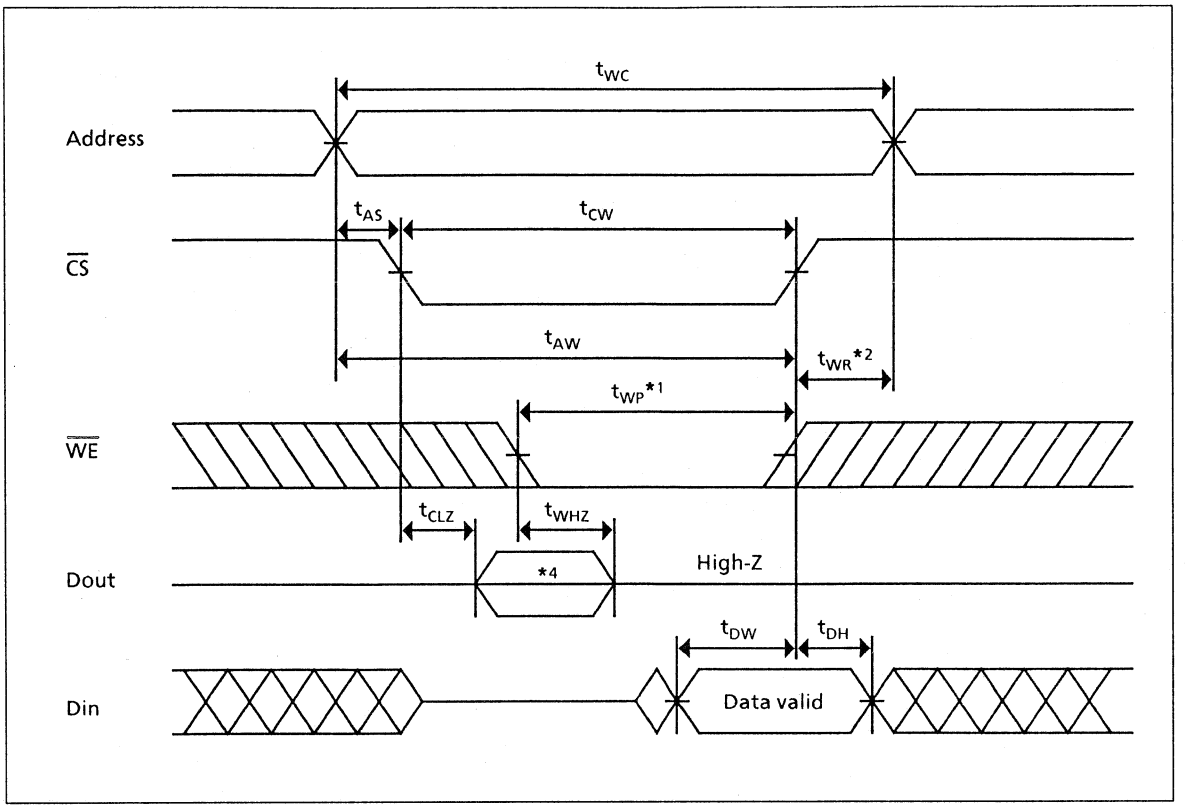
Write Timing Waveform (4) ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



Write Timing Waveform (5) ($\overline{OE}$ = L, $\overline{WE}$ Controlled)

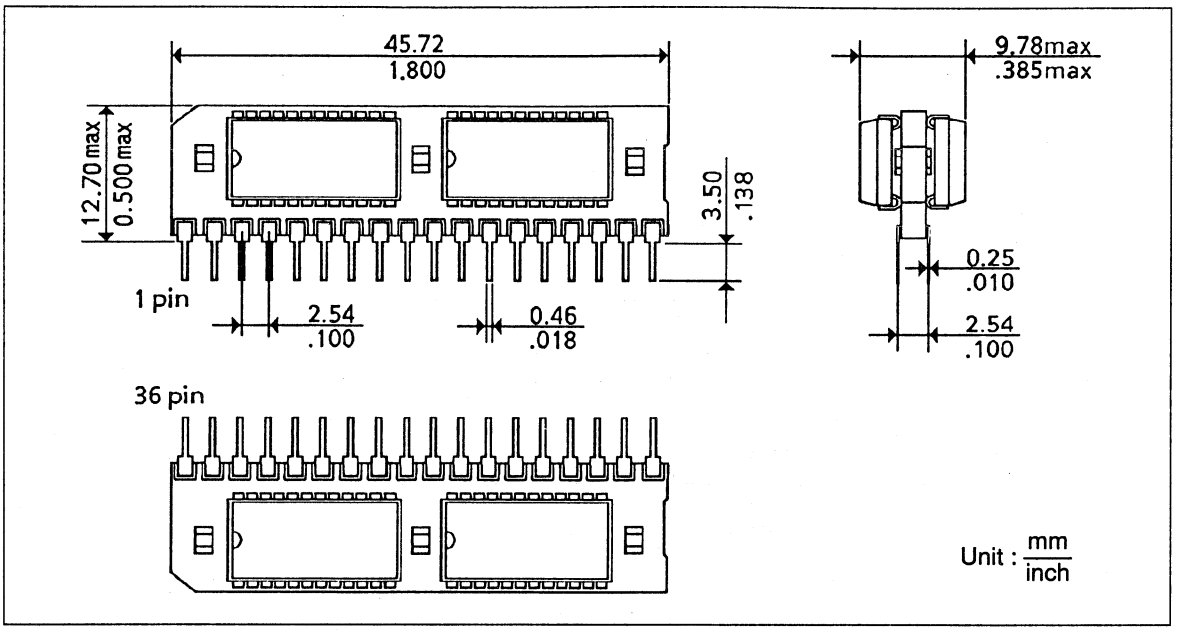


Write Timing Waveform (6) ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



Notes:
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state after t_{OW}.
   Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the sample phase of write data of this write cycle, if t_{WR} is long enough.
7. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, the output buffers remain in a high impedance state.

Package Dimension



HB66A2568A Series

262,144-word × 8-bit High Speed Static RAM Module

The HB66A2568A is a high speed 256k × 8 Static RAM module, mounted 8 pieces of 256-kbit SRAM (HM6207HJP) sealed in SOJ package. An outline of the HB66A2568A is 60-pin zigzag in-line package. Therefore, the HB66A2568A makes high density mounting possible without surface mount technology. The HB66A2568A provides separate data inputs and output. Its module board has decoupling capacitors to reduce noise.

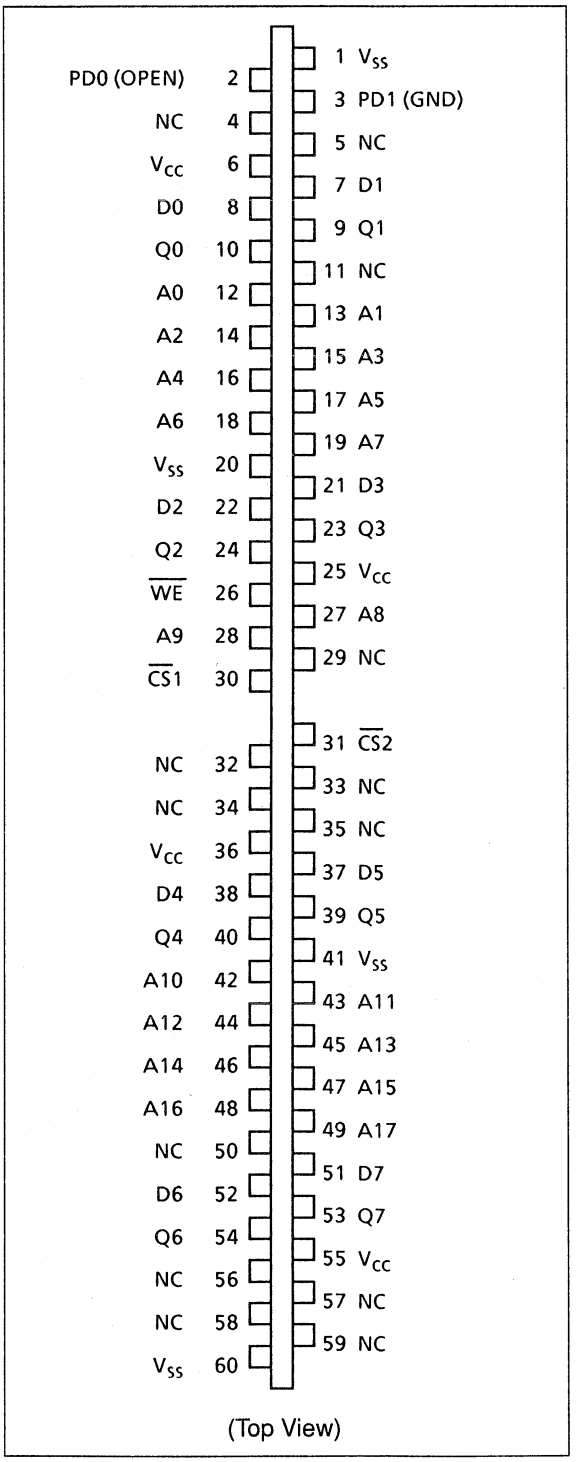
Features

- Single 5 V (±10%) supply
- High speed
  Access time: 25 ns/35 ns (max)
- Low power dissipation
  Active mode: 2400 mW typ
  Standby mode: 800 mW typ (TTL level)
  0.8 mW typ (CMOS level)
- Equal access and cycle time
- Completely static RAM
  No clock or timing strobe required
- Directly TTL compatible: All inputs and outputs

Ordering Information

Type No.	Access time	Package
HB66A2568A-25	25 ns	60-pin zigzag in-line leaded type
HB66A2568A-35	35 ns	

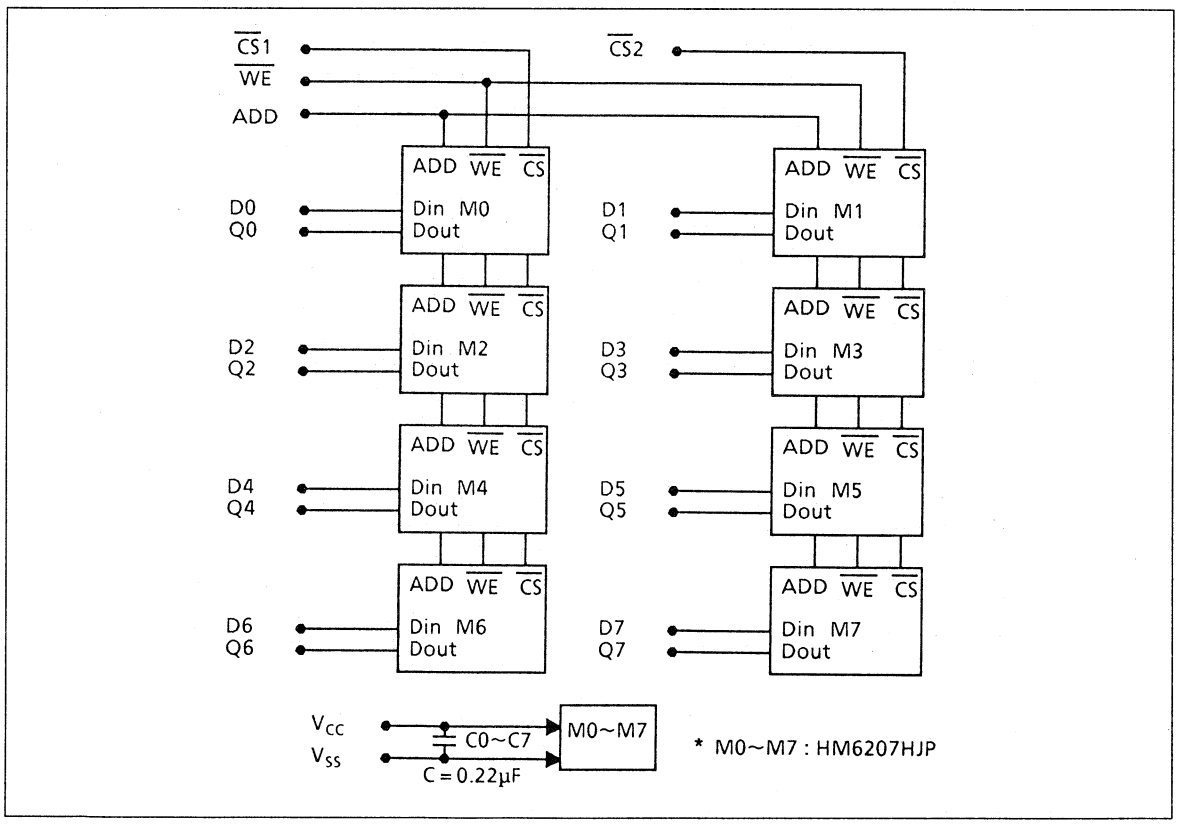
Pin Arrangement



Pin Description

Pin name	Function
A0 – A17	Address Input
D0 – D7	Data-in
Q0 – Q7	Data-out
$\overline{CS1}$, $\overline{CS2}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	Vin	–0.5*1 to +7.0	V
Power dissipation	P_T	8.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–10 to + 85	°C

Note: 1. Vin min = –2.5V for pulse width ≤ 10 ns.

Truth Table

$\overline{CS}$1, 2	$\overline{WE}$	Mode	V_{CC} current	Dout pin	Ref. cycle
H	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	I_{CC}	Dout	Read cycle
L	L	Write	I_{CC}	High-Z	Write cycle

Note: X means don't care.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note : 1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test condition	Note
Input leakage current	I_{LI}	–10	—	10	µA	V_{CC} = Max. Vin = V_{SS} to V_{CC}	
Output leakage current	I_{LO}	–10	—	10	µA	$\overline{CS}$1,2 = V_{IH} $V_{I/O}$= V_{SS} to V_{CC}	
Operating power supply current	I_{CC}	—	480	960	mA	$\overline{CS}$1,2 = V_{IL}, $I_{I/O}$ 0 mA min. cycle, duty = 100%	
Standby power supply current	I_{SB}	—	160	320	mA	$\overline{CS}$1,2 = V_{IH} min. cycle	
Standby power supply current (1)	I_{SB1}	—	0.16	16	mA	$\overline{CS}$1,2 ≥ V_{CC} –0.2 V 0 V ≤ Vin ≤ 0.2 V or Vin ≥ V_{CC} –0.2 V	
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4mA	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA	

Note : 1. Typical limits are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1 MHz) *1

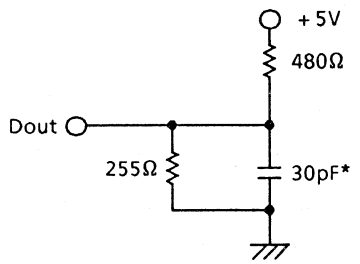
Parameter	Symbol	Min	Max	Unit	Test condition
Input capacitance (Address, $\overline{WE}$)	C_{I1}	—	70	pF	Vin = 0 V
Input capacitance ($\overline{CS}$)	C_{I2}	—	45	pF	Vin = 0 V
Input capacitance (Data in)	C_{I3}	—	12	pF	Vin = 0 V
Output capacitance (Data out)	C_O	—	16	pF	Vout = 0 V

Note : 1. This parameter is sampled and not 100% tested.

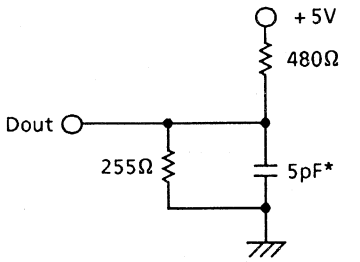
AC Characteristics (Ta = 0°C to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures



Output Load (A)
* Including scope & jig



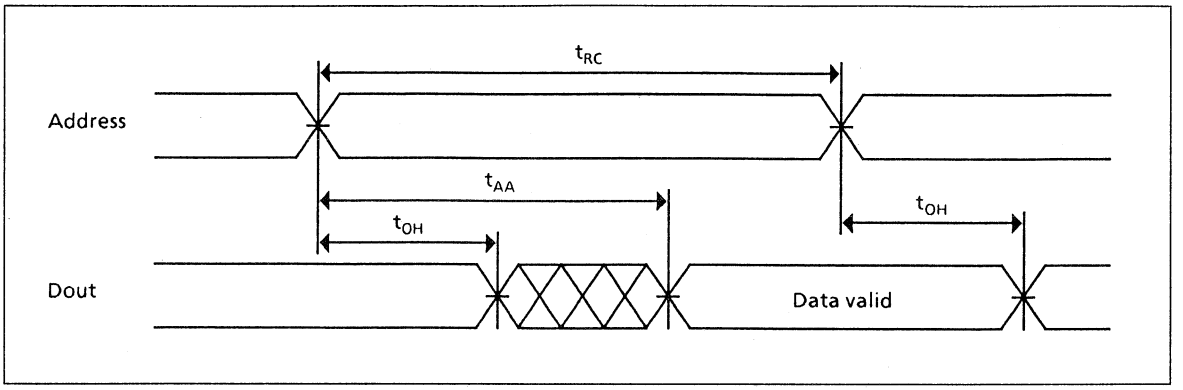
Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

Read Cycle

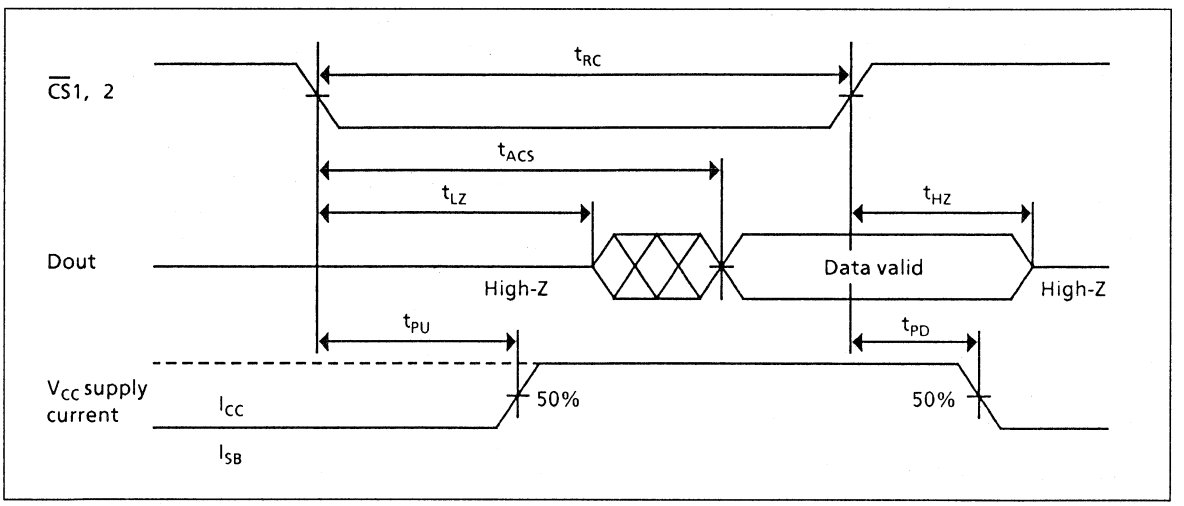
		HB66A2568A-25		HB66A2568A-35		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	25	—	35	—	ns
Address Access time	t_{AA}	—	25	—	35	ns
Chip select access time	t_{ACS}	—	25	—	35	ns
Output hold from address change	t_{OH}	5	—	5	—	ns
Chip selection to output in low-Z	t_{LZ}*1	5	—	5	—	ns
Chip deselection to output in high-Z	t_{HZ}*1	0	12	0	20	ns
Chip selection to power up time	t_{PU}	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	15	—	25	ns

Note : 1. Tansition is measured ±200 mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *3



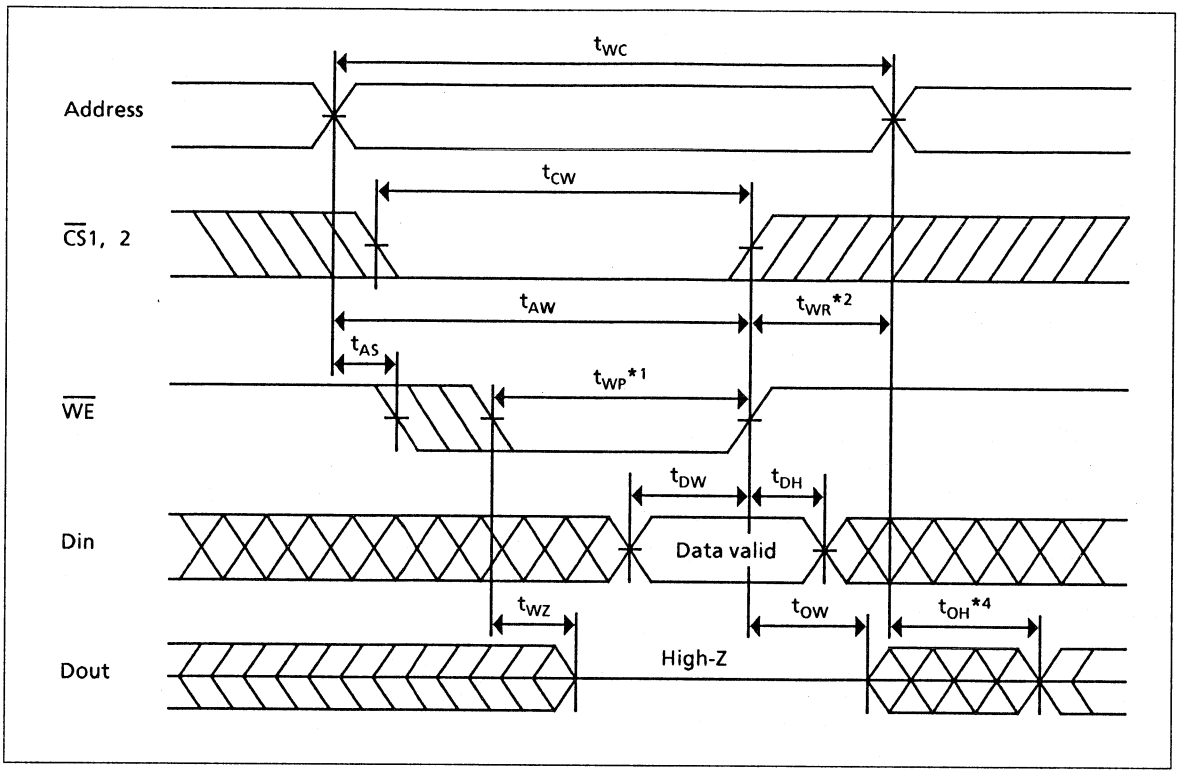
Notes : 1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition Low.

Write Cycle

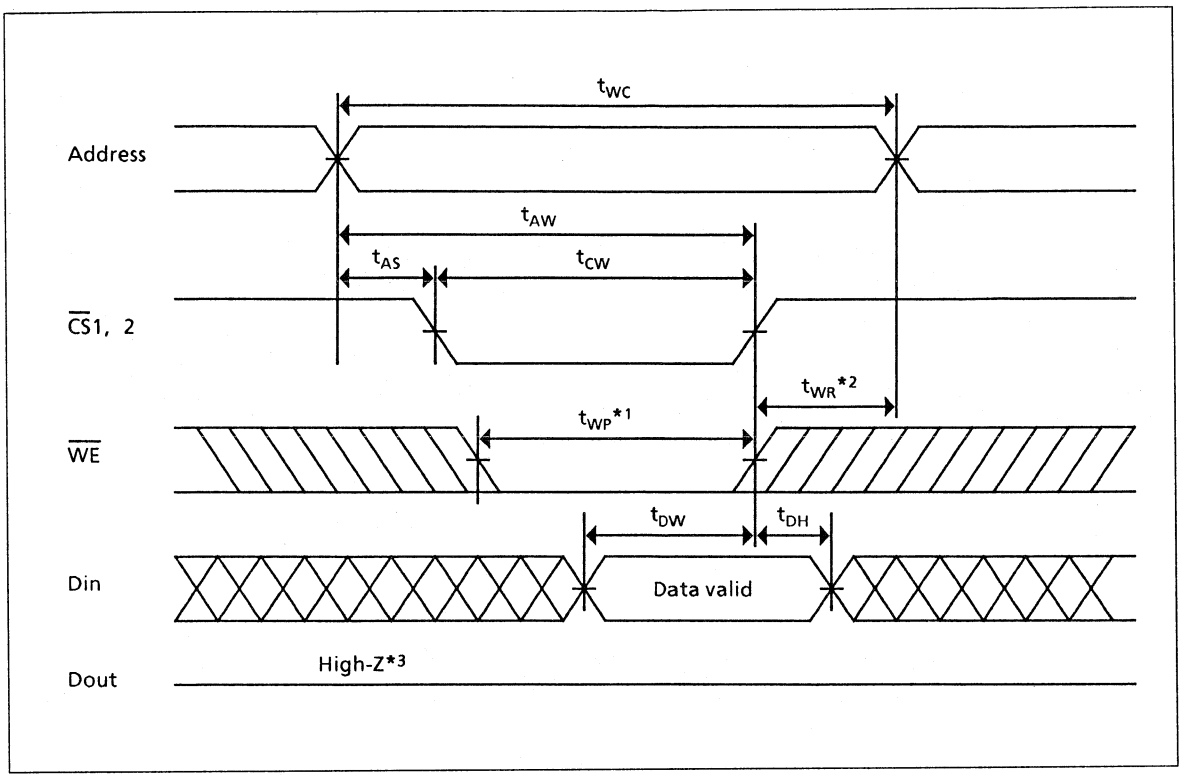
Parameter	Symbol	HB66A2568A-25		HB66A2568A-35		Unit
		Min	Max	Min	Max	
Write cycle time	t_{WC}	25	—	35	—	ns
Chip selection to end of write	t_{CW}	20	—	30	—	ns
Address valid to end of write	t_{AW}	20	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	30	—	ns
Write recovery time	t_{WR}	3	—	3	—	ns
Data valid to end of write	t_{DW}	15	—	20	—	ns
Data hold time	t_{DH}	0	—	0	—	ns
Write enabled to output in high-Z	t_{WZ}*1	0	8	0	10	ns
Output active from end of write	t_{OW}*1	0	—	0	—	ns

Note : 1. Trasition is measured ±200 mV from high impedance voltage with Load (B).
This parameter is sampled and not 100% tested.

Write Timing Waveform (1) ($\overline{WE}$ controlled)

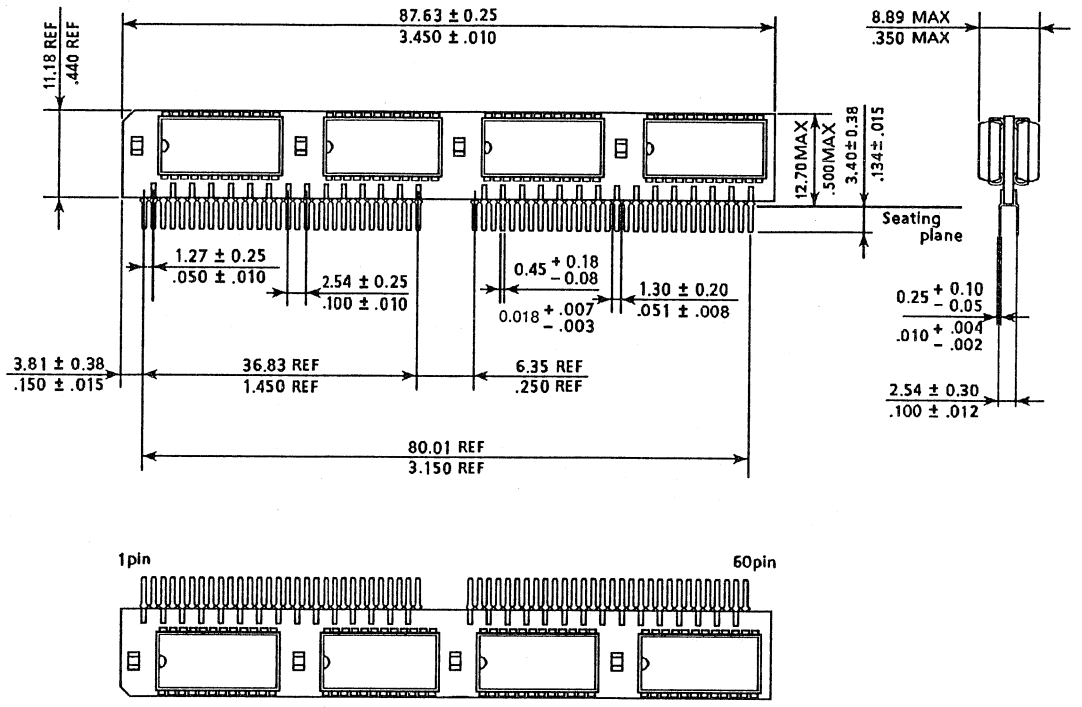


Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes:
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
4. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

Package Dimension



Notes: 1. Unit: $\frac{\text{mm}}{\text{inch}}$

2. Pin NO. 1: Back side

MOS Pseudo Static RAM

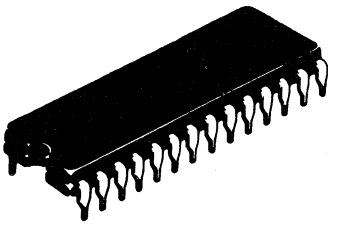
HM65256B Series

32768-word X 8-bit High Speed Pseudo Static RAM

■ FEATURES

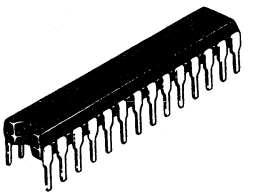
- Single 5V (±10%)
- High Speed
  Access Time
  $\overline{CE}$ Access Time 100/120/150/200ns
  Address Access Time 50/60/75/100ns
  (in Static Column Mode)
  Cycle Time
  Random Read/Write Cycle Time 160/190/235/310ns
  Static Column Mode Cycle Time 55/65/80/105ns
- Low Power
  175mW typ. Active.
- All inputs and outputs TTL compatible
- Static Column Mode Capability
- Non Multiplexed Address
- 256 Refresh Cycles (4ms)
- Refresh Functions
  Address Refresh
  Automatic Refresh
  Self Refresh

HM65256BP Series



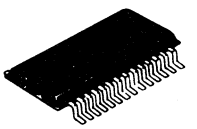
(DP-28)

HM65256BSP Series



(DP-28N)

HM65256BFP Series

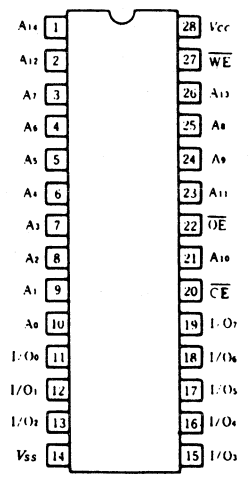


(FP-28DA)

■ ORDERING INFORMATION

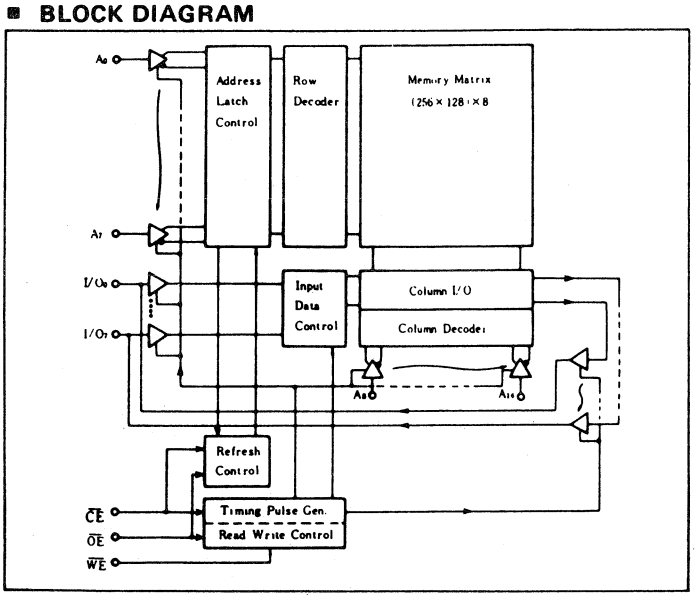
Type No.	Access Time	Package
HM65256BP-10	100ns	600 mil 28 pin Plastic DIP
HM65256BP-12	120ns	
HM65256BP-15	150ns	
HM65256BP-20	200ns	
HM65256BLP-10	100ns	
HM65256BLP-12	120ns	
HM65256BLP-15	150ns	
HM65256BLP-20	200ns	
HM65256BSP-10	100ns	300 mil 28 pin Plastic DIP
HM65256BSP-12	120ns	
HM65256BSP-15	150ns	
HM65256BSP-20	200ns	
HM65256BLSP-10	100ns	
HM65256BLSP-12	120ns	
HM65256BLSP-15	150ns	
HM65256BLSP-20	200ns	
HM65256BFP-10T	100ns	28 pin Plastic SOP
HM65256BFP-12T	120ns	
HM65256BFP-15T	150ns	
HM65256BFP-20T	200ns	
HM65256BLFP-10T	100ns	
HM65256BLFP-12T	120ns	
HM65256BLFP-15T	150ns	
HM65256BLFP-20T	200ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	mode
L	L	H	Low Z	Read
L	×	L	High Z	Write
L	H	H	High Z	–
H	L	×	High Z	Refresh
H	H	×	High Z	Standby

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to V_{SS}	V_T	−1.0 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. V_{IL} min = −3.0V for pulse width ≦ 10ns.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Test Conditions	HM65256B Series			HM65256BL Series			Unit
			min.	typ.	max.	min.	typ.	max.	
Operating Power Supply Current	I_{CC1}	$I_{I/O}$ = 0mA, t_{cyc} = min.	–	35	65	–	35	65	mA
Standby Power Supply Current	I_{SB1}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}, $Vin \geq 0V$	–	1	2	–	1	2	mA
	I_{SB2}	$\overline{CE} \geq V_{CC}-0.2V$, $\overline{OE} \geq V_{CC}-0.2V$, $Vin \geq 0$	–	–	–	–	0.05	0.1	mA
Operating Power Supply Current in Self Refresh Mode	I_{CC2}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}, $Vin \geq 0V$	–	1	2	–	0.6	1	mA
	I_{CC3}	$\overline{CE} \geq V_{CC}-0.2V$, $\overline{OE} \leq 0.2V$, $Vin \geq 0V$	–	–	–	–	50	100	μA
Input Leakage Current	I_{LI}	V_{CC} = 5.5V, Vin = V_{SS} to V_{CC}	–10	–	10	–10	–	10	μA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}	–10	–	10	–10	–	10	μA
Output Voltage	V_{OL}	I_{OL} = 2.1 mA	–	–	0.4	–	–	0.4	V
	V_{OH}	I_{OH} = –1 mA	2.4	–	–	2.4	–	–	V

■ CAPACITANCE

Item	Symbol	Test Conditions	typ.	max.	Unit
Input Capacitance	Cin	Vin = 0V	–	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	7	pF

Note) This Parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±10%)

● AC Test Conditions

Input Pulse Levels 2.4V, 0.4V
Input Rise and Fall Times 5ns
Timing Measurement Level 2.2V, 0.8V
Reference Level . . . . . V_{OH} = 2.0V, V_{OL} = 0.8V
Output Load . . . . . 1 TTL and 100pF (including scope and jig)

Item	Symbol	HM65256B-10		HM65256B-12		HM65256B-15		HM65256B-20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Random Read or Write Cycle Time	t_{RC}	160	–	190	–	235	–	310	–	ns
Static Column Mode Read or Write Cycle	t_{RSC}	55	–	65	–	80	–	105	–	ns
Chip Enable Access Time	t_{CEA}	–	100	–	120	–	150	–	200	ns
Address Access Time	t_{AA}	–	50	–	60	–	75	–	100	ns
Output Enable Access Time	t_{OEA}	–	40	–	50	–	60	–	75	ns
Chip Disable to Output in High Z	t_{CHZ}	–	25	–	25	–	30	–	35	ns
Chip Enable to Output in Low Z	t_{CLZ}	30	–	30	–	35	–	40	–	ns
Output Enable to Output in Low Z	t_{OLZ}	10	–	10	–	10	–	10	–	ns
Output Disable to Output in High Z	t_{OHZ}	–	25	–	25	–	30	–	35	ns
Chip Enable Pulse Width	t_{CE}	100n	4m	120n	4m	150n	4m	200n	4m	s
Chip Enable Precharge Time	t_P	50	–	60	–	75	–	100	–	ns
Address Set-up Time	t_{AS}	0	–	0	–	0	–	0	–	ns
Row Address Hold Time	t_{RAH}	20	–	20	–	25	–	30	–	ns
Column Address Hold Time	t_{CAH}	100	–	120	–	150	–	200	–	ns
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	0	–	ns
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	0	–	ns
Output Enable Hold Time	t_{OHC}	0	–	0	–	0	–	0	–	ns
Output Enable to Chip Enable Delay Time	t_{OCD}	0	–	0	–	0	–	0	–	ns
Output Hold Time from Column Address	t_{OH}	5	–	5	–	5	–	10	–	ns
Write Command Pulse Width	t_{WP}	25	–	25	–	30	–	35	–	ns
Chip Enable to End of Write	t_{CW}	100	–	120	–	150	–	200	–	ns
Column Address Set-up Time	t_{ASW}	0	–	0	–	0	–	0	–	ns

(to be continued)

Item	Symbol	HM65256B-10		HM65256B-12		HM65256B-15		HM65256B-20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Column Address Hold Time after Write	t_{AHW}	0	–	0	–	0	–	0	–	ns
Data Valid to End of Write	t_{DW}	20	–	20	–	25	–	30	–	ns
Data In Hold Time for Write	t_{DH}	0	–	0	–	0	–	0	–	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	5	–	ns
Write to Output in High Z	t_{WHZ}	–	25	–	25	–	30	–	35	ns
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns
Refresh Command Delay Time	t_{RFD}	50	–	60	–	75	–	100	–	ns
Refresh Precharge Time	t_{FP}	30	–	30	–	30	–	30	–	ns
Refresh Command Pulse Width for Automatic Refresh	t_{FAP}	80	10000	80	10000	80	10000	80	10000	ns
Automatic Refresh Cycle Time	t_{FC}	160	–	190	–	235	–	310	–	ns
Refresh Command Pulse Width for Self Refresh	t_{FAS}	10000	–	10000	–	10000	–	10000	–	ns
Refresh Reset Time for Self Refresh	t_{FRS}	160	–	190	–	235	–	310	–	ns
Refresh Period	t_{REF}	–	4	–	4	–	4	–	4	ms

Notes:

(1) t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit conditions.

(2) t_{CLZ}, t_{OLZ} and t_{OW} are sampled under the condition of t_T=5ns, and not 100% tested.

(3) A write occurs during the overlap of a low $\overline{CE}$ and low $\overline{WE}$.

(4) If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.

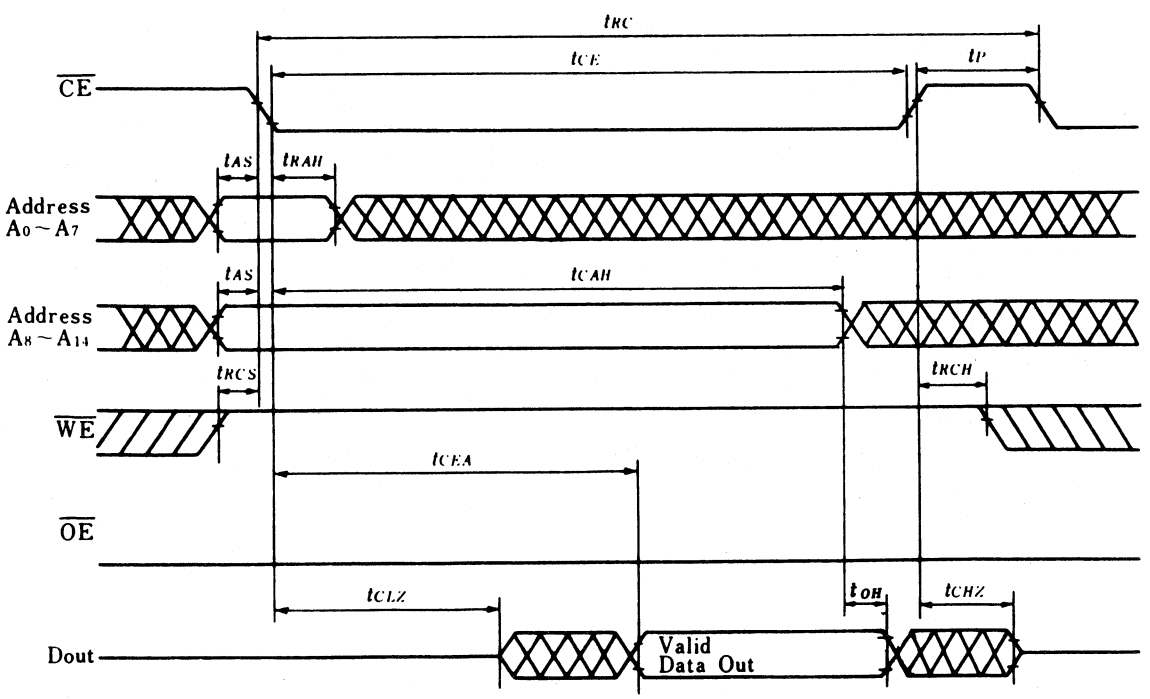
(5) If input signals of opposite phase to the outputs are applied in write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and data inputs must be floating prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.

(6) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

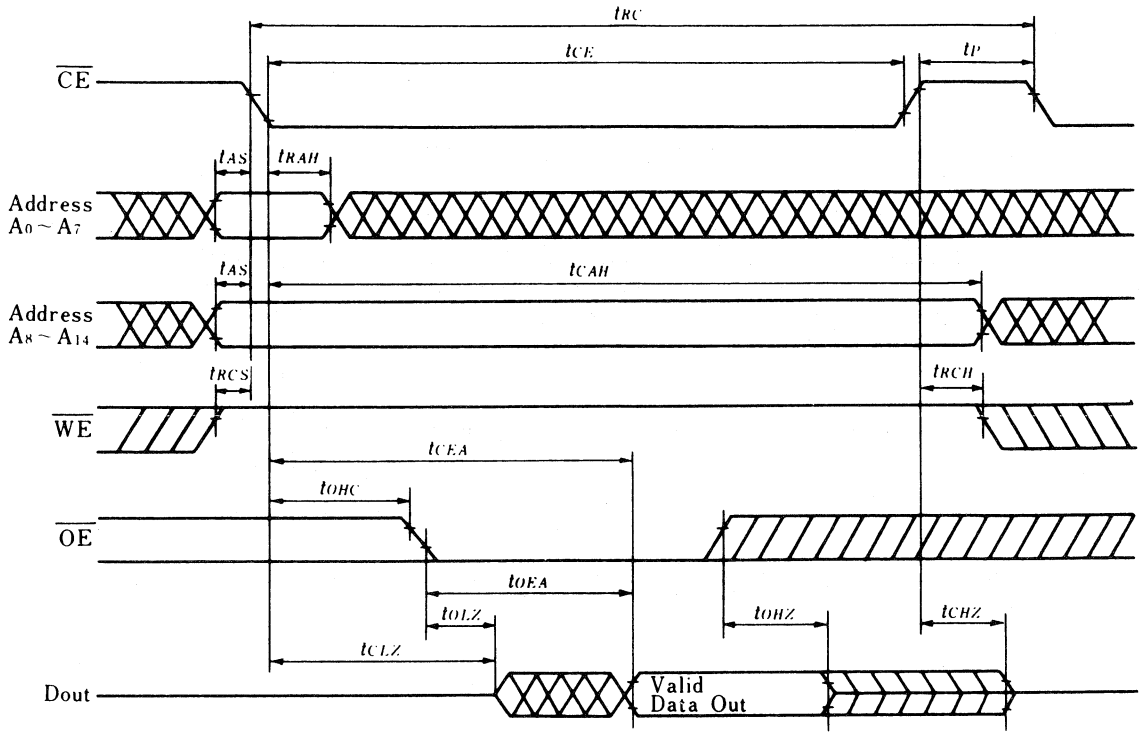
(7) An initial pause of 100μs is required after power-up followed by a minimum of 8 initialization cycles.

■ TIMING WAVEFORMS

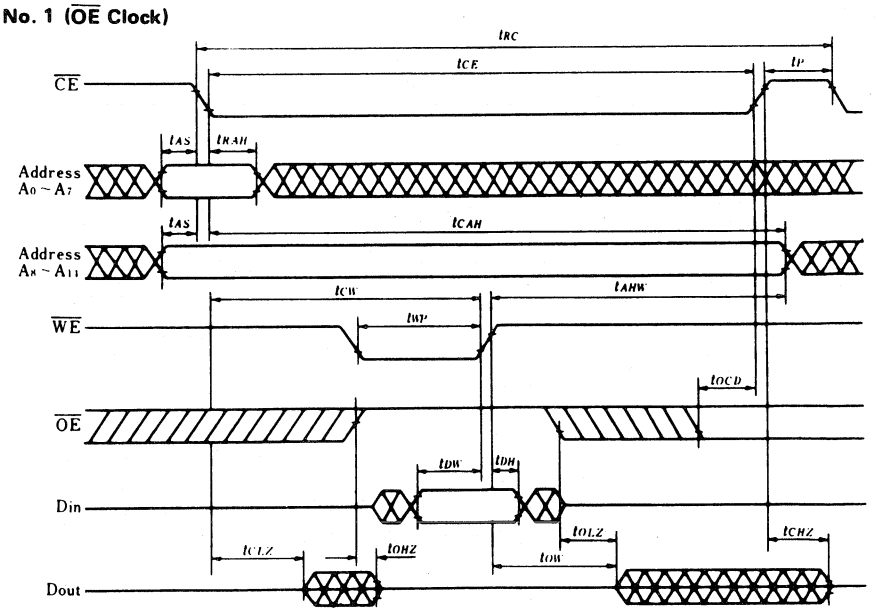
• Read Cycle No. 1 ($\overline{CE}$ controlled)



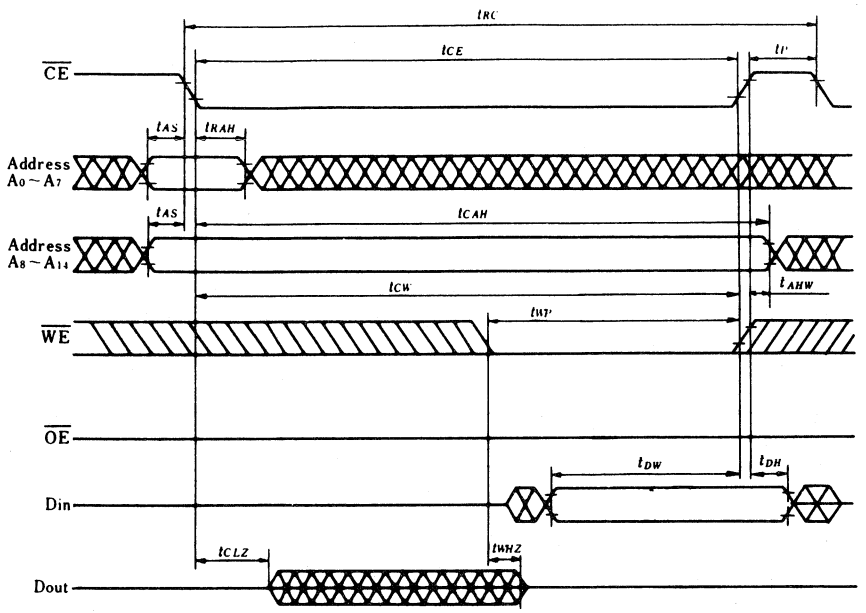
- **Read Cycle No. 2 ($\overline{OE}$ controlled)**



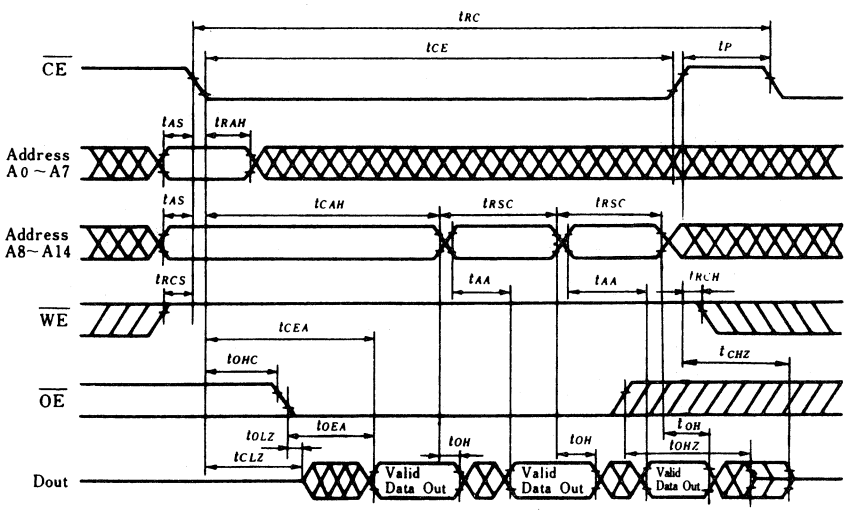
- **Write Cycle No. 1 ($\overline{OE}$ Clock)**



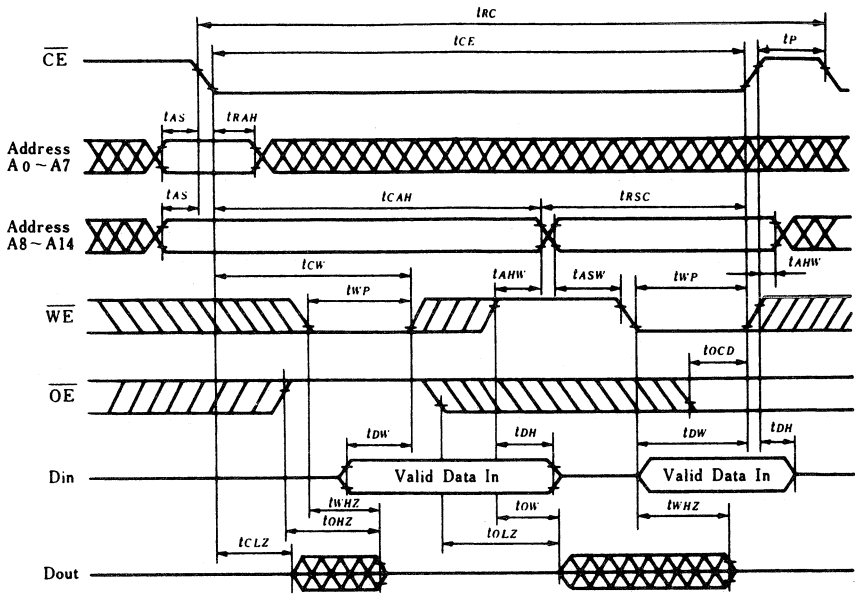
- **Write Cycle No. 2 ($\overline{OE}$ low fix)**



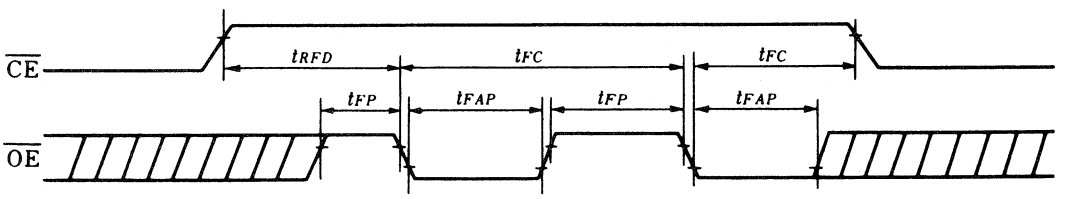
- **Static Column Mode Read Cycle**



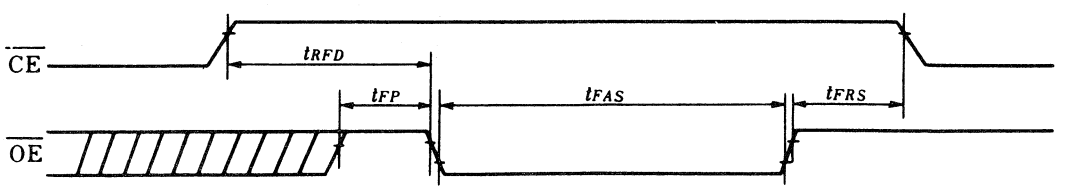
- **Static Column Mode Write Cycle**



- **Automatic Refresh Cycle**



- **Self Refresh Cycle**



HM658128A Series

131072-word × 8-bit High Speed CMOS Pseudo Static RAM

The Hitachi HM658128A is a pseudo-static RAM organized as 131,072-word × 8-bit. HM658128A realizes low power consumption and high speed access time by employing 1.3 µm CMOS process technology.

The HM658128A supports 3 refresh functions: address refresh, auto refresh and self refresh. Low power version dissipates only 0.5 mW (typ) in self refresh mode and retains the data with battery. Self refresh mode is guaranteed only for L-version and LL-version.

The HM658128A is pin-compatible with 1-Mbit static RAM.

Features

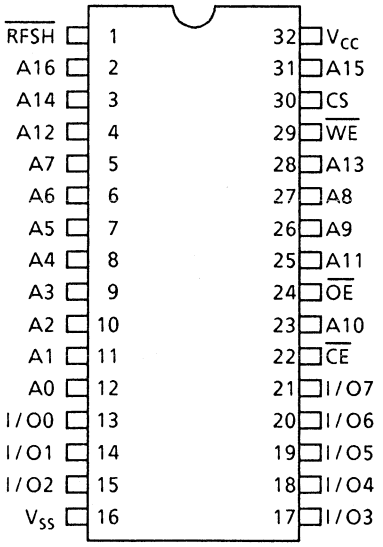
- Single 5 V (± 10%)
- High speed
  - Access time
    $\overline{CE}$ Access time: 80/100/120 ns
  - Cycle time
    Random read/
    Write cycle time : 130/160/190 ns
- Low power: 300 mW typ (active)
  0.5 mW (standby)
- All inputs and outputs TTL compatible
- Non multiplexed address
- 512 refresh cycles (8 ms)
- Refresh functions
  Address refresh
  Automatic refresh
  Self refresh (Only for L-version and LL-version)

Ordering Information

Type No.	Access time	Package
HM658128ADP-8	80 ns	600-mil 32-pin plastic DIP (DP-32)
HM658128ADP-10	100 ns	
HM658128ADP-12	120 ns	
HM658128ALP-8	80 ns	
HM658128ALP-10	100 ns	
HM658128ALP-12	120 ns	
HM658128ALP-8L	80 ns	
HM658128ALP-10L	100 ns	
HM658128ALP-12L	120 ns	
HM658128ADFP-8	80 ns	32-pin plastic SOP (FP-32D)
HM658128ADFP-10	100 ns	
HM658128ADFP-12	120 ns	
HM658128ALFP-8	80 ns	
HM658128ALFP-10	100 ns	
HM658128ALFP-12	120 ns	
HM658128ALFP-8L	80 ns	
HM658128ALFP-10L	100 ns	
HM658128ALFP-12L	120 ns	
HM658128ALT-8	80 ns	8 mm × 20 mm 32-pin plastic TSOP (TFP-32D)
HM658128ALT-10	100 ns	
HM658128ALT-12	120 ns	
HM658128ALT-8L	80 ns	
HM658128ALT-10L	100 ns	
HM658128ALT-12L	120 ns	
HM658128ADT-8	80 ns	
HM658128ADT-10	100 ns	
HM658128ADT-12	120 ns	
HM658128ADR-8	80 ns	8 mm × 20 mm 32-pin plastic TSOP reverse type (TFP-32DR)
HM658128ADR-10	100 ns	
HM658128ADR-12	120 ns	
HM658128ALR-8	80 ns	
HM658128ALR-10	100 ns	
HM658128ALR-12	120 ns	
HM658128ALR-8L	80 ns	
HM658128ALR-10L	100 ns	
HM658128ALR-12L	120 ns	

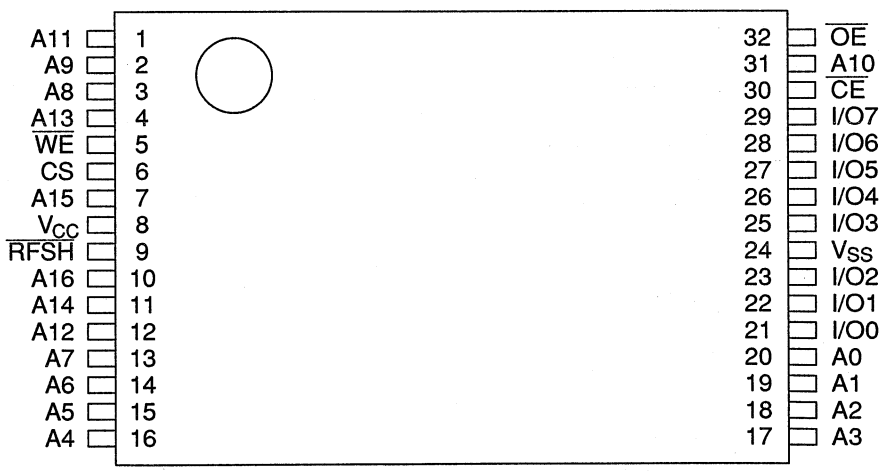
Pin Arrangement

HM658128AP/AFP Series



(Top View)

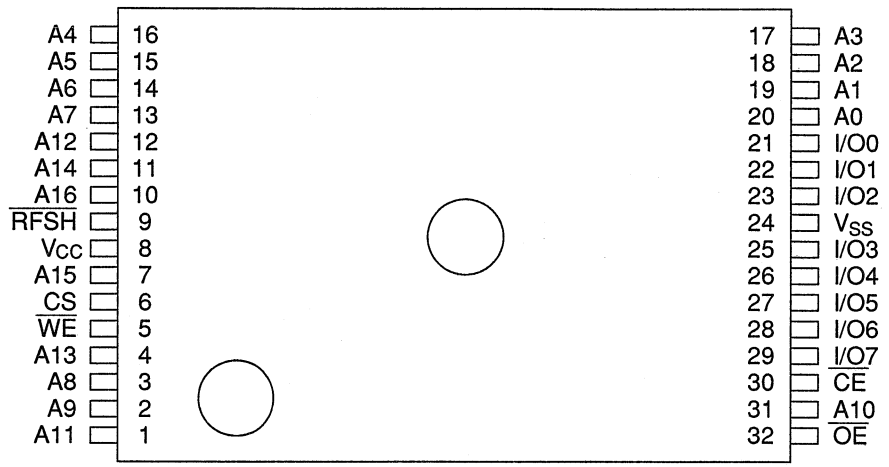
HM658128AT Series



(Top View)

Pin Arrangement (cont)

HM658128AR Series

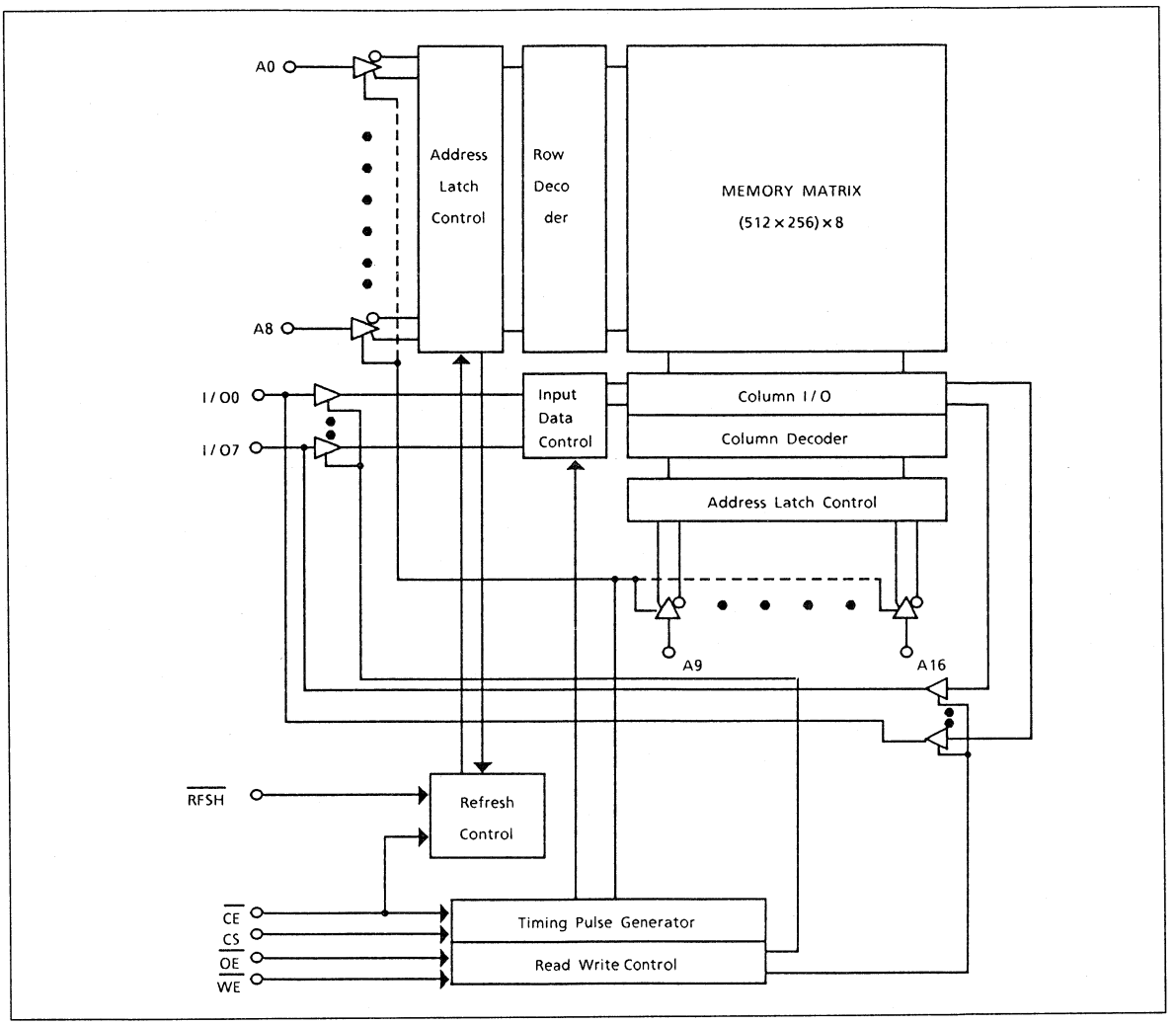


(Top View)

Pin Description

Symbol	Pin name
A0 - A16	Address inputs
I/O0 - I/O7	Data input/output
$\overline{RFSH}$	Refresh
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
CS	Chip select
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Truth Table

$\overline{CE}$	CS at $\overline{CE}$ going low	$\overline{RFSH}$	$\overline{OE}$	$\overline{WE}$	I/O pin	Mode
L	H	X	L	H	Low-Z	Read
L	H	X	X	L	High-Z	Write
L	H	X	H	H	High-Z	—
L	L	X	X	X	High-Z	CS Standby
H	X	L	X	X	High-Z	Refresh*1
H	X	H	X	X	High-Z	Standby

Note: 1. Self refresh is guaranteed only for L-version and LL-version.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage with respect to V_{SS}	V_T	–1.0 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	– 0.5*1	—	0.8	V

Note: 1. V_{IL} min = –3.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Operating power supply current	I_{CC1}	—	60	85	mA	$I_{I/O}$ = 0 mA tcyc = min.
Standby power supply current	I_{SB1}	—	1	2	mA	$\overline{CE}$ = V_{IH} $\overline{RFSH}$ = V_{IH}, Vin ≥ 0 V
Standby power supply current	I_{SB2}	—	100*1	200*1	µA	$\overline{CE}$ ≥ V_{CC} –0.2 V $\overline{RFSH}$ ≥ V_{CC} –0.2 V, Vin ≥ 0 V
		—	70*2	100*2	µA	
Operating power supply current in self refresh mode	I_{CC2}	—	1*1, *2	2*1, *2	mA	$\overline{CE}$ = V_{IH} $\overline{RFSH}$ = V_{IL}, Vin ≥ 0 V
	I_{CC3}	—	100*1	200*2	µA	$\overline{CE}$ ≥ V_{CC} –0.2 V $\overline{RFSH}$ ≤ 0.2 V, Vin ≥ 0 V
		—	70*2	100*2	µA	
Input leakage current	I_{LI}	–10	—	10	µA	V_{CC} = 5.5 V Vin = V_{SS} to V_{CC}
Output leakage current	I_{LO}	–10	—	10	µA	$\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –1 mA

Notes: 1. This characteristics is guaranteed only for L-version.
2. This characteristics is guaranteed only for LL-version.

Capacitance (Ta = 25°C, f = 1 MHz)

Item	Symbol	Typ	Max	Unit	Test condition
Input capacitance	Cin	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0 V

Note: This Parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

Test Conditions

- Input pulse levels: 2.4 V, 0.4 V
- Input rise and fall times: 5 ns
- Timing measurement level: 2.2 V, 0.8 V
- Reference level: V_{OH} = 2.0 V, V_{OL} = 0.8 V
- Output load: 1 TTL and 100 pF (including scope and jig)

		HM658128A-8		HM658128A-10		HM658128A-12		
Itme	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Random read or write cycle time	t_{RC}	130	—	160	—	190	—	ns
Random read-modify-write cycle time	t_{RWC}	190	—	220	—	260	—	ns
Chip enable access time	t_{CEA}	—	80	—	100	—	120	ns
Output enable access time	t_{OEA}	—	30	—	30	—	40	ns
Chip disable to output in high-Z	t_{CHZ}	0	30	0	30	0	35	ns
Chip enable to output in low-Z	t_{CLZ}	20	—	20	—	20	—	ns
Output disable to output in high-Z	t_{OHZ}	—	25	—	25	—	30	ns
Output enable to output in low-Z	t_{OLZ}	0	—	0	—	0	—	ns
Chip enable pulse width	t_{CE}	80 ns	10 µs	100 ns	10 µs	120 ns	10 µs	
Chip enable precharge time	t_{P}	40	—	50	—	60	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Address hold time	t_{AH}	30	—	30	—	35	—	ns
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns
$\overline{\text{RFSH}}$ hold time	t_{RHC}	15	—	15	—	15	—	ns
Chip select setup time	t_{CSS}	0	—	0	—	0	—	ns
Chip select hold time	t_{CSH}	30	—	30	—	35	—	ns
Write command pulse width	t_{WP}	30	—	30	—	35	—	ns
Chip enable to end of write	t_{CW}	80	—	100	—	120	—	ns
Data in to end of write	t_{DW}	25	—	25	—	30	—	ns
Data in hold time for write	t_{DH}	0	—	0	—	0	—	ns

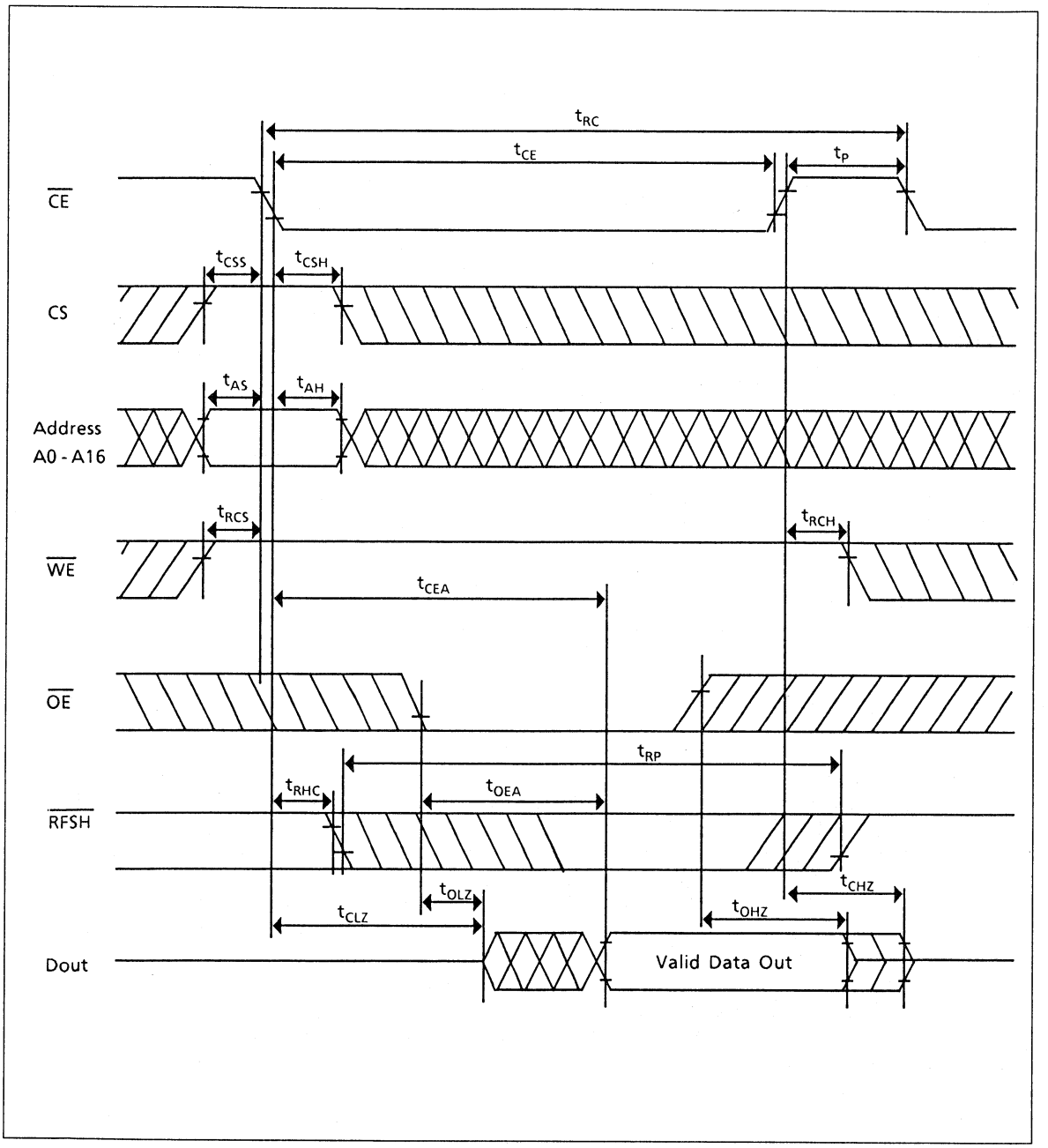
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%) (cont)

Itme	Symbol	HM658128A-8 Min	HM658128A-8 Max	HM658128A-10 Min	HM658128A-10 Max	HM658128A-12 Min	HM658128A-12 Max	Unit
Output active from end of write	t_{OW}	5	—	5	—	5	—	ns
Write to output in high-Z	t_{WHZ}	—	25	—	25	—	30	ns
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns
Refresh command delay time	t_{RFD}	40	—	50	—	60	—	ns
Refresh precharge time	t_{FP}	40	—	40	—	40	—	ns
Refresh command pulse width	t_{RP}	—	8	—	8	—	8	µs
Refresh command pulse width for automatic refresh	t_{FAP}	80 ns	8 µs	80 ns	8 µs	80 ns	8 µs	
Automatic refresh cycle time	t_{FC}	130	—	160	—	190	—	ns
Refresh command pulse width for self refresh	t_{FAS} *9	8	—	8	—	8	—	µs
Refresh reset time for self refresh	t_{RFS} *9	130	—	160	—	190	—	ns
Refresh period (512 cycles)	t_{REF}	—	8	—	8	—	8	ms

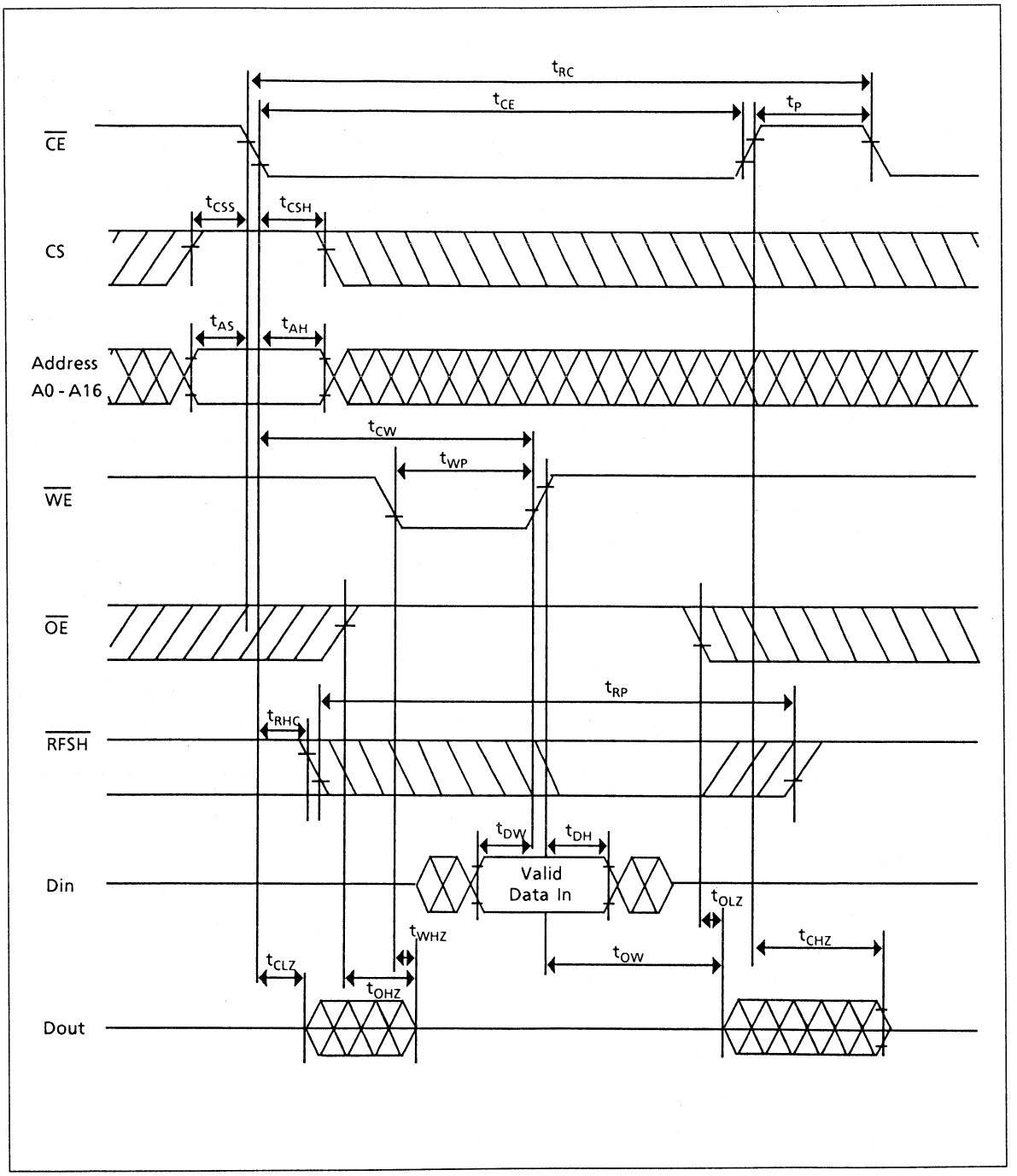
Notes:
1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit conditions.
2. t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ} and t_{OW} are sampled under the condition of t_T = 5 ns and not 100% tested.
3. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. Write ends at the earlier of $\overline{WE}$ going high or $\overline{CE}$ going high.
4. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition, the output buffers remain in high impedance state.
5. In write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and at the end of write cycle data inputs must be floated prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
6. Transition time t_T is measured between V_{IH} min and V_{IL} max.
7. After power-up, pause more than 100 µs and execute at least 8 initialization cycles.
8. 512 cycles of burst refresh or the first cycle of distributed automatic refresh must be executed within 15 µs after self refresh, in order to meet the refresh specification of 8 ms and 512 cycles.
9. This characteristics is guaranteed only for L-version and LL-version.

Timing Waveforms

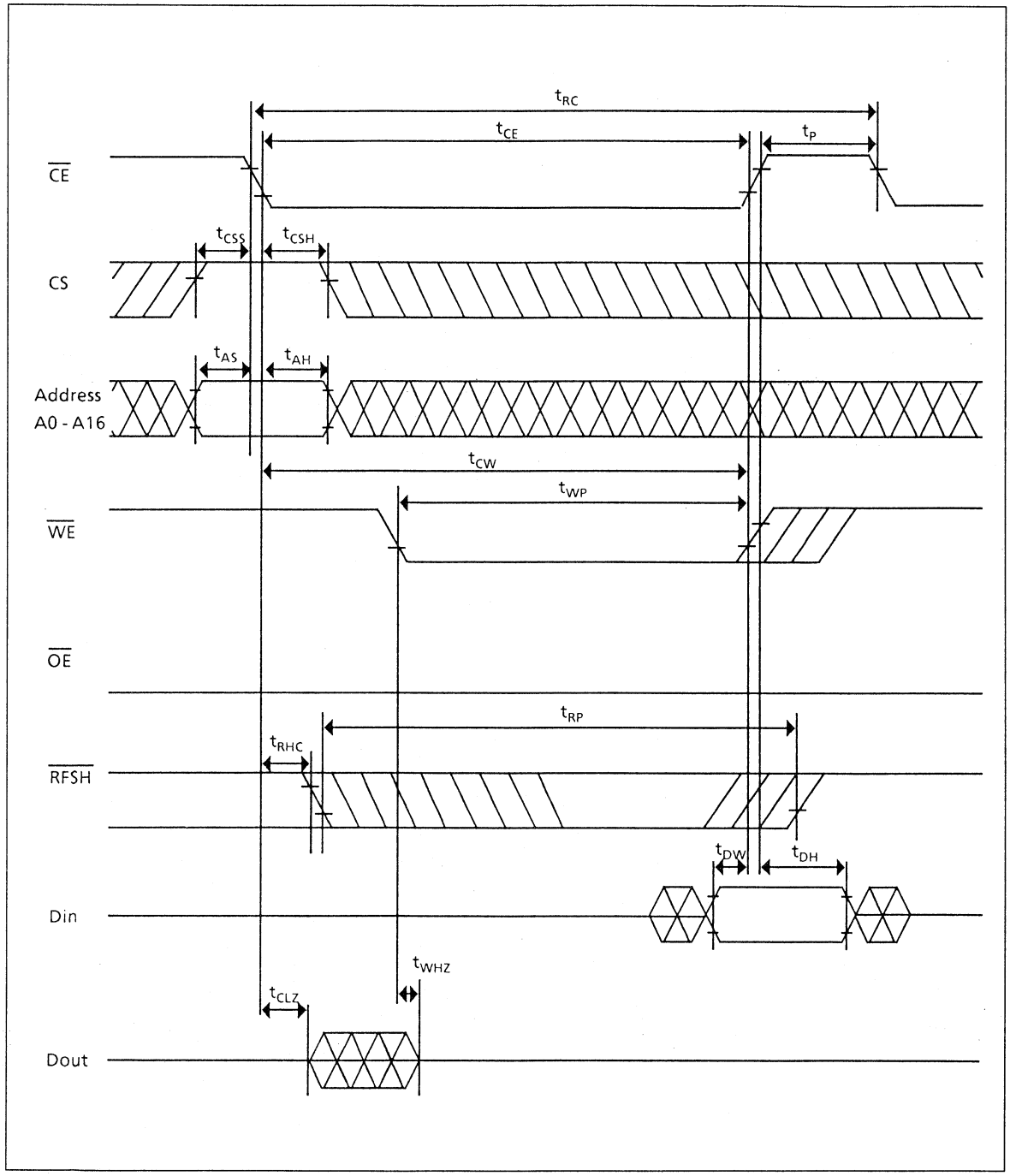
Read Cycle



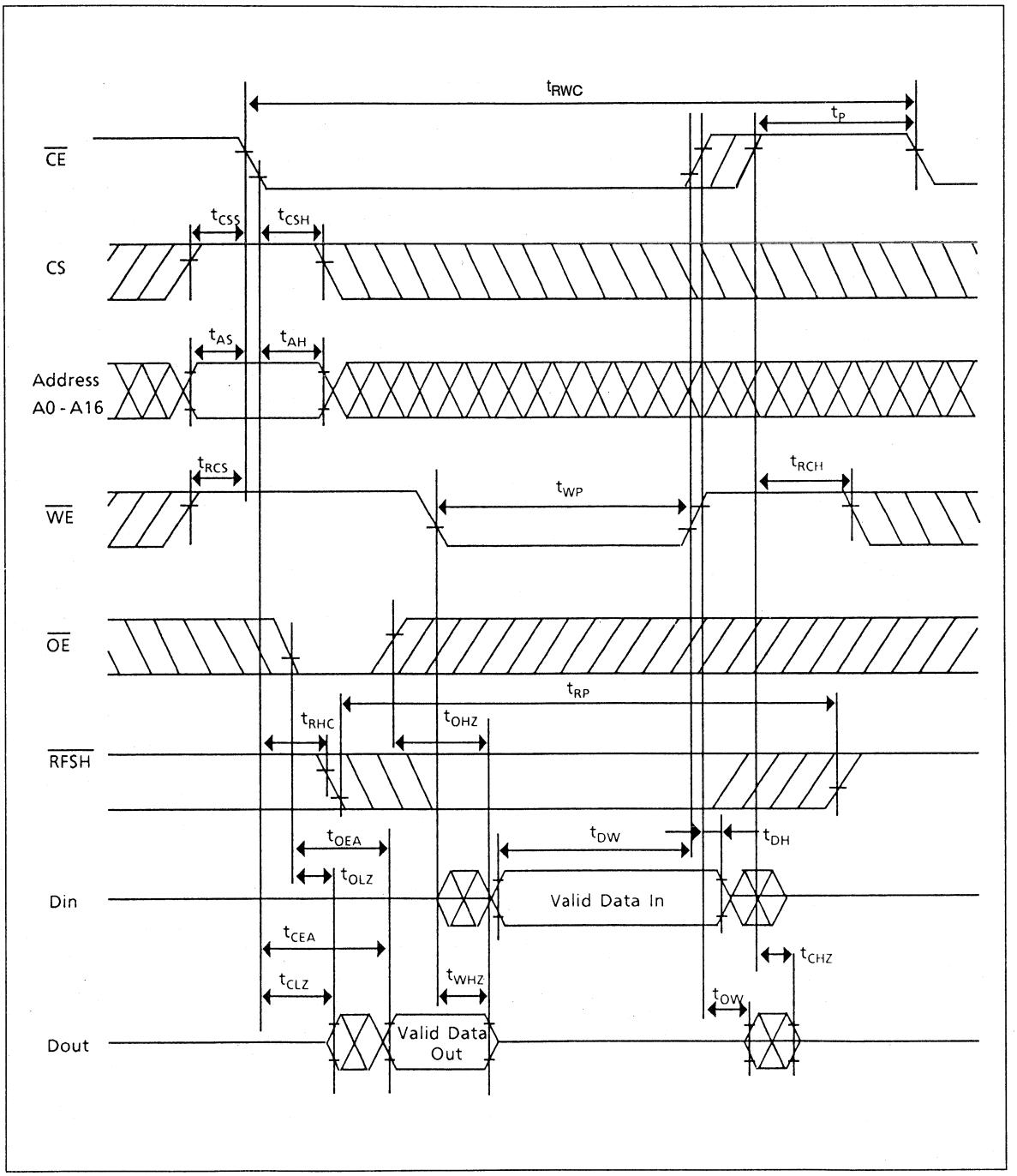
Write Cycle ($\overline{OE}$ clock)



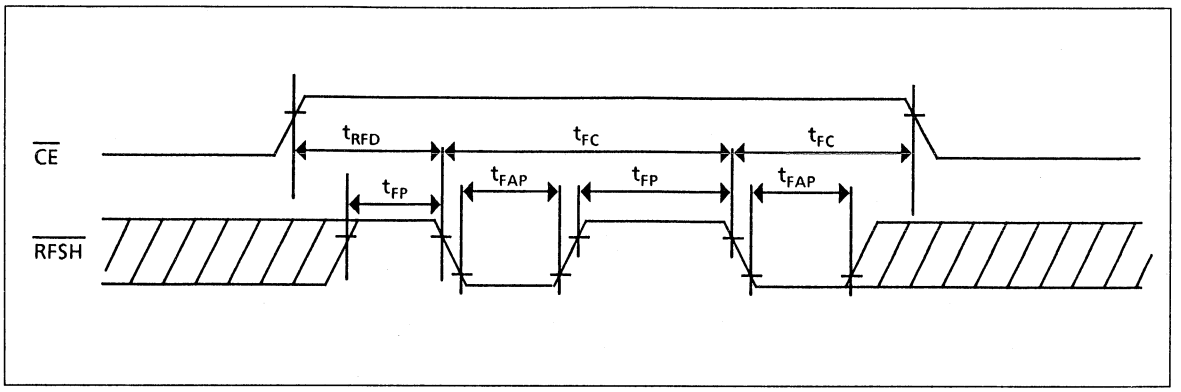
Write Cycle ($\overline{OE}$ Low Fix)



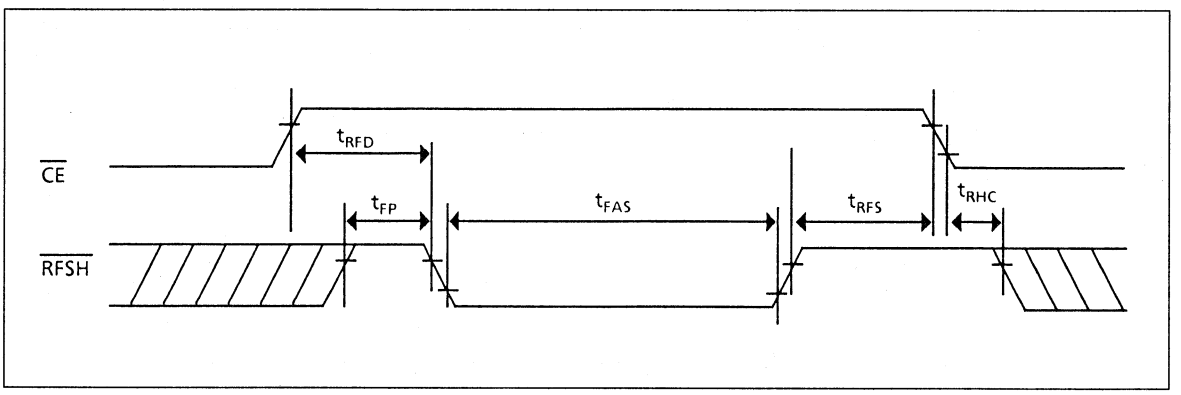
Read-Modify-Write Cycle



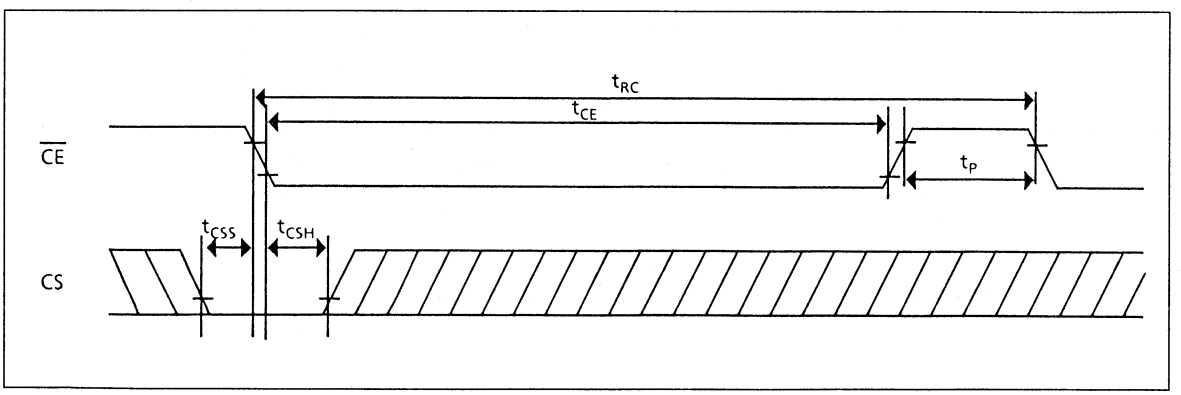
Auto Refresh Cycle



Self Refresh Cycle



CS Standby Mode



HM658512 Series

524288-Word × 8-Bit High Speed Pseudo Static RAM

Features

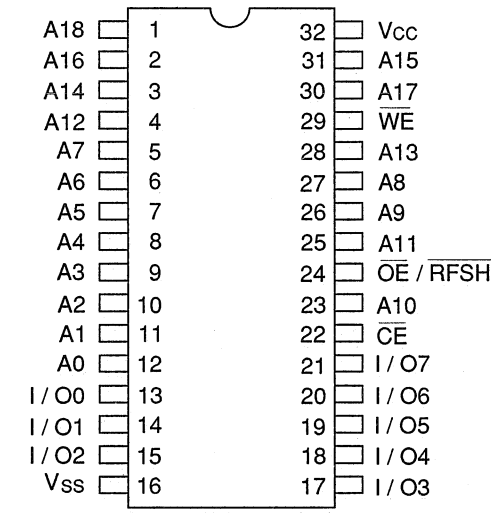
- Single 5 V (± 10%)
- High speed
  - Access time
    $\overline{CE}$ access time: 80/100/120 ns
  - Cycle time
    Random read/write cycle time:
    130/160/190 ns
- Low power
  - 250 mW typ active
  - 350 µW typ standby (L-version)
  - 200 µW typ standby (LL-version)
- All inputs and outputs TTL compatible
- Package
  - 32-pin dual-in-line plastic package
  - 32-pin SOP package
- Non multiplexed address
- 2048 refresh cycles (32 ms)
- Refresh functions
  - L-version: Address refresh
    LL-version Automatic refresh
    Self refresh
  - D-version: Address refresh
    Automatic refresh

Ordering Information

Type No.	Access	Package
HM658512LP-8	80 ns	600 mil 32-pin plastic DIP (DP-32)
HM658512LP-10	100 ns	
HM658512LP-12	120 ns	
HM658512LP-8L	80 ns	
HM658512LP-10L	100 ns	
HM658512LP-12L	120 ns	
HM658512DP-8	80 ns	
HM658512DP-10	100 ns	
HM658512DP-12	120 ns	
HM658512LFP-8	80 ns	32-pin plastic SOP (FP-32D)
HM658512LFP-10	100 ns	
HM658512LFP-12	120 ns	
HM658512LFP-8L	80 ns	
HM658512LFP-10L	100 ns	
HM658512LFP-12L	120 ns	
HM658512DFP-8	80 ns	
HM658512DFP-10	100 ns	
HM658512DFP-12	120 ns	
HM658512DTT-8	80 ns	8 mm × 20 mm 32-pin plastic TSOP (TTP-32D)
HM658512DTT-10	100 ns	
HM658512DTT-12	120 ns	
HM658512LTT-8	80 ns	
HM658512LTT-10	100 ns	
HM658512LTT-12	120 ns	
HM658512LTT-8L	80 ns	
HM658512LTT-10L	100 ns	
HM658512LTT-12L	120 ns	
HM658512DRR-8	80 ns	8 mm × 20 mm 32-pin plastic TSOP reverse type (TTP-32DR)
HM658512DRR-10	100 ns	
HM658512DRR-12	120 ns	
HM658512LRR-8	80 ns	
HM658512LRR-10	100 ns	
HM658512LRR-12	120 ns	
HM658512LRR-8L	80 ns	
HM658512LRR-10L	100 ns	
HM658512LRR-12L	120 ns	

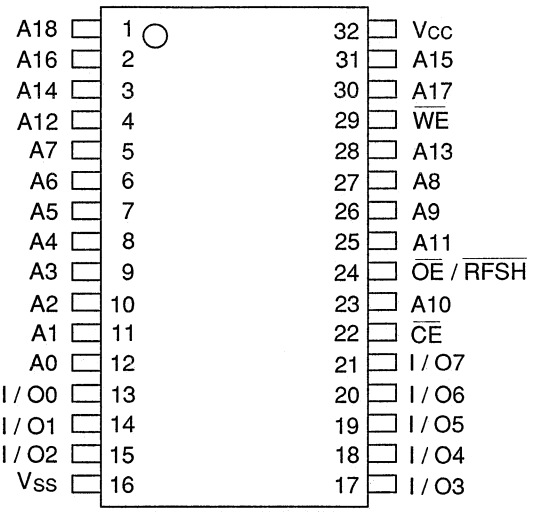
Pin Arrangement

HM658512P/FP Series



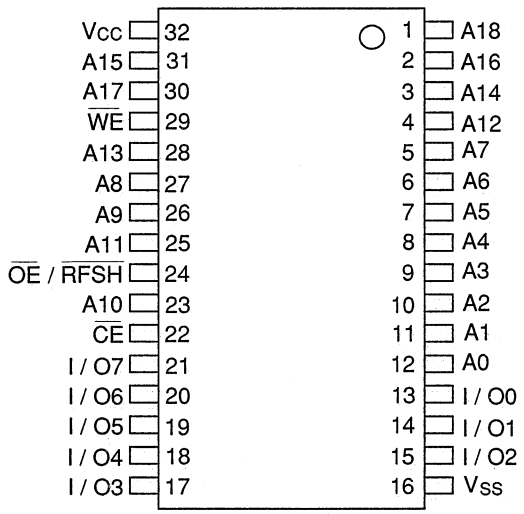
(Top View)

HM658512TT Series



(Top View)

HM658512RR



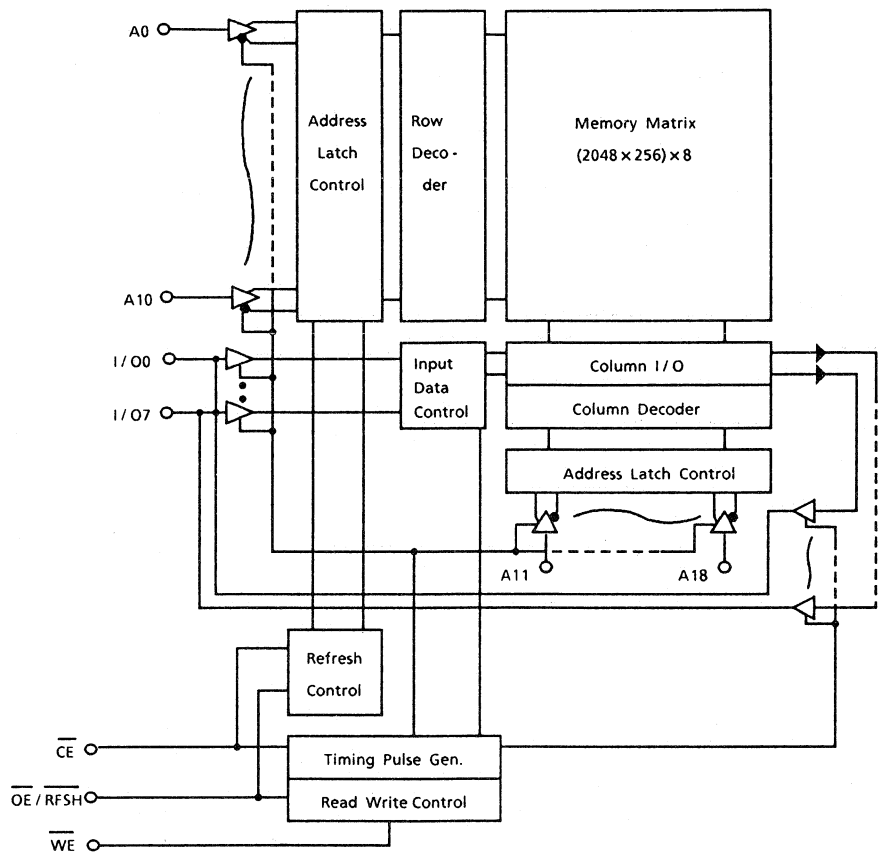
(Top View)

Pin Description

Pin name	Function
A0 – A18	Address
I/O0 – I/O7	Input/output
$\overline{CE}$	Chip enable
$\overline{OE}$/$\overline{RFSH}$	Output enable/refresh

Pin name	Function
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Function Table

$\overline{CE}$	$\overline{OE}$/$\overline{RFSH}$	$\overline{WE}$	I/O pin	Mode
L	L	H	Low-Z	Read
L	X	L	High-Z	Write
L	H	H	High-Z	—
H	L	X	High-Z	Refresh *2
H	H	X	High-Z	Standby

Notes: 1. X means don't care
2. Self refresh is guaranteed only for L-version and LL-version.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage with respect to V_{SS}	V_T	–1.0 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.4	—	6.0	V
	V_{IL}	–1.0 *1	—	0.8	V

Note: 1. V_{IL} min = –3.0 V for pulse width 30 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Operating power supply current	I_{CC1}	—	—	75	mA	$I_{I/O}$ = 0 tcyc = min
Standby power supply current	I_{SB1}	—	1	2	mA	$\overline{CE}$ = V_{IH}, Vin ≥ 0V $\overline{OE}$/$\overline{RFSH}$ = V_{IH}
	I_{SB2}	—	20 *1	200 *1	µA	$\overline{CE}$ ≥ V_{CC} – 0.2 V, Vin ≥ 0 V $\overline{OE}$/$\overline{RFSH}$ ≥ V_{CC} – 0.2 V
			20 *2	100 *2	µA	
Operating power supply current in self refresh mode	I_{CC2}	—	1 *1,2	2 *1,2	mA	$\overline{CE}$ = V_{IH} $\overline{OE}$/$\overline{RFSH}$ = V_{IL}, Vin ≥ 0 V
	I_{CC3}	—	70 *1	200 *1	µA	$\overline{CE}$ ≥ V_{CC} – 0.2 V $\overline{OE}$/$\overline{RFSH}$ ≤ 0.2 V
			40 *2	100 *2	µA	Vin ≥ 0 V
Input leakage current	I_{LI}	–10	—	10	µA	V_{CC} = 5.5 V Vin = V_{SS} to V_{CC}

Notes: 1. This characteristics is guaranteed only for L-version.
2. This characteristics is guaranteed only for LL-version.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%) (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Output leakage current	I_{LO}	–10	—	10	µA	$\overline{OE}/\overline{RFSH}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –1 mA

Capacitance

Item	Symbol	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

Test Conditions

Input pulse levels: 2.4 V, 0.4 V
Input rise and fall times: 5 ns
Timing measurement level: 2.2 V, 0.8 V
Reference level: V_{OH} = 2.0 V, V_{OL} = 0.8 V
Output load: 1 TTL and 100 pF

		HM658512–8		HM658512–10		HM658512–12			
Item	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	130	—	160	—	190	—	ns	
Chip enable access time	t_{CEA}	—	80	—	100	—	120	ns	
Read-modify-write cycle time	t_{RWC}	180	—	220	—	260	—	ns	
Output enable access time	t_{OEA}	—	30	—	40	—	50	ns	
Chip disable to output in high-Z	t_{CHZ}	0	25	0	25	0	30	ns	1
Chip enable to output in low-Z	t_{CLZ}	20	—	20	—	20	—	ns	2

AC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 10%) (cont)

Item	Symbol	HM658512–8		HM658512–10		HM658512–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Output disable to output in high-Z	t_{OHZ}	—	25	—	25	—	30	ns	1
Output enable to output in low-Z	t_{OLZ}	0	—	0	—	0	_	ns	2
Chip enable pulse width	t_{CE}	80 ns	10 µs	100 ns	10 µs	120 ns	10 µs		
Chip enable precharge time	t_P	40	—	50	—	60	—	ns	
Address setup time	t_{AS}	0	—	0	—	0	—	ns	
Address hold time	t_{AH}	20	—	25	—	30	—	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns	
Write command pulse width	t_{WP}	25	—	30	—	35	—	ns	
Chip enable to end of write	t_{CW}	80	—	100	—	120	—	ns	
Chip enable to output enable delay time	t_{OCD}	0	—	0	—	0	—	ns	
Output enable hold time	t_{OHC}	15	—	15	—	15	—	ns	
Data in to end of write	t_{DW}	20	—	25	—	30	—	ns	
Data in hold time for write	t_{DH}	0	—	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	5	—	ns	2
Write to output in high-Z	t_{WHZ}	—	20	—	25	—	30	ns	1
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	6
Refresh command delay time	t_{RFD}	40	—	50	—	60	—	ns	
Refresh precharge time	t_{FP}	40	—	40	—	40	—	ns	
Refresh command pulse width for automatic refresh	t_{FAP}	80 ns	8 µs	80 ns	8 µs	80 ns	8 µs		

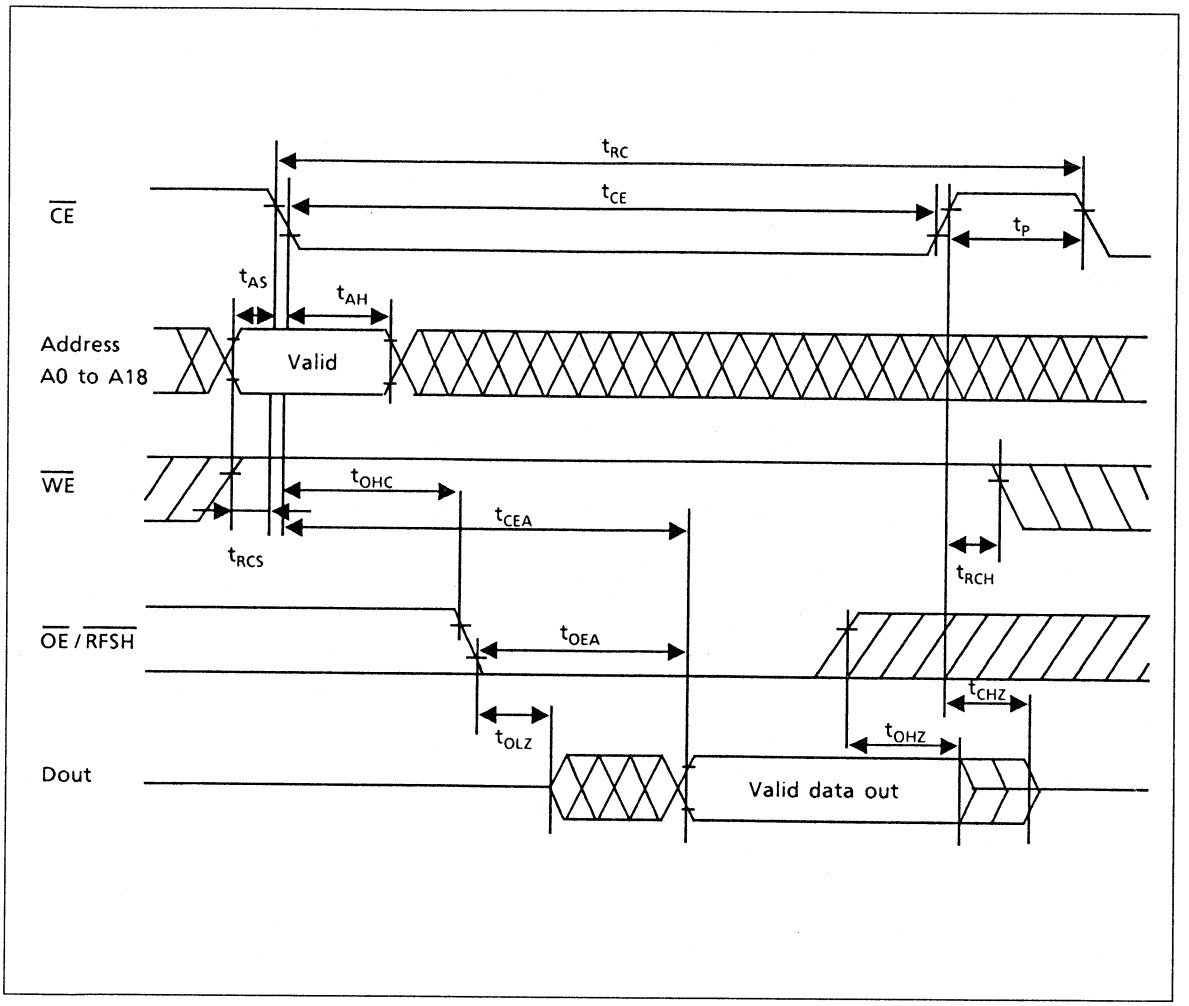
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%) (cont)

Item	Symbol	HM658512–8		HM658512–10		HM658512–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Automatic refresh cycle time	t_{FC}	130	—	160	—	190	—	ns	
Refresh command pulse width for self refresh	t_{FAS}*9	8	—	8	—	8	—	µs	
Refresh reset time from self refresh	t_{RFS}*9	600	—	600	_	600	—	ns	
Refresh period	t_{REF}	—	32	—	32	—	32	ms	2048 cycle

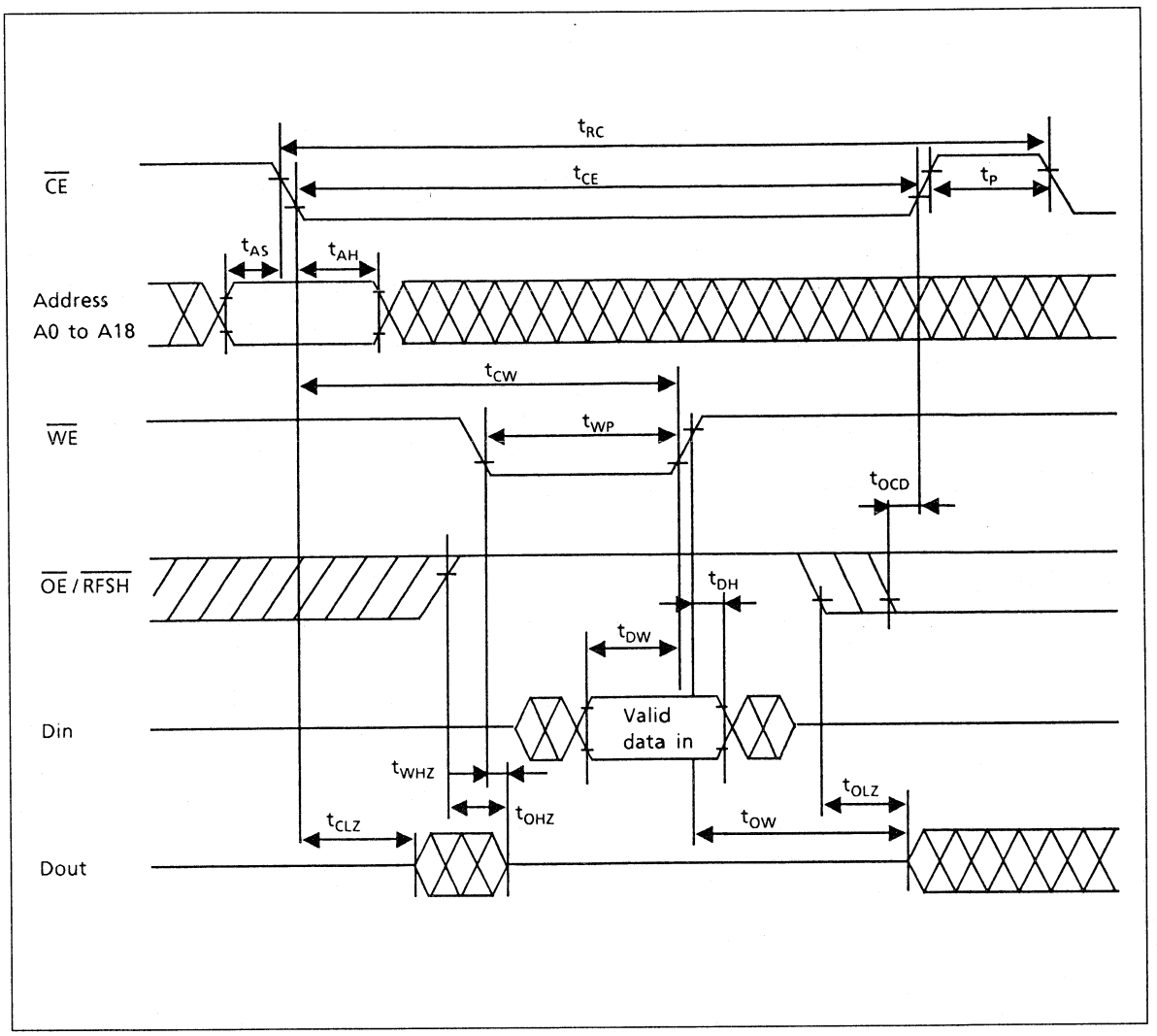
Notes:
1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit condition.
2. t_{CHZ}, t_{CLZ} t_{OHZ} t_{OLZ},t_{WHZ} and t_{OW}, are sampled under the condition of t_T = 5 ns and not 100% tested.
3. A write occurs during the overlap of low $\overline{CE}$ and low $\overline{WE}$.
4. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition, the output buffers remain in high impedance state.
5. In write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and at the end of write cycle data inputs must be floated prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
6. Transition time t_T is measured between V_{IH} min and V_{IL} max.
7. After power-up, pause for more than 100 µs and execute at least 8 initialization cycles.
8. 2048 cycles of burst refresh or the first cycle of distributed automatic refresh must be executed within 15µs after self refresh, in order to meet the refresh specification of 32 ms and 2048 cycles.
9. This characteristics is guaranteed only for L-version and LL-version.

Timing Waveforms

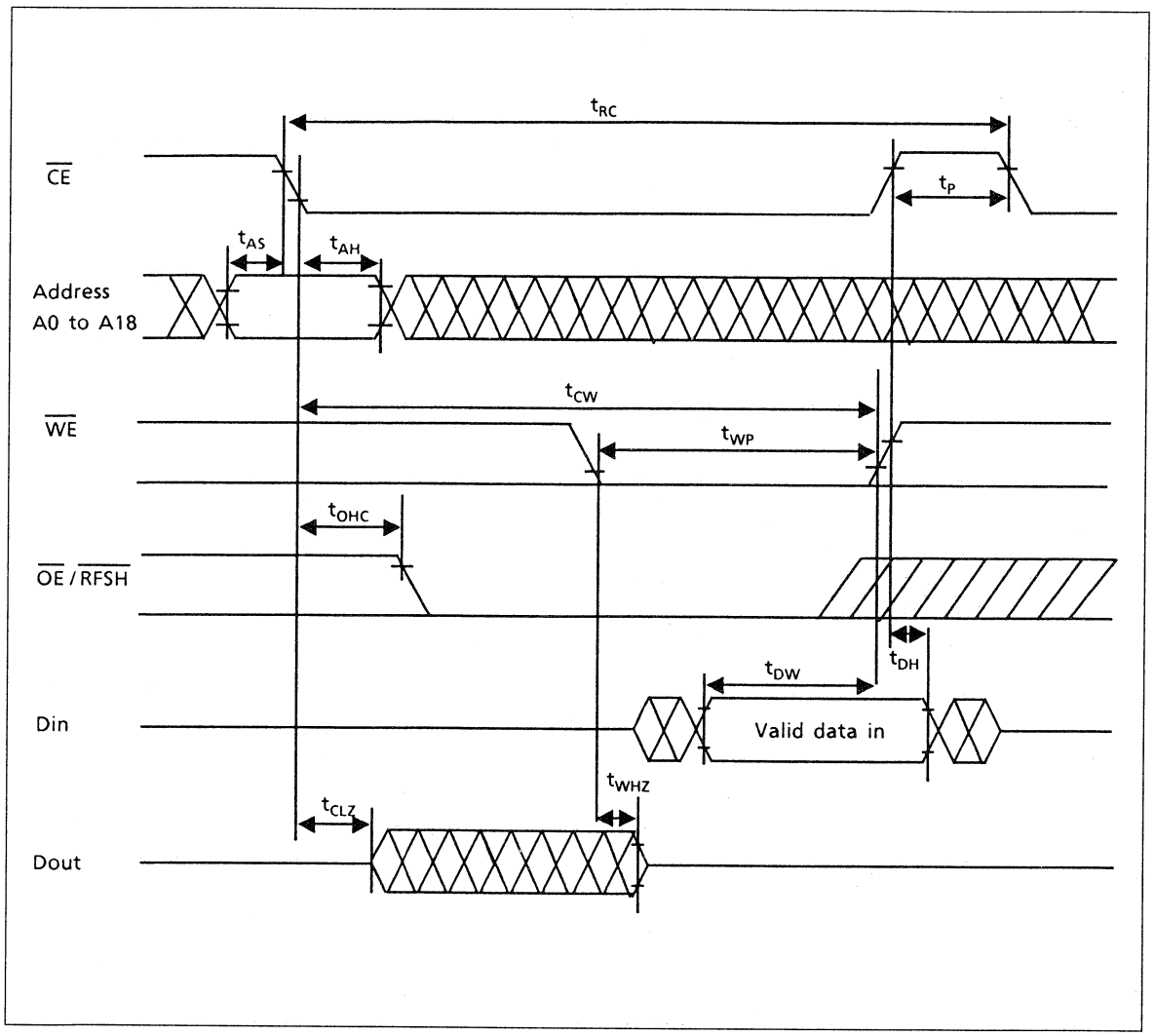
Read Cycle



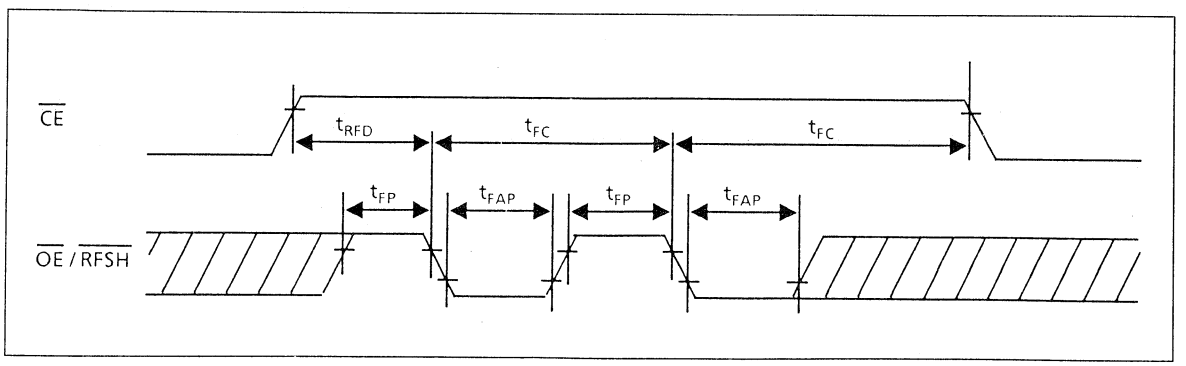
Write Cycle (1) ($\overline{OE}$ High)



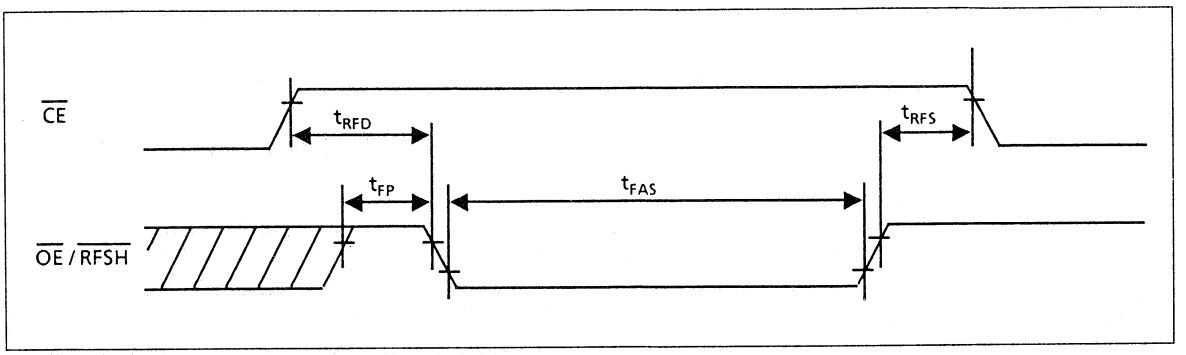
Write Cycle (2) ($\overline{OE}$ Low)



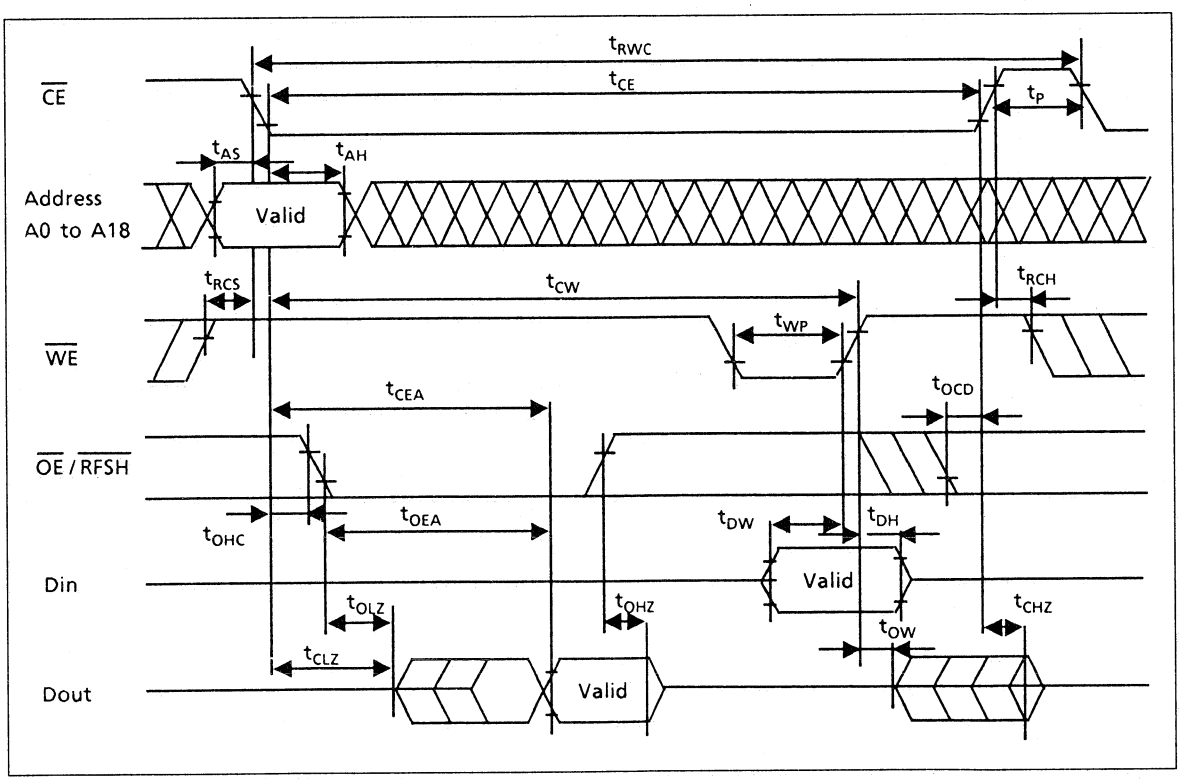
Automatic Refresh Cycle



Self Refresh Cycle



Read-Modify-Write Cycle



HM65V8512 Series

524288-Word × 8-Bit High Speed Pseudo Static RAM

HM65V8512 is a pseudo-static RAM organized as 524,288-word × 8-bit. HM65V8512 realized low power consumption by employing 0.8 μm CMOS process technology.
Power supply voltage is 3 V ±10% and all inputs and outputs are CMOS compatible. The low power version dissipates only 60 μW (typ) in self refresh mode, so it retains the data with battery.
The HM65V8512 is pin-compatible with 4-Mbit static RAM and with 4-Mbit 5 V operation Pseudo Static RAM.

Features

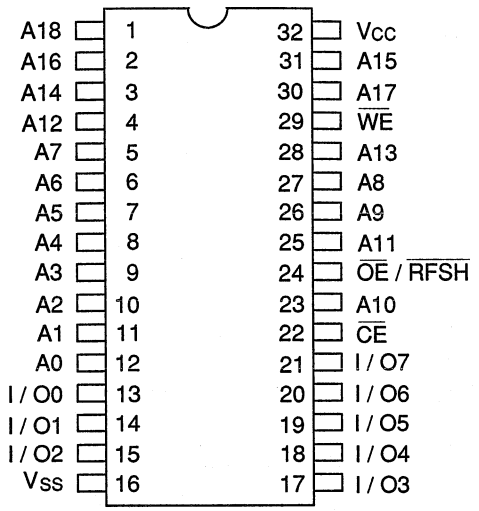
- Single 3 V (± 10%)
- High speed
  - Access time
    $\overline{CE}$ access time: 120 ns/150 ns (max)
  - Cycle time
    Random read/
    write cycle time: 190 ns/230 ns (min)
- Low power
  - 75 mW typ active
  - 60 μW typ standby
- All inputs and outputs CMOS compatible
- Package
  - 32-pin SOP package
  - 32-pin TSOP package
- Non multiplexed address
- 2048 refresh cycles (32 ms)
- Refresh functions:
  - L/LL-version: Address refresh
    Automatic refresh
    Self refresh
  - D-version: Address refresh
    Automatic refresh

Ordering Information

Type No.	Access time	Package
HM65V8512DFP-12	120 ns	32-pin plastic SOP (FP-32D)
HM65V8512DFP-15	150 ns	
HM65V8512LFP-12	120 ns	
HM65V8512LFP-15	150 ns	
HM65V8512LFP-12L	120 ns	
HM65V8512LFP-15L	150 ns	
HM65V8512DTT-12	120 ns	8 mm × 20 mm 32-pin plastic TSOP (TTP-32D)
HM65V8512DTT-15	150 ns	
HM65V8512LTT-12	120 ns	
HM65V8512LTT-15	150 ns	
HM65V8512LTT-12L	120 ns	
HM65V8512LTT-15L	150 ns	
HM65V8512DRR-12	120 ns	8 mm × 20 mm 32-pin plastic TSOP reverse type (TTP-32DR)
HM65V8512DRR-15	150 ns	
HM65V8512LRR-12	120 ns	
HM65V8512LRR-15	150 ns	
HM65V8512LRR-12L	120 ns	
HM65V8512LRR-15L	150 ns	

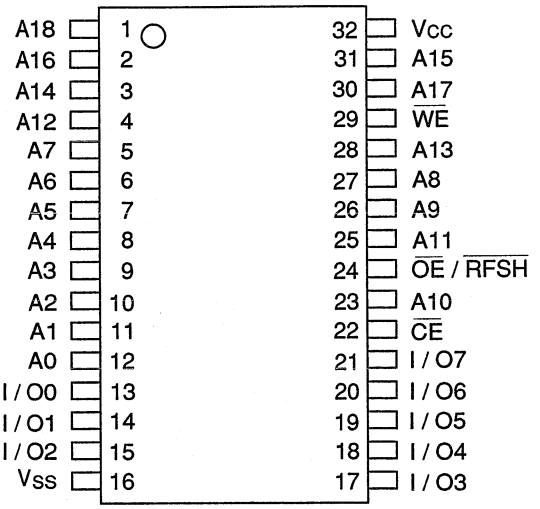
Pin Arrangement

HM65V8512FP Series



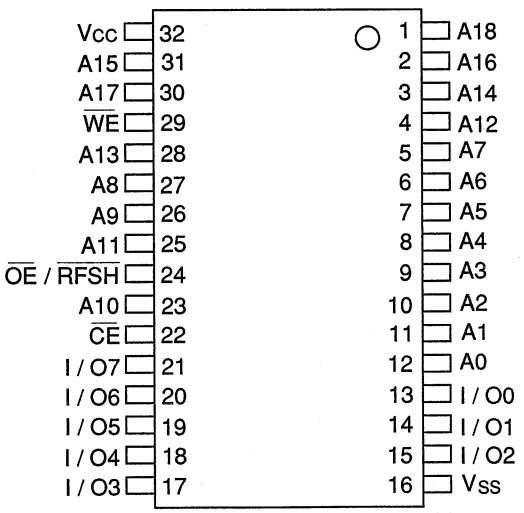
(Top View)

HM65V8512TT Series



(Top View)

HM65V8512RR Series



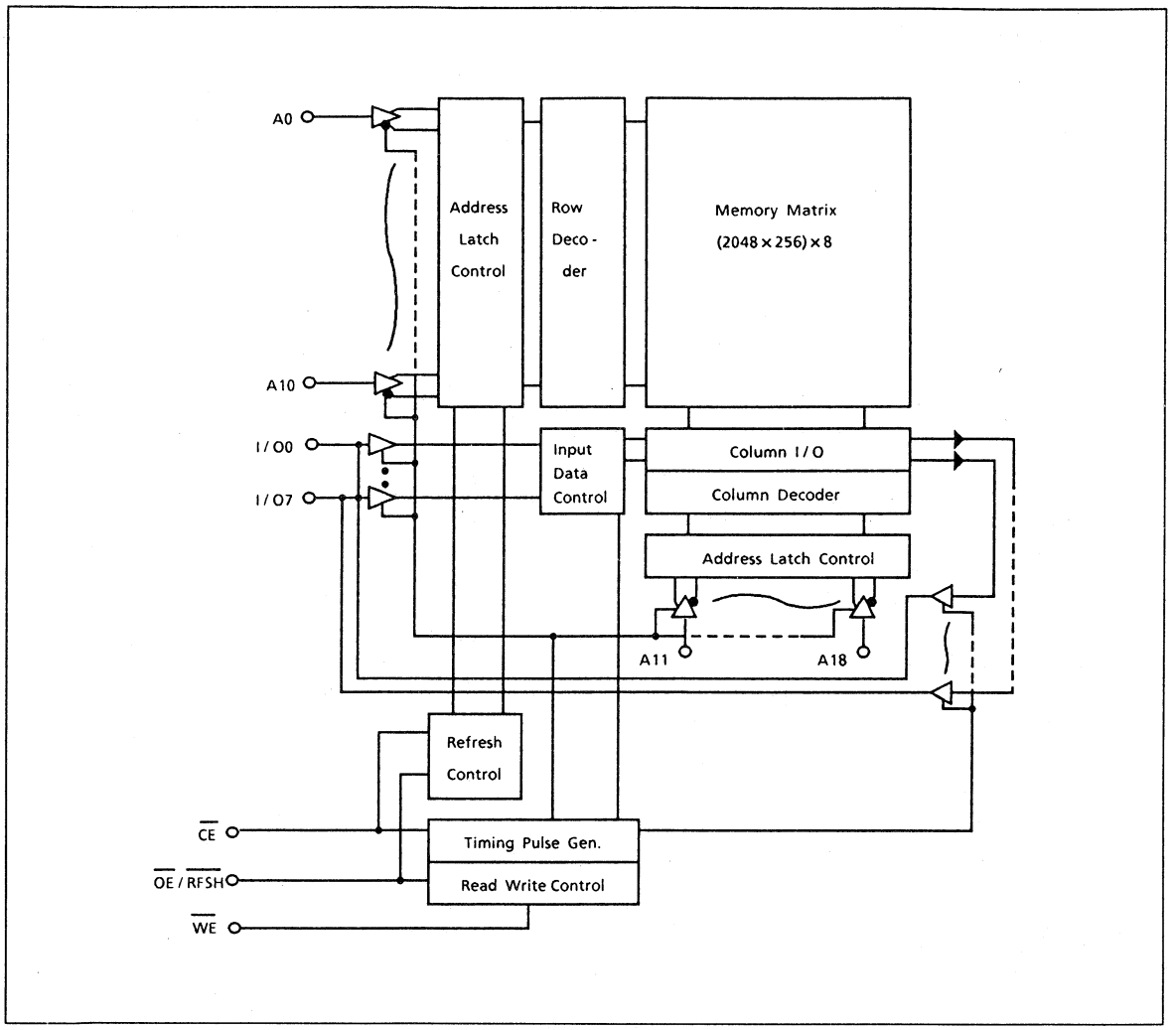
(Top View)

Pin Description

Pin name	Function
A0 – A18	Address
I/O0 – I/O7	Input/output
$\overline{CE}$	Chip enable
$\overline{OE}$/$\overline{RFSH}$	Output enable/refresh

Pin name	Function
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Function Table

$\overline{CE}$	$\overline{OE}$/$\overline{RFSH}$	$\overline{WE}$	I/O pin	Mode
L	L	H	Low-Z	Read
L	X	L	High-Z	Write
L	H	H	High-Z	—
H	L	X	High-Z	Refresh *2
H	H	X	High-Z	Standby

Notes: 1. X means don't care
2. Self refresh is guaranteed only for L-version and LL-version.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage with respect to V_{SS}	V_T	–0.5 to +6.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	3.3	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.1	—	6.0	V
	V_{IL}	–0.5 *1	—	0.7	V

Note: 1. V_{IL} min = –1.2 V for pulse width 30 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3 V ± 10%)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Operating power supply current	I_{CC1}	—	25	40	mA	$I_{I/O}$ = 0 tcyc = min
Standby power supply current	I_{SB1}	—	—	0.5	mA	$\overline{CE}$ = V_{IH}, Vin ≥ 0V $\overline{OE}$/$\overline{RFSH}$ = V_{IH}
	I_{SB2}	—	8	20	µA	$\overline{CE}$ ≥ V_{CC} – 0.2 V, Vin ≥ 0 V $\overline{OE}$/$\overline{RFSH}$ ≥ V_{CC} – 0.2 V
Operating power supply current in self refresh mode	I_{CC2}	—	—	0.5 *1,2	mA	$\overline{CE}$ = V_{IH} $\overline{OE}$/$\overline{RFSH}$ = V_{IL}, Vin ≥ 0 V
	I_{CC3}	—	20 *1	40 *1	µA	$\overline{CE}$ ≥ V_{CC} – 0.2 V $\overline{OE}$/$\overline{RFSH}$ ≤ 0.2 V
			15 *2	20 *2	µA	Vin ≥ 0 V
Input leakage current	I_{LI}	–1	—	1	µA	V_{CC} = 3.3 V Vin = V_{SS} to V_{CC}

Notes: 1. This characteristics is guaranteed only for L-version.
2. This characteristics is guaranteed only for LL-version.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3 V ± 10%) (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Output leakage current	I_{LO}	–1	—	1	µA	$\overline{OE}/\overline{RFSH}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Output voltage	V_{OL}	—	—	0.1	V	I_{OL} = 100 µA
	V_{OH}	2.6	—	—	V	I_{OH} = –100 µA

Capacitance

Item	Symbol	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3 V ± 10%)

Test Conditions

Input pulse levels: 2.4 V, 0.6 V
Input rise and fall times: 5 ns
Timing measurement level: 1.5 V
Reference level: V_{OH} = 2.1 V, V_{OL} = 0.9 V
Output load: 50 pF

		HM65V8512–12		HM65V8512–15			
Item	Symbol	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	190	—	230	—	ns	
Chip enable access time	t_{CEA}	—	120	—	150	ns	
Read-modify-write cycle time	t_{RWC}	250	—	290	—	ns	
Output enable access time	t_{OEA}	—	60	—	80	ns	
Chip disable to output in high-Z	t_{CHZ}	0	30	0	30	ns	1
Chip enable to output in low-Z	t_{CLZ}	20	—	20	—	ns	2
Output disable to output in high-Z	t_{OHZ}	—	30	—	30	ns	1
Output enable to output in low-Z	t_{OLZ}	0	—	0	_	ns	2

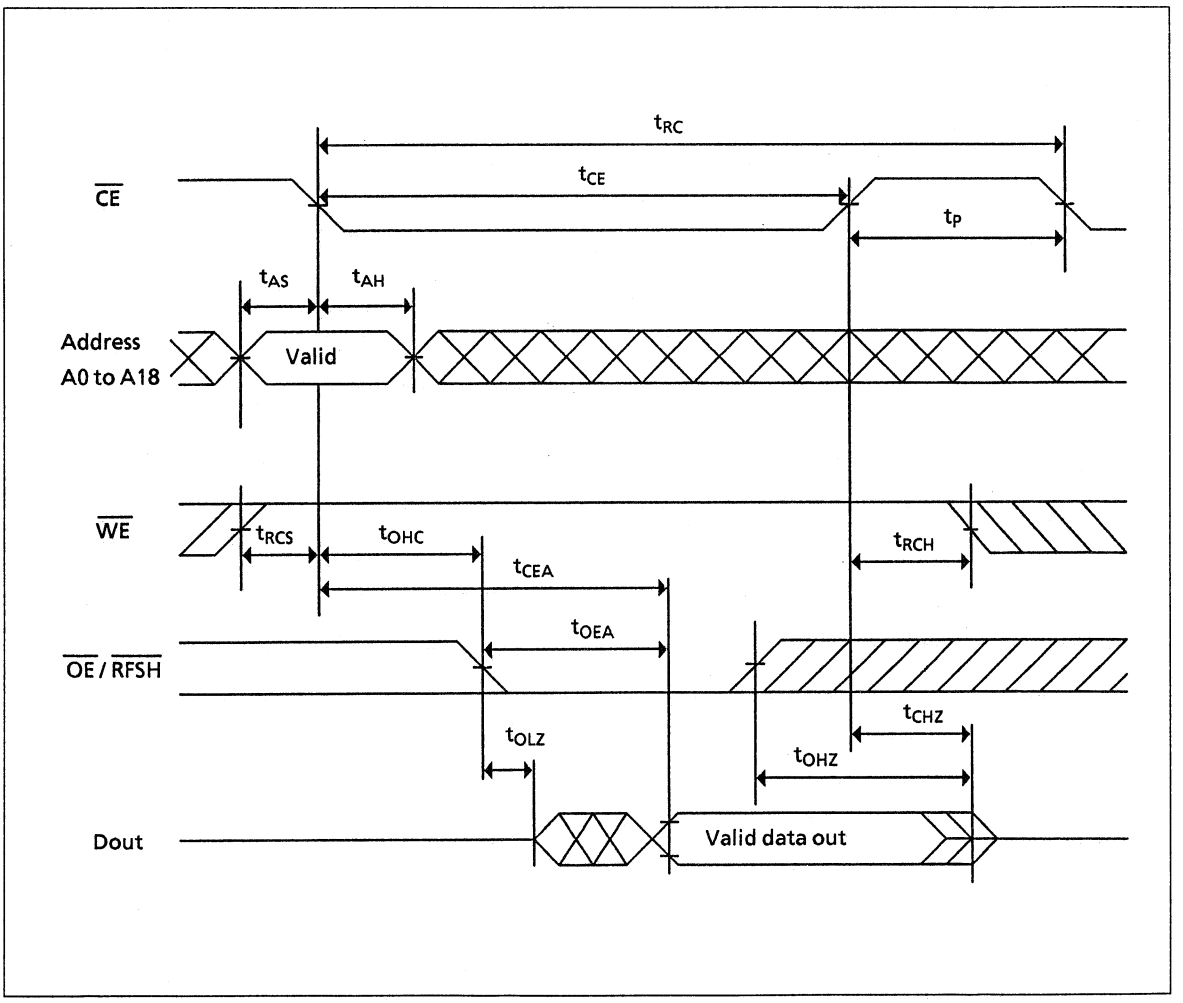
AC Characteristics (Ta = 0 to 70°C, V_{CC} = 3 V ± 10%) (cont)

Item	Symbol	HM65V8512-12 Min	HM65V8512-12 Max	HM65V8512-15 Min	HM65V8512-15 Max	Unit	Notes
Chip enable pulse width	t_{CE}	120 ns	10 µs	150 ns	10 µs		
Chip enable precharge time	t_P	70	—	80	—	ns	
Address setup time	t_{AS}	0	—	0	—	ns	
Address hold time	t_{AH}	30	—	30	—	ns	
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	ns	
Write command pulse width	t_{WP}	35	—	35	—	ns	
Chip enable to end of write	t_{CW}	120	—	150	—	ns	
Chip enable to output enable delay time	t_{OCD}	0	—	0	—	ns	
Output enable hold time	t_{OHC}	15	—	15	—	ns	
Data in to end of write	t_{DW}	30	—	30	—	ns	
Data in hold time for write	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	ns	2
Write to output in high-Z	t_{WHZ}	—	30	—	30	ns	1
Transition time (rise and fall)	t_T	3	50	3	50	ns	6
Refresh command delay time	t_{RFD}	70	—	80	—	ns	
Refresh precharge time	t_{FP}	40	—	40	—	ns	
Refresh command pulse width for automatic refresh	t_{FAP}	80 ns	8 µs	80 ns	8 µs		
Automatic refresh cycle time	t_{FC}	190	—	230	—	ns	
Refresh command pulse width for self refresh	t_{FAS}*9	8	—	8	—	µs	
Refresh reset time from self refresh	t_{RFS}*9	600	_	600	—	ns	
Refresh period	t_{REF}	—	32	—	32	ms	2048 cycle

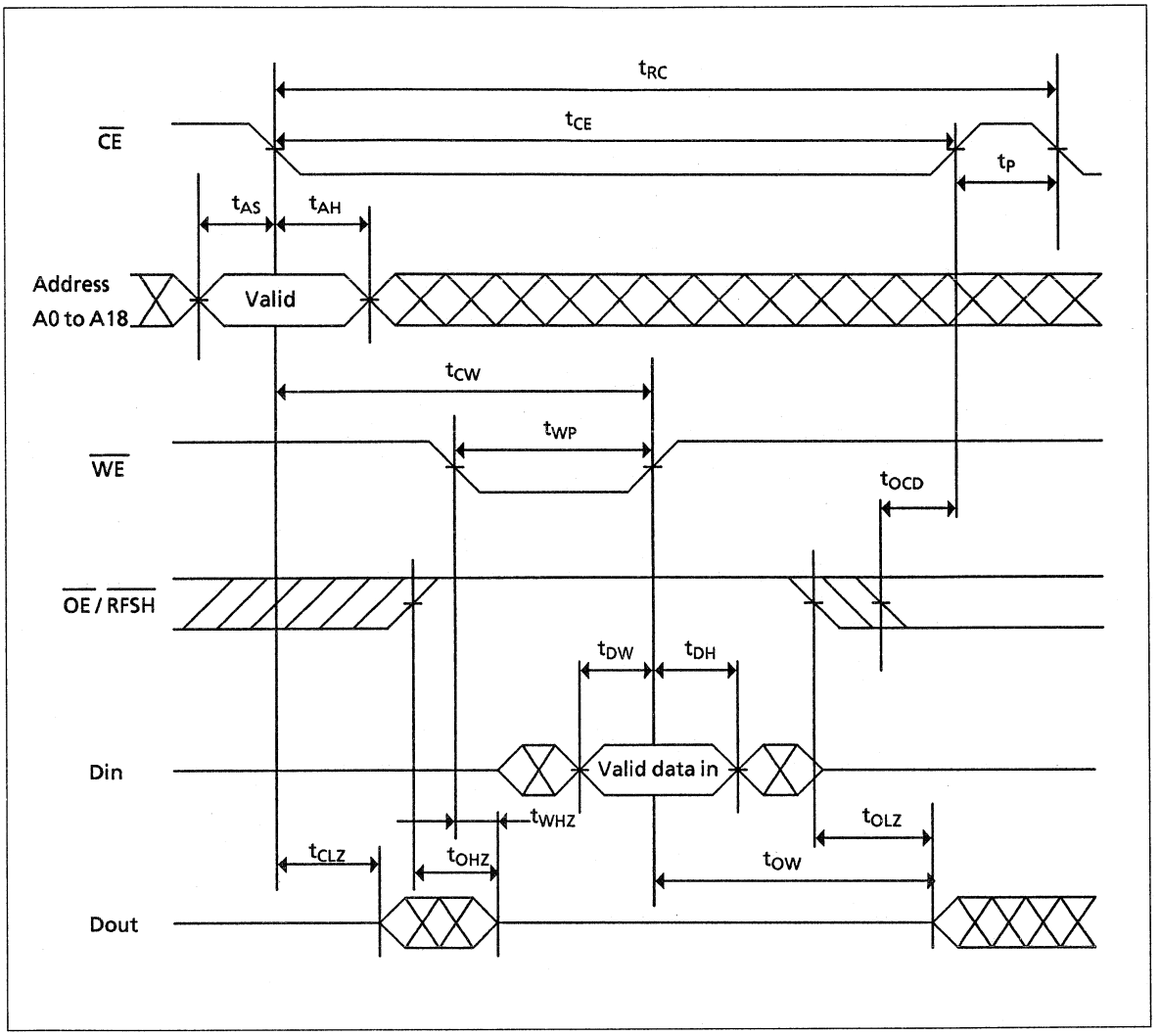
Notes:
1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit condition.
2. t_{CHZ}, t_{CLZ} t_{OHZ} t_{OLZ},t_{WHZ} and t_{OW}, are sampled under the condition of t_T = 5 ns and not 100% tested.
3. A write occurs during the overlap of low $\overline{CE}$ and low $\overline{WE}$.
4. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition, the output buffers remain in high impedance state.
5. In write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and at the end of write cycle data inputs must be floated prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
6. Transition time t_T is measured between V_{IH} min and V_{IL} max.
7. After power-up, pause for more than 100 µs and execute at least 8 initialization cycles.
8. 2048 cycles of burst refresh or the first cycle of distributed automatic refresh must be executed within 15µs after self refresh, in order to meet the refresh specification of 32 ms and 2048 cycles.
9. This characteristics is guaranteed only for L-version and LL-version.

Timing Waveforms

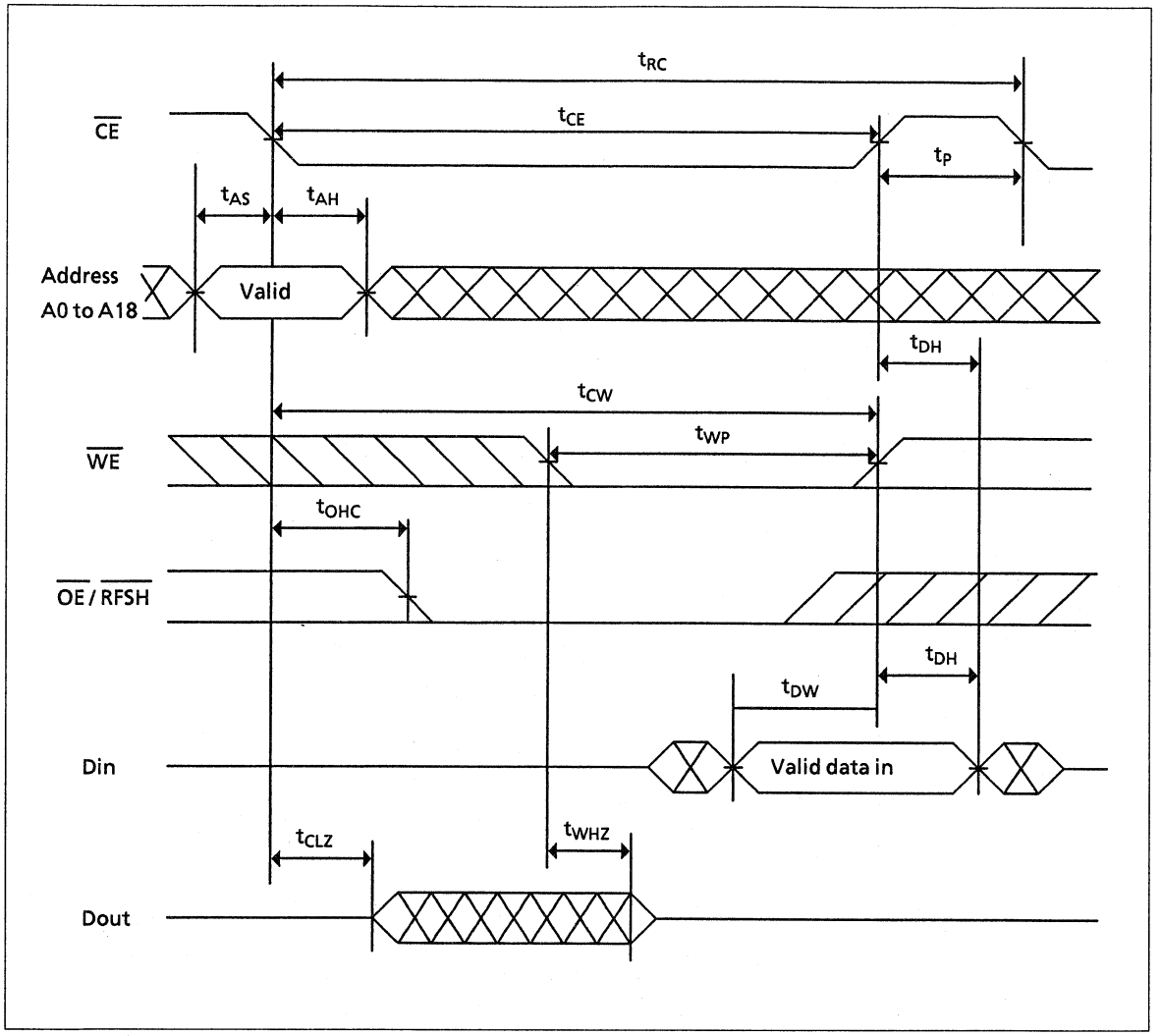
Read Cycle



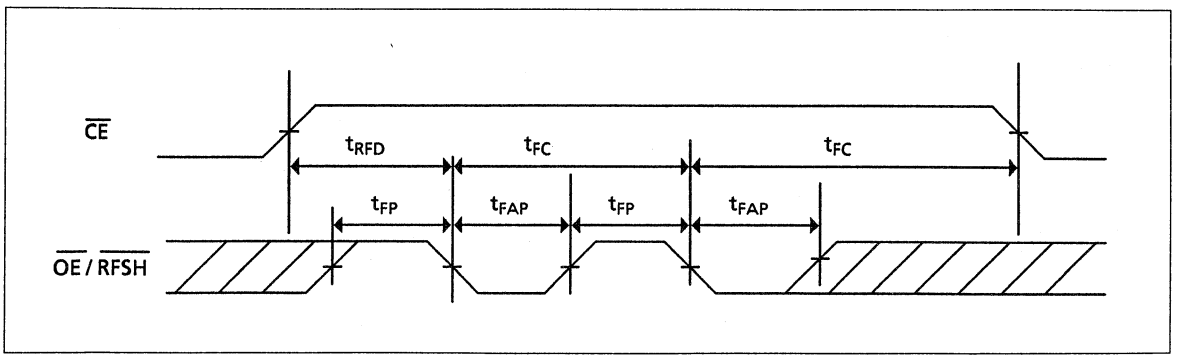
Write Cycle (1) ($\overline{OE}$ High)



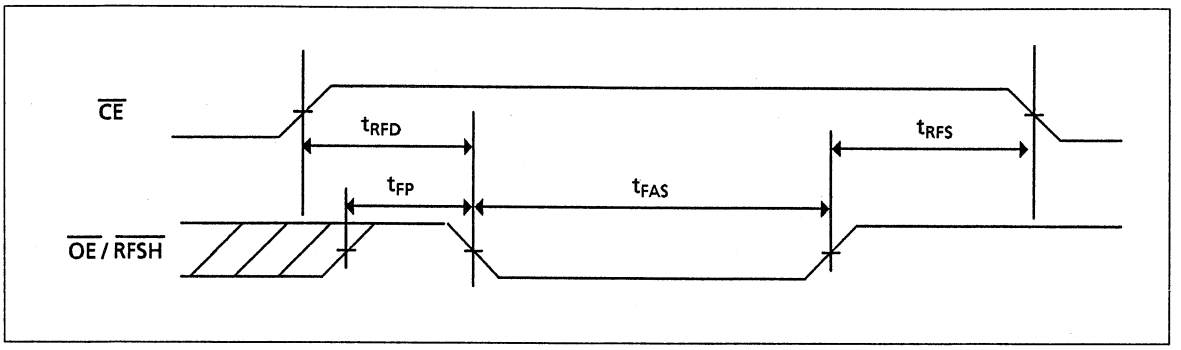
Write Cycle (2) ($\overline{OE}$ Low)



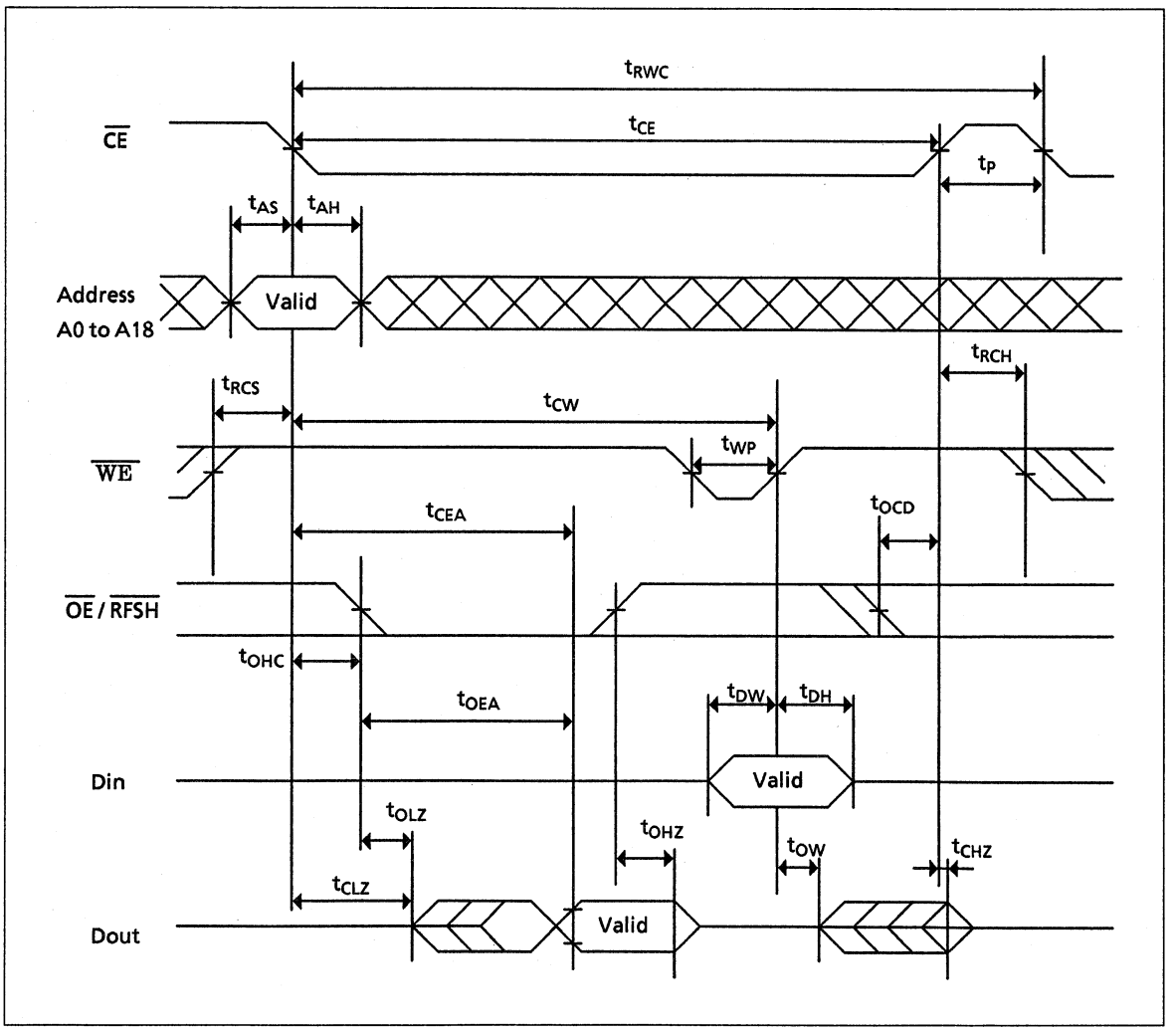
Automatic Refresh Cycle



Self Refresh Cycle



Read-Modify-Write Cycle



Application Specific Memory

HM63021 Series

2048-word x 8-bit Line Memory

HM63021 is a 2048-word x 8-bit static Serial Access Memory (SAM) with separate data inputs and outputs. Since it has an internal address counter, no external address signal is required and internal addresses are scanned serially. Using five different address scan modes, it is applicable to FIFO memories, double-speed conversions, 1H delay lines and 1H/2H delay lines for digital TV signals. Its minimum cycle times are 28 ns and 34 ns each corresponding to 8 fsc of PAL TV signals and NTSC TV signals. All inputs and outputs are TTL-compartiable.

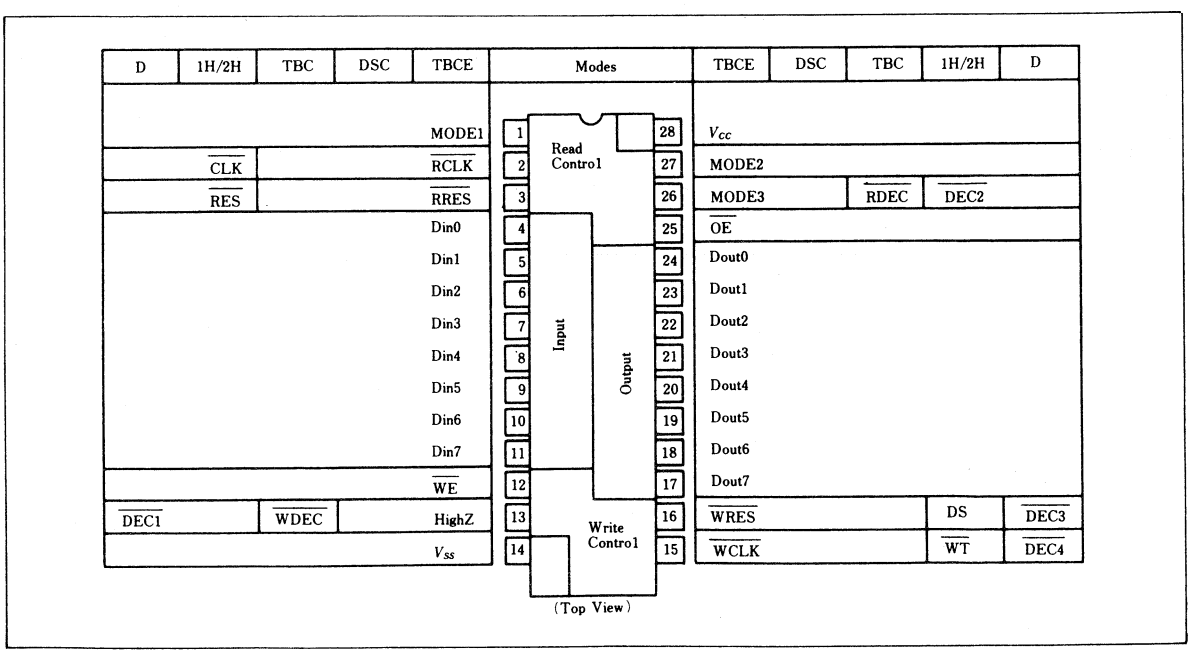
Features

- Five modes for various applications
- Corresponds to Digital TV system with 4 fsc sampling (PAL, NTSC)
- Decoder signal output pin; Fewer external circuits
- Asynchronous Read/Write operation;
  Separate address counters for Read/Write
  No Address Input required
- High Speed; Cycle Time 28/34/45 ns (min)
- Completely Static Memory; No refresh required
- 8-bit SAM with separate I/O
- Low Power; 250 mW typ. Active
- Single 5 V supply
- TTL compatible

Ordering Information

Type No.	Cycle Time	Package
HM63021P-28	28 ns	300-mil 28-pin Plastic DIP (DP-28N)
HM63021P-34	34 ns	
HM63021P-45	45 ns	
HM63021FP-28	28 ns	28-pin Plastic SOP (FP-28DA)
HM63021FP-34	34 ns	
HM63021FP-45	45 ns	

Pin Arrangement



Pin Description

Pin No.	Pin Name	Functions
1	MODE1	Mode Input 1 (All Modes)
2	$\overline{RCLK}/\overline{CLK}$	Read Clock Input (TBCE, DSC, TBC) Clock Input (1H/2H, D)
3	$\overline{RRES}/\overline{RES}$	Read Reset Input (TBCE, DSC, TBC) Reset Input (1H/2H, D)
4-11	Din 0 – Din 7	Data Inputs (All Modes)
12	$\overline{WE}$	Write Enable Input (All Modes)
13	High Z/$\overline{WDEC}/\overline{DEC1}$	High Impedance (TBCE, DSC) Write Decode Pulse Output (TBC) Decode Pulse Output 1 (1H/2H, D)
14	V_{SS}	Ground (All Modes)
15	$\overline{WCLK}/\overline{WT}/\overline{DEC4}$	Write Clock Input (TBCE, DSC, TBC) Write Timing Input (1H/2H) Decode Pulse Output 4 (D)
16	$\overline{WRES}$/DS/$\overline{DEC3}$	Write Reset Input (TBCE, DSC, TBC) Delay Select Input (1H/2H) Decode Pulse Output 3 (D)
17-24	Dout 0 – Dout 7	Data Outputs (All Modes)
25	$\overline{OE}$	Output Enable Input (All Modes)
26	MODE3/$\overline{RDEC}/\overline{DEC2}$	Mode Input 3 (TBCE) Read Decode Pulse Output (TBC) Decode Pulse Output 2 (1H/2H, D)
27	MODE2	Mode Input 2 (All Modes)
28	V_{CC}	Power Supply (+5V) (All Modes)

Mode Table

Mode Signals			Mode	Application Example
MODE1	MODE2	MODE3		
H	H	H	Time base compression/expansion (TBCE)	Picture in Picture
H	H	L	Double speed conversion (DSC)	Non interlace
H	L	– *1	Time base correction (TBC)	Time Base Corrector
L	H	– *1	1H/2H delay (1H/2H)	Vertical filter
L	L	– *1	Delay line (D)	Delay line

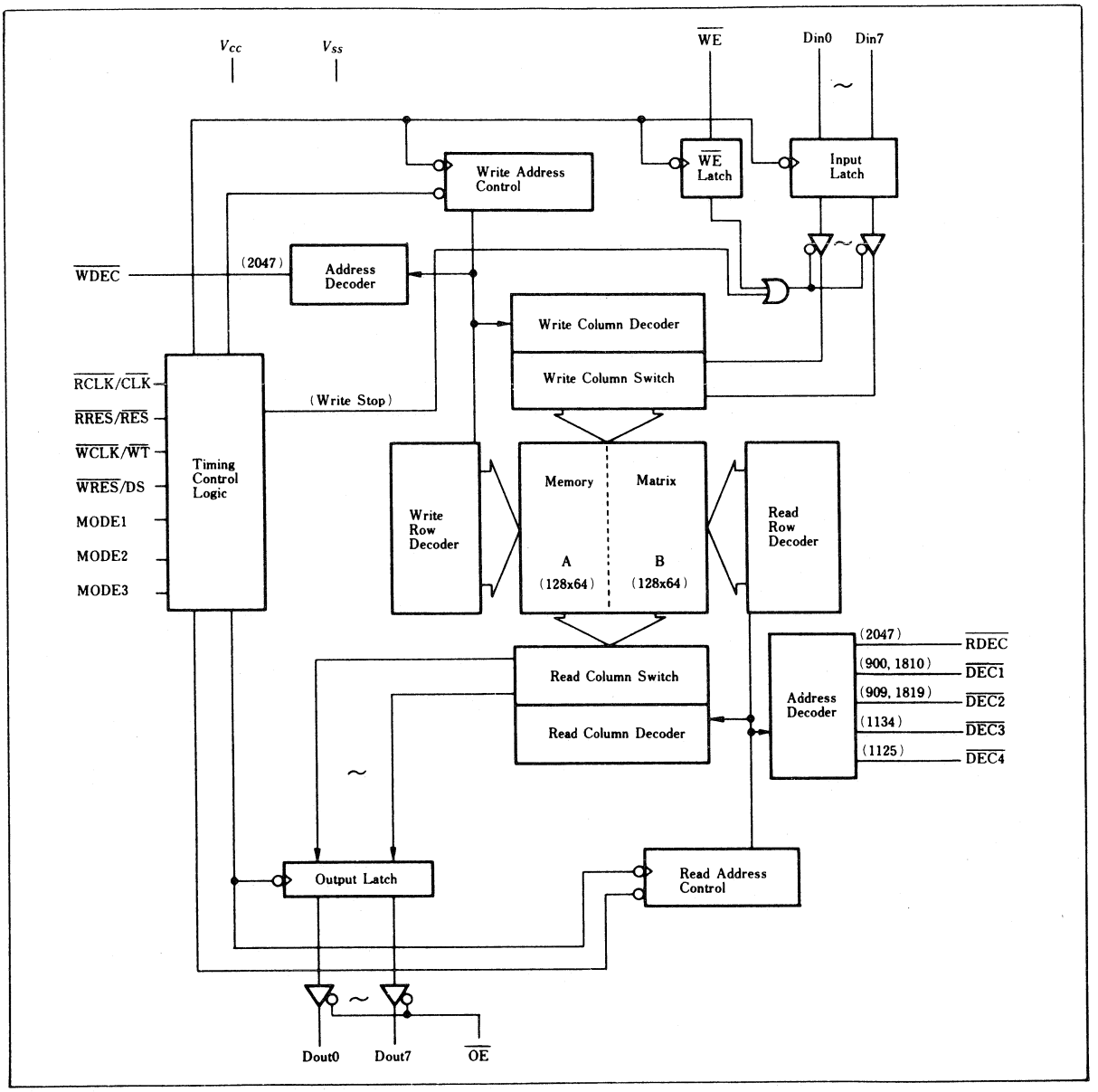
Note) *1. Decoder Output Signal ($\overline{RDEC}$, $\overline{DEC2}$)

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin relative to V_{SS}	V_T	−0.5 *1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	−55 to +125	°C
Storage Temperature under bias	Tbias	−10 to +85	°C

Note) *1. −3.5V for pulse width $\leqq$ 10 ns

Block Diagram



Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.4	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≤ 10 ns.

DC and Operating Characteristics ($Ta = 0$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$)

Parameter	Symbol	min	typ*1	max	Unit	Test Condition
Input Leakage Current	$\|I_{LI}\|$	–	–	10	μA	V_{CC} = 5.5 V Vin = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10	μA	$\overline{OE}$ = V_{IH} V_{out} = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	50	90	mA	Min. cycle, Iout*2 = 0 mA
Output Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8 mA*3, Dout 0 to Dout 7, $\overline{DEC}$ Output pin
	V_{OH}	2.4	–	–	V	I_{OH} = −4 mA, Dout 0 to Dout 7 pin
		2.4	–	–	V	I_{OH} = −1 mA, $\overline{DEC}$ Output pin

Notes) *1. Typical values are at V_{CC} = 5V, Ta = 25 °C and for reference only.
*2. Dout and $\overline{DEC}$
*3. I_{OL} = 6mA for 45ns version.

Capacitance ($Ta = 25°C, f = 1.0$ MHz)

Parameter	Symbol	min	typ	max	Unit	Conditions
Input Capacitance	Cin	–	–	6	pF	Vin = 0V
Output Capacitance*2	Cout	–	–	9	pF	Vout = 0V

Notes) *1. This parameter is sampled and not 100% tested.
*2. 13, 15 – 24, 26 pin

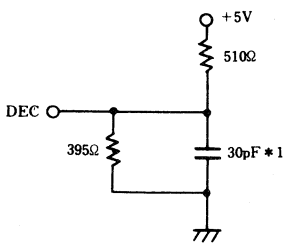
AC Characteristics ($V_{CC} = 5V \pm 10\%$, $Ta = 0$ to $+70°C$, unless otherwise noted.)

- AC Test Conditions

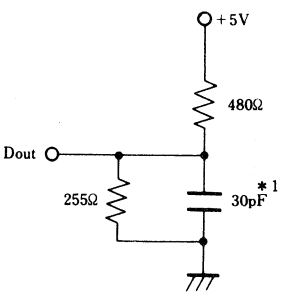
Input and Output timing reference levels: 1.5V
Input pulse levels: V_{SS} to 3V
Input rise and fall times: 5 ns

HM63021-28/34

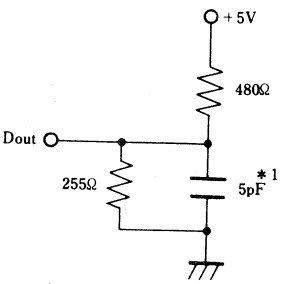
DEC Output Load



Dout Output Load (A)



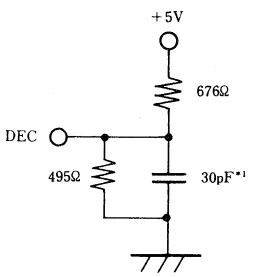
Dout Output Load (B) (t_{OLZ}, t_{OHZ})



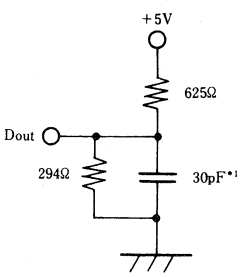
*1 Including scope and jig.

HM63021-45

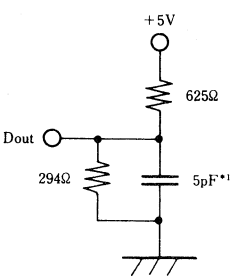
DEC Output Load



Dout Output Load (A)



Dout Output Load (B) (t_{OLZ}, t_{OHZ})



*1 Including scope and jig

Read Cycle

Parameter		Symbol	HM63021-28		HM63021-34		HM63021-45		Unit
			min	max	min	max	min	max	
Read Cycle Time		t_{RC}	28	–	34	–	45	–	ns
Read Clock Width		t_{RWL}	10	–	10	–	15	–	ns
		t_{RWH}	10	–	10	–	15	–	ns
Access Time		t_{AC}	–	20	–	25	–	30	ns
Decode Output Access Time	(fall)	t_{DA1}	–	20	–	25	–	30	ns
	(rise)	t_{DA2}	–	40	–	50	–	60	ns
Output Hold Time		t_{OH}	5	–	5	–	5	–	ns
Decode Output Hold Time	(fall)	t_{DOH1}	5	–	5	–	5	–	ns
	(rise)	t_{DOH2}	5	–	5	–	5	–	ns
Output Enable Access Time		t_{OE}	–	20	–	25	–	30	ns
Output Disable to Output in High Z		t_{OHZ}	0	15	0	20	0	25	ns
Output Enable to Output in Low Z		t_{OLZ}	5	–	5	–	5	–	ns

Write Cycle

Parameter	Symbol	HM63021-28		HM63021-34		HM63021-45		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	28	–	34	–	45	–	ns
	t_{WC}(1H/2H Mode)	56	–	68	–	90	–	ns
Write Clock Width	t_{WWL}	10	–	10	–	15	–	ns
	t_{WWH}	10	–	10	–	15	–	ns
Input Data Setup Time	t_{DS}	5	–	5	–	7	–	ns
Input Data Hold Time	t_{DH}	5	–	5	–	7	–	ns
$\overline{WE}$ Setup Time	t_{WESL}	5	–	5	–	7	–	ns
	t_{WESH}	5	–	5	–	7	–	ns
$\overline{WE}$ Hold Time	t_{WEHL}	5	–	5	–	7	–	ns
	t_{WEHH}	5	–	5	–	7	–	ns
$\overline{WT}$ Setup Time	t_{WTSL}	5	–	5	–	7	–	ns
	t_{WTSH}	5	–	5	–	7	–	ns
$\overline{WT}$ Hold Time	t_{WTHL}	5	–	5	–	7	–	ns
	t_{WTHH}	5	–	5	–	7	–	ns

Reset Cycle

Parameter	Symbol	HM63021-28		HM63021-34		HM63021-45		Unit
		min	max	min	max	min	max	
Reset Setup Time	t_{RES}	8	–	9	–	10	–	ns
Reset Hold Time	t_{REH}	5	–	5	–	7	–	ns
Clock Setup Time Before Reset	t_{REPS}	8	–	9	–	10	–	ns
Clock Hold Time Before Reset	t_{REPH}	5	–	5	–	7	–	ns

Mode Description

- Time Base Compression/Expansion Mode
  This mode turns HM63021 into a 2048-word x 8-bit FIFO memory with asynchronous input/output. The HM63021 provides 2 clocks ($\overline{RCLK}$, $\overline{WCLK}$) and 2 resets ($\overline{RRES}$, $\overline{WRES}$), one each for read and write. The internal address counters increment by 1 address clock and are reset to address 0. A write-inhibit function of HM63021 stops writing automatically after the data has been written into all addresses 0 to 2047. The write-inhibit function is released by reset using $\overline{WRES}$, and the HM63021 restarts writing into address 0.
- Double-Speed Conversion Mode
  This mode turns HM63021 into a 1024-word x

8-bit x 2 memory with asynchronous input/output. It is used for generating non-interlaced TV signals. When the original signal and the interpolated signal (1 field delay) of interlaced signals are input to the HM63021, multiplexed per dot, it outputs non-interlaced signals for each line. 8 fsc should be input to $\overline{RCLK}$ and $\overline{WCLK}$. A standard H synchronizing signal and a non-interlace H synchronizing signal are input to $\overline{WRES}$ and $\overline{RRES}$ respectively. A write-inhibit function is provided in this mode, making it applicable to PAL TV, where extra data (1135-1024 = 111 bits) is ignored.

- TBC Mode
  This mode turns HM63021 into 2048-word x 8-bit FIFO memory with asynchronous input/output. The HM63021 provides 2 clocks ($\overline{RCLK}$, $\overline{WCLK}$) and 2 resets ($\overline{RRES}$, $\overline{WRES}$), one each for read and write. The internal address counters increment by 1 address at each clock and are reset to address 0. The internal address counters return to address 0 after they reach address 2047. The HM63021 outputs a write decode pulse from $\overline{WDEC}$, synchronizing it with address 2047 in the write address counter, and read a decode pulse from $\overline{RDEC}$, synchronizing with address 2047 in the read address counter. Using these pulses, the memory area can be extended easily (multiple-HM63021s can be used with ease).

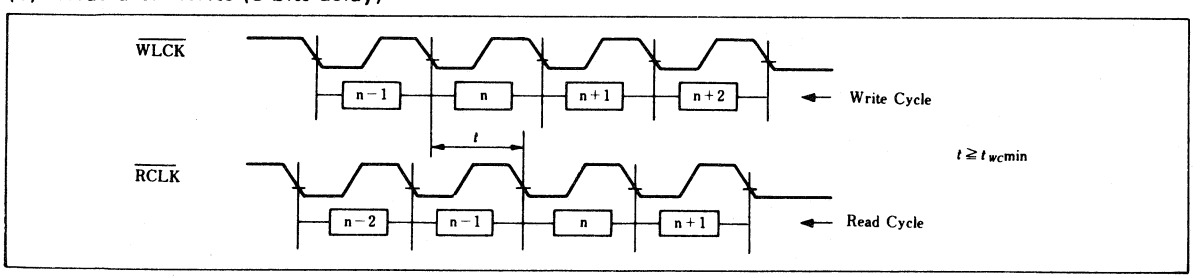
- 1H/2H Delay Mode
  This mode turns HM63021 into a 1024-word x 8-bit x 2 delay line with synchronous input/output. Delay time is defined by the reset period of $\overline{RES}$. Since the HM63021 outputs a 901 decode pulse ($\overline{DEC1}$) and a 910 decode pulse ($\overline{DEC2}$), connecting $\overline{DEC2}$ to $\overline{RES}$, for example, outputs 1H- and 2H- delayed signals alternately at a 8- fsc cycle when the original signal is input at a 4- fsc cycle. A write-inhibit function is provided in this mode, making it applicable to PAL TV, where extra data (1135-1024 = 111 bits) is ignored.

- Delay Line Mode
  This mode turns HM63021 into a 2048-word x 8-bit delay line with synchronous input/output. Delay time (3 to 2048 bits) is defined by the reset period of $\overline{RES}$. The delay is 2048 bits when $\overline{RES}$ is fixed High. Signals delayed by 910 bits to 1135 bits for example, can be easily obtained without external circuits by just connecting selected decoded pulses on $\overline{DEC1}$ – $\overline{DEC4}$ to $\overline{RES}$.

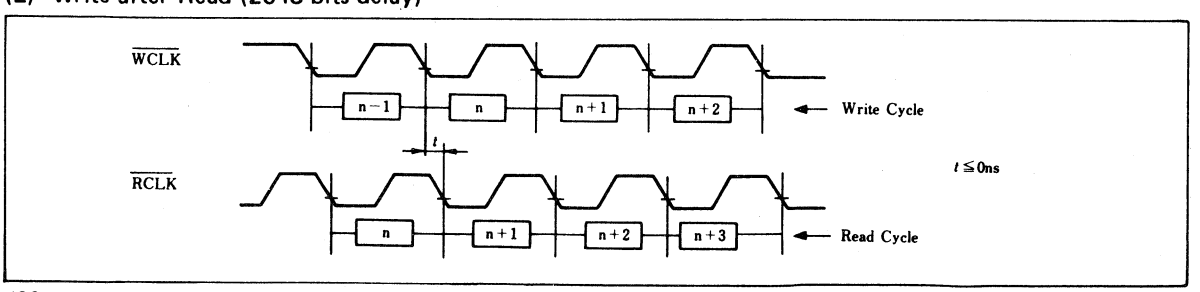
Notes on Using HM63021

- Hitachi recommends that pin 13 (high impedance) should be fixed by pulling up or down with a resistor (of several kΩ) in TBC or DSC mode.
- Hitachi recommends that the mode signal input pins and DS pin should be fixed by pulling them up or down with a resistor (of several kΩ).
- Data integrity cannot be guaranteed when mode or DS is changed during operation
- When a read address coincides with a write address in TBCE, TBC or DSC mode, the data is written correctly but it is not always read correctly.

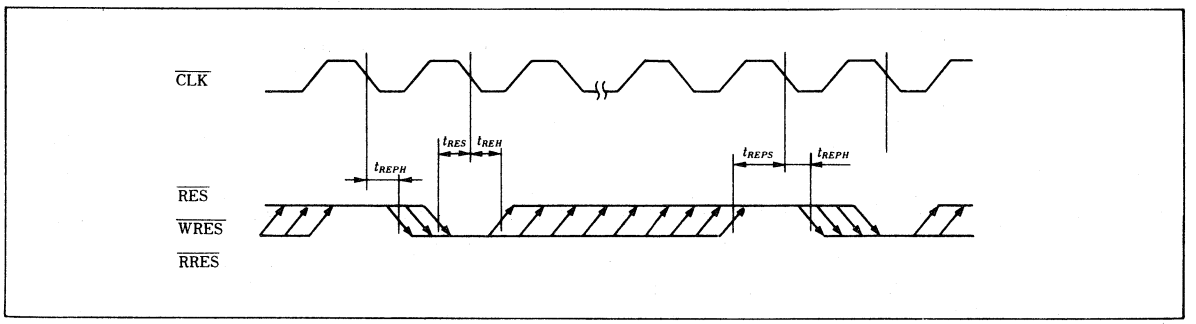
(1) Read after Write (3 bits delay)



(2) Write after Read (2048 bits delay)

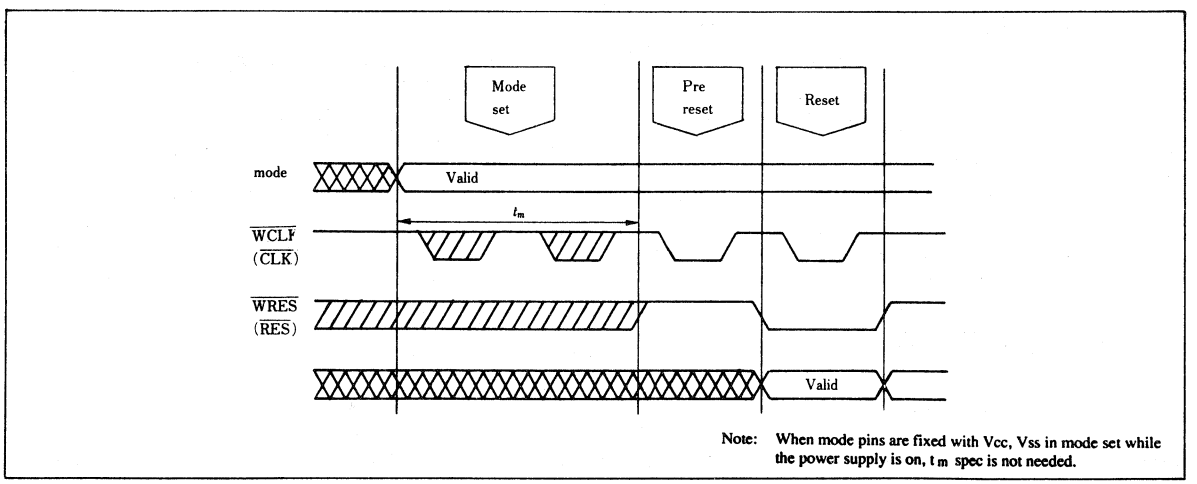


- At power on, the output of the address counter is not defined. Therefore, operations before the system is reset cannot be guaranteed, and decode signal output is not defined until after the first reset cycle.
- The decode signal is latched by a decode output latch circuit at the previous address of the internal counter address and is output synchronized with the next address. For example, $\overline{WDEC}$ in TBC mode is latched at write address 2046 and is output at write address 2047. If a write reset is performed on address 2047 at this time, the write address becomes 0 and $\overline{WDEC}$ is output.
  The same operation is performed in other modes.
- In the reset cycle, the input levels of $\overline{WRES}$, $\overline{RRES}$, $\overline{RES}$ are raised to satisfy t_{REH}, and are fixed high until t_{REPH} in the next pre-reset cycle is satisfied. The rise timings of the reset signals ($\overline{RES}$, $\overline{WRES}$, $\overline{RRES}$) are optionals provided that the t_{REPS} specification is satisfied. The timings at which $\overline{RES}$, $\overline{WRES}$, and $\overline{RRES}$ fall after pre-reset are also optional, provided that the t_{REPH} and t_{RES} specifications are satisfied.



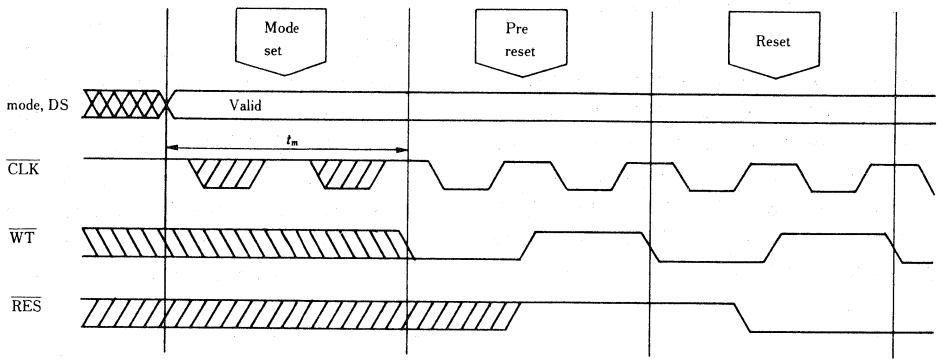
- Hitachi recommends that t_m (time between mode set and the first cycle (Pre-reset)) should be kept for 2 cycle time (56ns / 68ns / 90ns) or more while the power supply is on.

(1) TBCE, TBC, DSC and Delay Line Mode



Note: When mode pins are fixed with Vcc, Vss in mode set while the power supply is on, t_m spec is not needed.

(2) 1H / 2H Delay Mode



Note : When mode pins are fixed with *Vcc*, *Vss* in mode set while the power supply is on, *tm* spec is not needed.

Decode Signal

When internal address counter reaches the specified address as shown below, decode outputs become low.

Mode	Pin No.	Pin Name	Internal Address counter	Timing of the Output Signal	Operation
TBC	13	$\overline{\text{WDEC}}$	Write 2047	After Write 2047	Completion of Writing on all bits is detected.
	26	$\overline{\text{RDEC}}$	Read 2047	Output of 2046	Completion of Reading from all bits is detected.
1H/2H	13	$\overline{\text{DEC1}}$	Read 900 (2H)	Output of 900 (1H)	By inputting this signal to pin #3, 901/1802-bit delay output is obtained.
	26	$\overline{\text{DEC2}}$	Read 909 (2H)	Output of 909 (1H)	By inputting this signal to pin #3, 910/1820-bit delay output is obtained.
Delay line	13	$\overline{\text{DEC1}}$	Read 900	Output of 899	By inputting this signal to pin #3, 901-bit delay output is obtained.
			Read 1810	Output of 1809	By inputting this signal to pin #3 after the frequency of $\overline{\text{DEC1}}$ is devided into two, 1811-bit delay output is obtained.
	26	$\overline{\text{DEC2}}$	Read 909	Output of 908	By inputting this signal to pin #3, 910-bit delay output is obtained.
			Read 1819	Output of 1818	By inputting this signal to pin #3 after the frequency of $\overline{\text{DEC2}}$ is devided into two, 1820-bit delay output is obtained.
	16	$\overline{\text{DEC3}}$	Read 1134	Output of 1133	By inputting this signal to pin #3, 1135-bit delay output is obtained.
	15	$\overline{\text{DEC4}}$	Read 1125	Output of 1124	By inputting this signal to pin #3, 1126-bit delay output is obtained.

Note) When counter is reset by Reset Signal ($\overline{\text{RRES}}$, $\overline{\text{RES}}$, $\overline{\text{WRES}}$), address becomes 0.

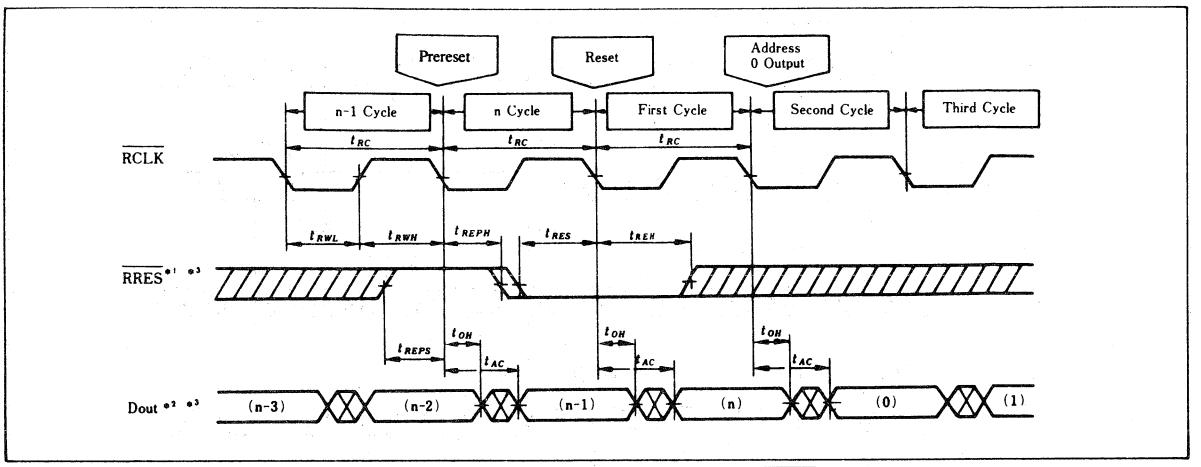
Write-inhibit Function

When internal address counter is as follows, writing is inhibited automatically for the next cycle. The write-inhibit function is cancelled by reset through $\overline{\text{WRES}}$ or $\overline{\text{RES}}$.

Mode	Write-inhibit Function (internal counter address)
TBCE	Write-inhibit after address 2047
DSC	Write-inhibit after address 1023 x 2
TBC	No function
1H/2H	Write-inhibit after address 1023
D	No function

Note) When address counter is reset by $\overline{\text{WRES}}$ or $\overline{\text{RES}}$, address becomes 0.

Read Reset Cycle (TBCE, TBC Modes)

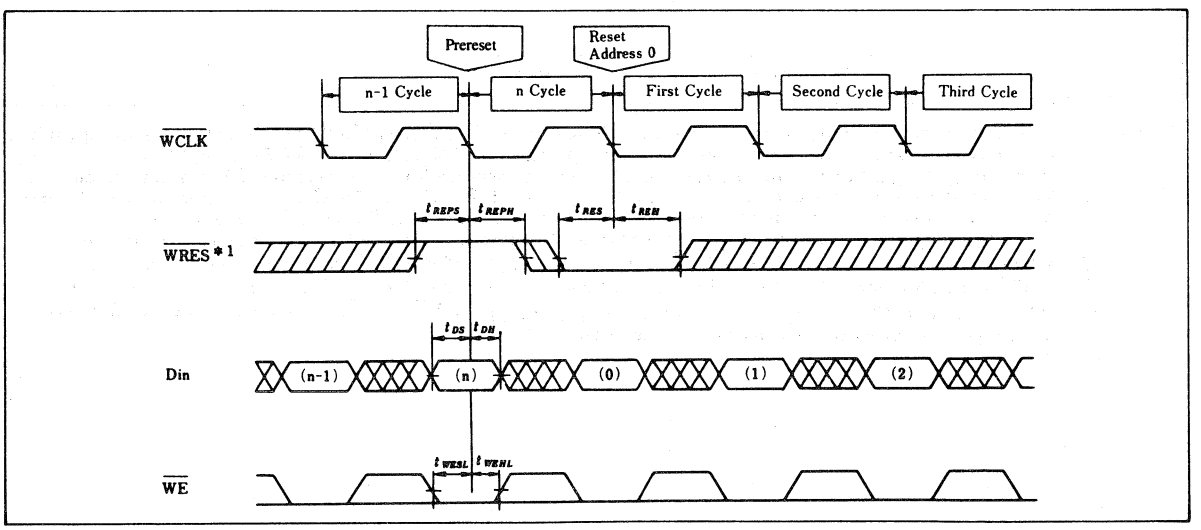


Notes) *1. The read address counter is reset at the first falling edge of $\overline{RCLK}$ after $\overline{RRES}$ falls, meeting the specifications of t_{REPS}, and t_{REPH}, and it is not reset at the next falling edge of $\overline{RCLK}$ even if $\overline{RRES}$ is kept low. When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meeet the specifications, the reset operation is not guaranteed. In reset operation, both prereset and reset are required.

*2. Output is from the read address of the previous cycle.

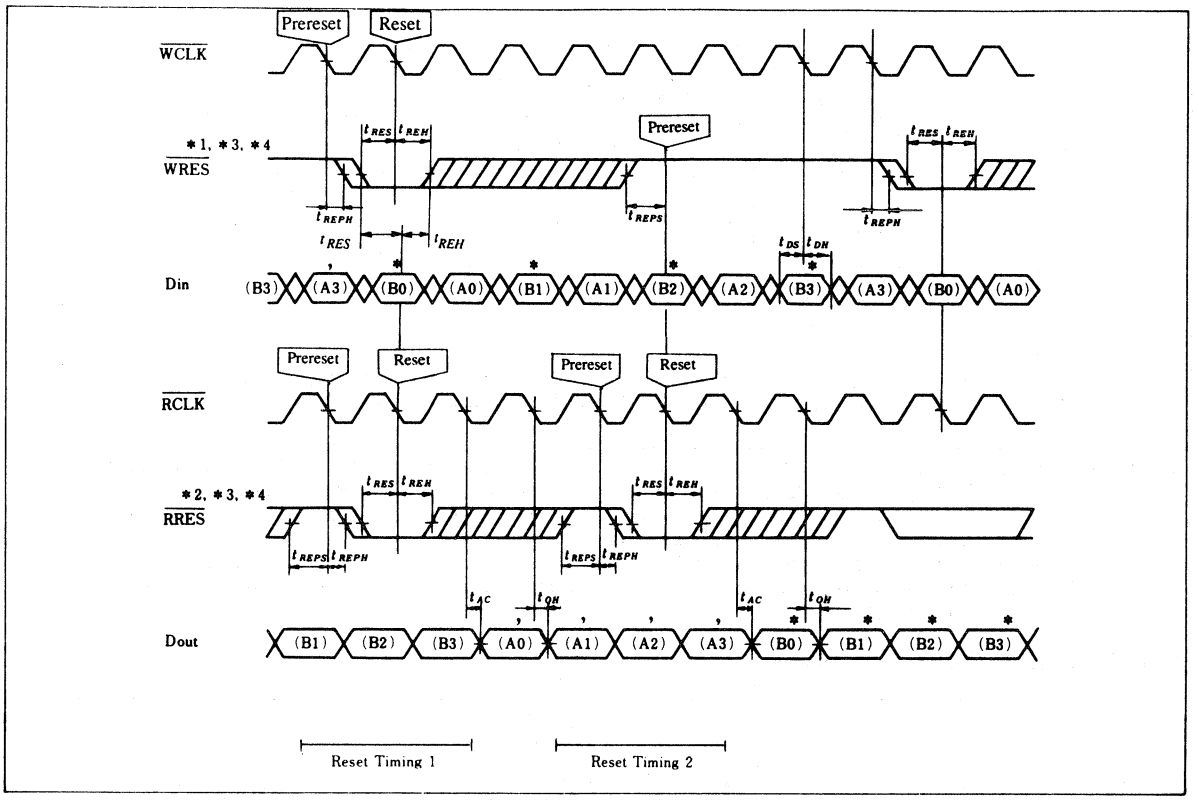
*3. When $\overline{RRES}$ is fixed high, the data at the read address counter is reset after the data of address 2047 is output, and the same operation restarts.

Write Reset Cycle (TBCE, TBC Modes)



Note) The write address counter is reset at the first falling edge of $\overline{WCLK}$ after $\overline{WRES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{WCLK}$ even if $\overline{WRES}$ is kept low. When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed. In reset operation, both prereset and reset are required.

Reset Cycle (DSC Mode)



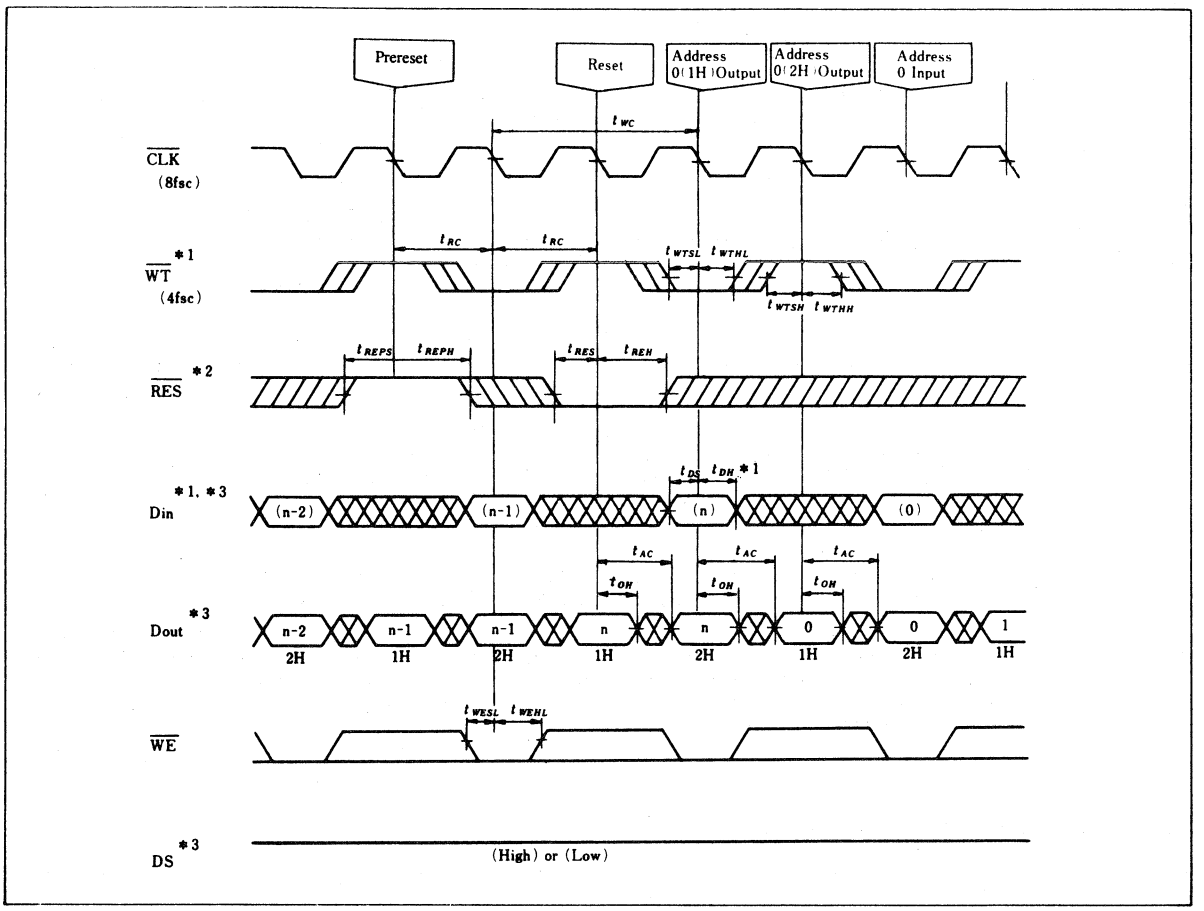
Notes) *1. The write address counter is reset at the first falling edge of $\overline{WCLK}$ after $\overline{WRES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and is not reset at the next falling edge of $\overline{WCLK}$ even if $\overline{WRES}$ is kept low.
When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed.

*2. The read address counter is reset at the first falling edge of $\overline{RCLK}$ after $\overline{RRES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{RCLK}$ even if $\overline{RRES}$ is kept low.
When t_{RES}, t_{REH}, t_{REPS} and t_{REPH} cannot meet the specifications, reset operation is not guaranteed.

*3. When t_{REPH}, t_{RES}, t_{REH}, ($\overline{WRES}$ to $\overline{WCLK}$), t_{RES}, t_{REH}, ($\overline{WRES}$ to $\overline{RCLK}$) or t_{REPS}, t_{REPH}, t_{RES}, t_{REH} ($\overline{PRES}$ to $\overline{RCLK}$) cannot meet the specifications, the output of video signal A is not guaranteed, (Reset Timing I).

*4. When t_{REPS}, ($\overline{WRES}$ to $\overline{RCLK}$), or t_{RES}, t_{REH}, t_{REPS}, t_{REPH}, ($\overline{PRES}$ to $\overline{RCLK}$) cannot meet the specifications, the interpolation signal B is not guaranteed. (Reset Timing II).

Reset Cycle (1H/2H Mode)

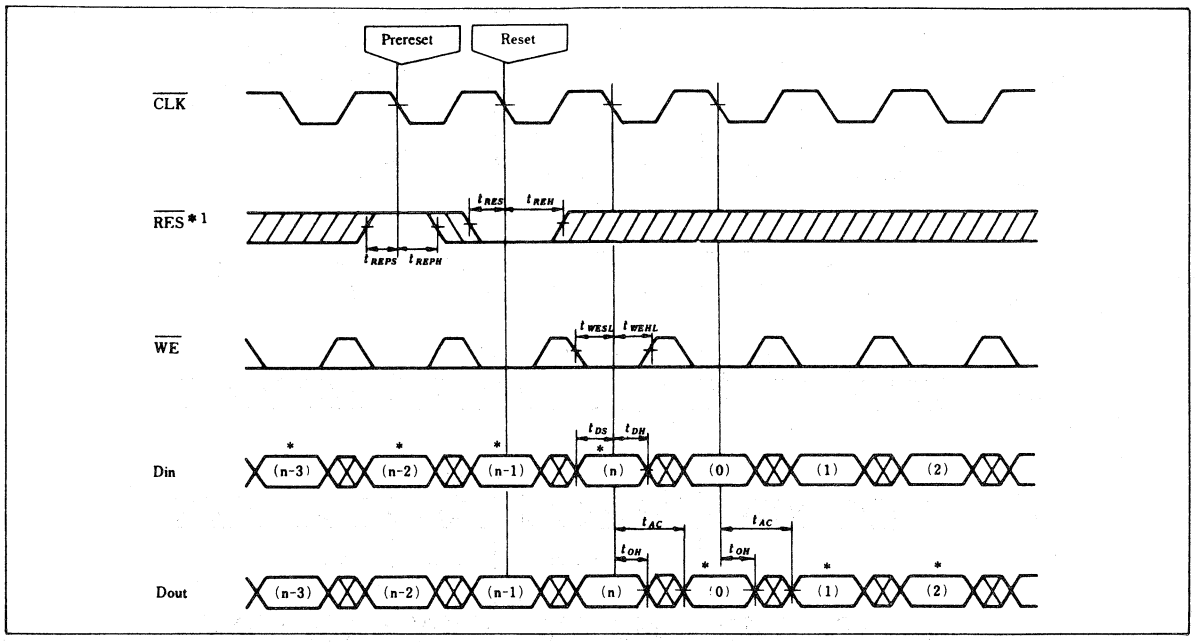


Notes) *1. $\overline{WT}$ is the input during half cycle of $\overline{CLK}$, meeting the specifications of t_{WTSL}, t_{WTHL}, t_{WTSH}, and t_{WTHH}. Data is written when $\overline{WT}$ is low. Reset is possible when $\overline{WT}$ is high.

*2. Read address counter is reset at the first falling edge of $\overline{CLK}$ after $\overline{RES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{CLK}$ even if $\overline{RES}$ is kept low.
When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH}, cannot meet the specifications, the reset operation is not guaranteed.
In reset operation, both prereset and reset are required.

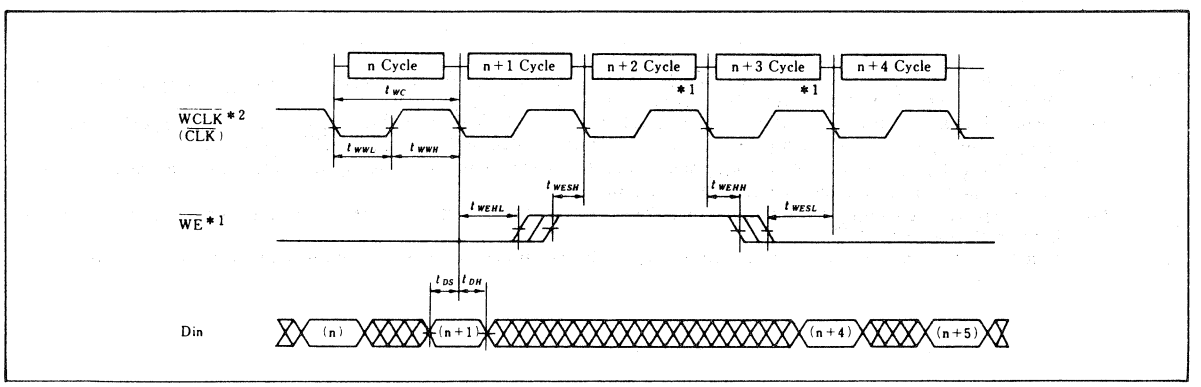
*3. When DS is fixed high, 1H output data is delayed by n bits and 2H output data is delayed by 2n bits where 2n is the reset cycle of $\overline{RES}$.
When DS is fixed low, 1H output data is delayed by n-5 bits and 2H output data is delayed by 2n-5 bits.

Reset Cycle (D Mode)



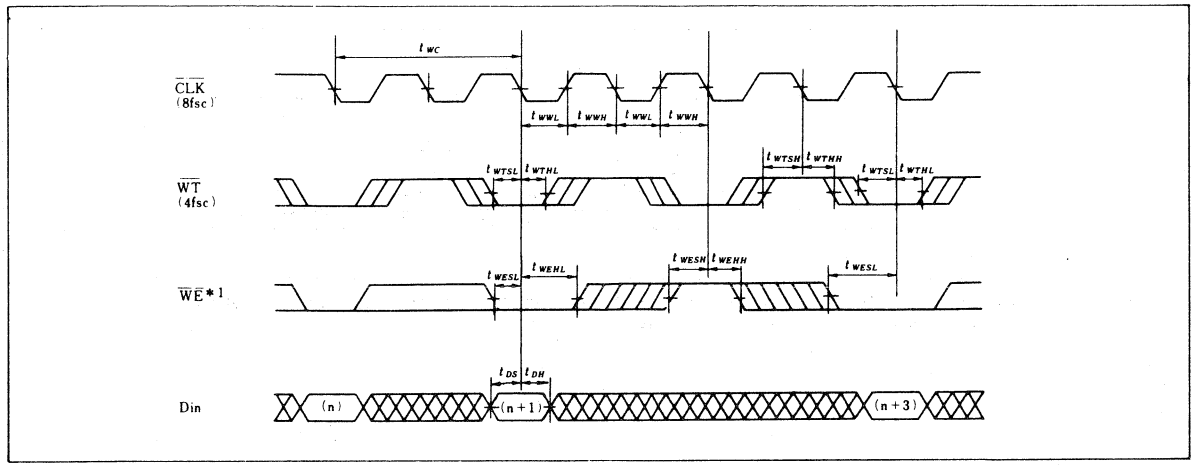
Note) *1. The read address counter is reset at the first falling edge of $\overline{CLK}$ after $\overline{RES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{CLK}$ even if $\overline{RES}$ is kept low.
When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH}, cannot meet the specifications, the reset operation is not guaranteed.
In reset operation, both prereset and reset are required.

Write Enable (TBCE, DSC, TBC, D Modes)



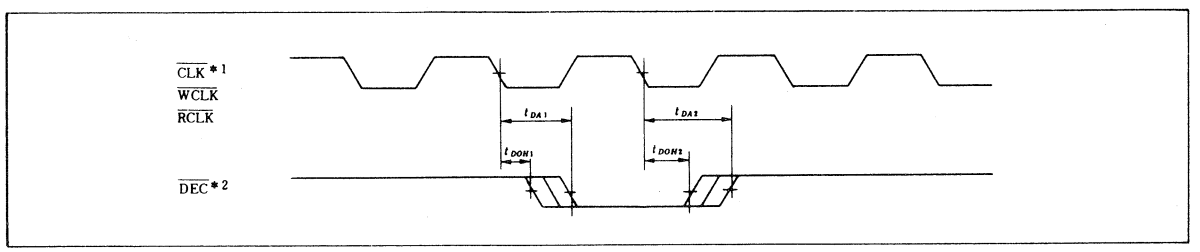
Notes) *1. When t_{WEHL}, t_{WESH}, t_{WEHH}, and t_{WESL} cannot meet this specifications, the write enable operation is not guaranteed.
*2. In the delay line mode, $\overline{CLK}$ takes the place of $\overline{WCLK}$.

Write Enable (1H/2H Mode)



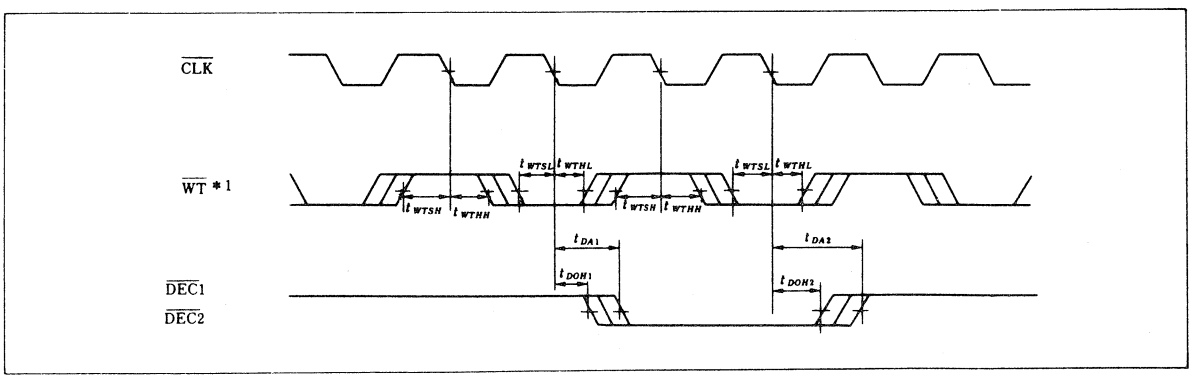
Note) *1. When t_{WTSL}, t_{WTHL}, t_{WEHL}, and t_{WEHH} cannot meet the specifications, the write enable operation is not guaranteed.

Decode Output (TBC, D Modes)



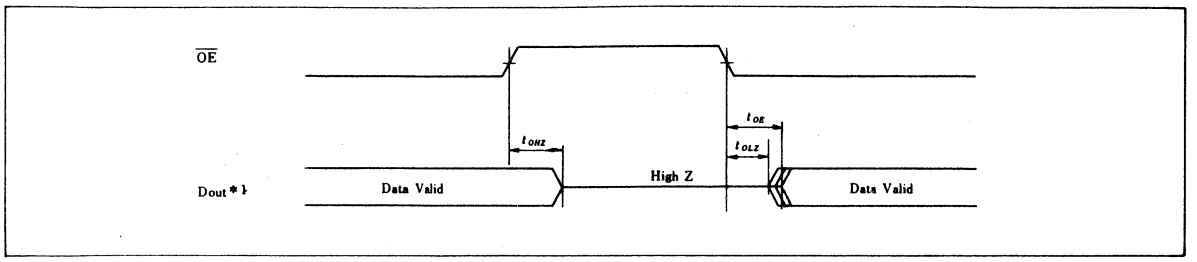
Notes) *1. In TBC mode, $\overline{WCLK}$ or $\overline{RCLK}$ takes the place of $\overline{CLK}$.
*2. $\overline{DEC}$ is $\overline{WDEC}$ or $\overline{RDEC}$ in TBC, $\overline{DEC1}$, $\overline{DEC2}$, $\overline{DEC3}$ or $\overline{DEC4}$ in D mode.

Decode Output (1H/2H Mode)



Note) *1. When t_{WTSL}, t_{WTHL}, t_{WTSH}, and t_{WTHH} cannot meet the specifications, the decode output operation is not guaranteed.

Output Enable (All Modes)



Note) *1. Transition of t_{OHZ} and t_{WLZ} is measured ±200 mV from steady state voltage with Output Load B. This parameter is sampled and not 100% tested.

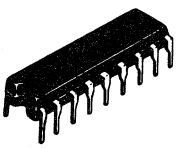
HM53051 Series

262144-word x 4-bit Frame Memory

HM53051P is a 262,144-word x 4-bit frame memory, using the most advanced 1.3µm CMOS processes. It performs serial access by an internal address generator.

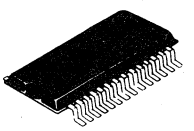
It offers a high-speed cycle time of 34ns, 45ns or 60ns (min). As input data and output data can be written or read in any cycle, synchronized with a system clock, and the delay between data read/write operations is freely settable. Y/C separation and frozen pictures can be realized easily in 8fsc NTSC digital TV or VCR systems. Also, it enables random access in 32-word x 4-bit data block. With this function, picture in picture or a multiplexed picture can be displayed with ease.

HM53051P Series



(DP-18C)

HM53051FP Series



(FP-28DA)

Features

- 262,144-word x 4-bit serial access memory
- Organized with dual ports
  - Serial input x 4-bit
  - Serial output x 4-bit
- High Speed
  - Read/Write Cycle Time: 34ns/45ns/60ns (min)
  - Access Time: 30ns/35ns/40ns (max)
- Semi-synchronous Read/Write Cycle
- Low Power
  - Active : HM53051-34 225 mW(typ)
  - HM53051-45/60 200 mW(typ)
- Random Access in 32-word x 4-bit blocks
- External Refresh Control is unnecessary

Ordering Information

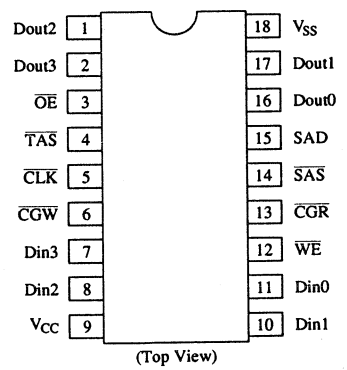
Type No.	Access Time	Package
HM53051P-34 HM53051P-45 HM53051P-60	34ns 45ns 60ns	300-mil 18-pin Plastic DIP
HM53051FP-34 HM53051FP-45 HM53051FP-60	34ns 45ns 60ns	28-pin Plastic SOP

Pin Description

Pin Name	Function
Din	Data Input
Dout	Data Output
$\overline{OE}$	Output Enable
$\overline{TAS}$	Transfer Address Strobe
$\overline{CLK}$	System Clock
$\overline{CGW}$	Clock Gate (Write)
$\overline{CGR}$	Clock Gate (Read)
SAD	Serial Address
$\overline{SAS}$	Serial Address Strobe
$\overline{WE}$	Write Enable

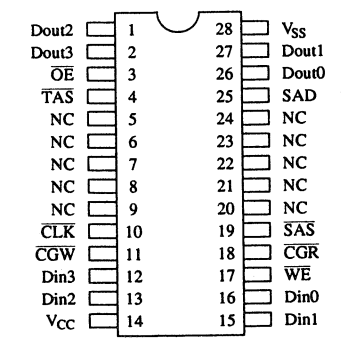
Pin Arrangement

HM53051P Series



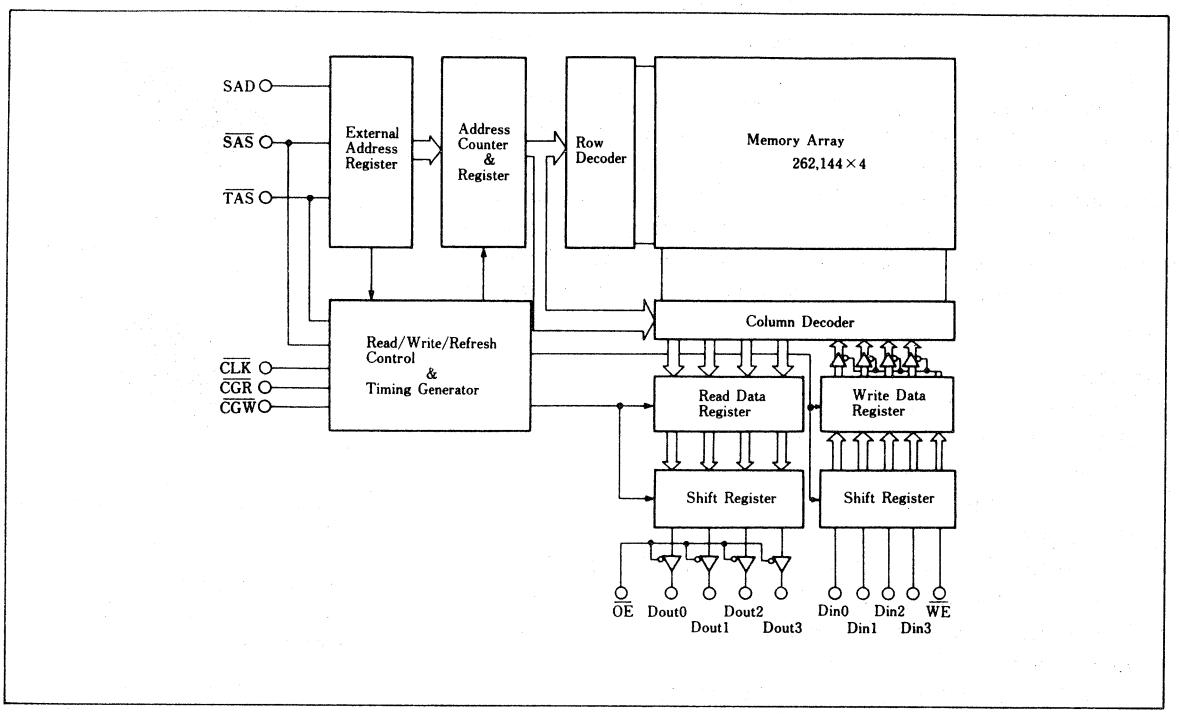
(Top View)

HM53051FP Series



(Top View)

Block Diagram



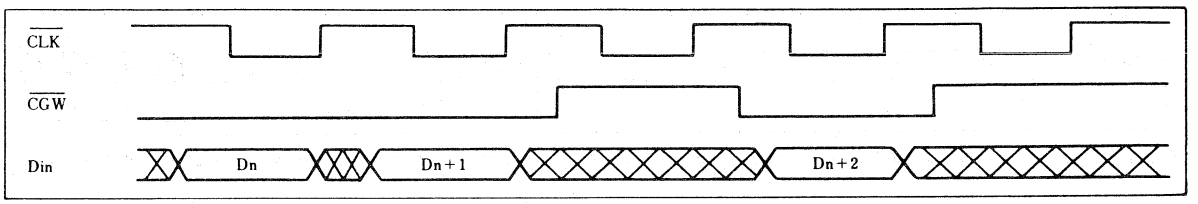
Functional Description

Serial access memory with I/O separated

Read cycle and write cycle of HM53051 can be operated independently synchronized with a system clock. It realizes time compression or expansion for picture in picture in digital TV, for example.

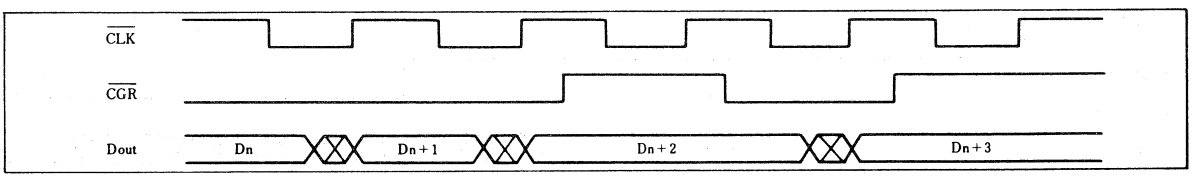
- **Write cycle by $\overline{CGW}$**

Write data are taken in at the falling edge of the system clock $\overline{CLK}$ when $\overline{CGW}$ is low. If $\overline{CGW}$ is high, HM53051 does not enter write cycle (cycle time is defined by system clock cycle time). Time is compressed easily with $\overline{CGW}$.



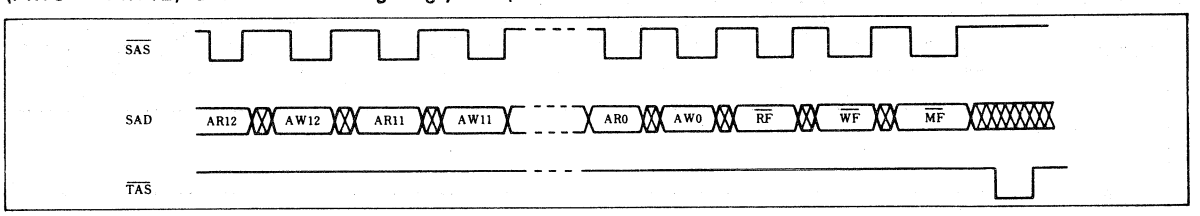
- **Read Cycle by $\overline{CGR}$**

Read data is output at the falling edge of the system clock $\overline{CLK}$ when $\overline{CGR}$ is low. If $\overline{CGR}$ is high, HM53051 does not enter read cycle (cycle time is defined by system clock time). Time is expanded is realized easily with $\overline{CGR}$.



Random Access

The HM53051 is also capable of random access by serial address input, SAD. Random access by the unit of 32-word x 4-bit is performed, when $\overline{TAS}$ is low after read address (AR0 – AR12), write address (AW0 – AW12) and mode setting flags, $\overline{RF}$ (Read Flag), $\overline{WF}$ (Write Flag) and $\overline{MF}$ (Mode Flag) are read into by $\overline{SAD}$ with synchronous $\overline{SAS}$. In order to output data continuously, the address specified by $\overline{SAD}$ increments automatically.



Mode Programming

Operation mode in HM53051 is programmed by the combination of SAD 5-bit.

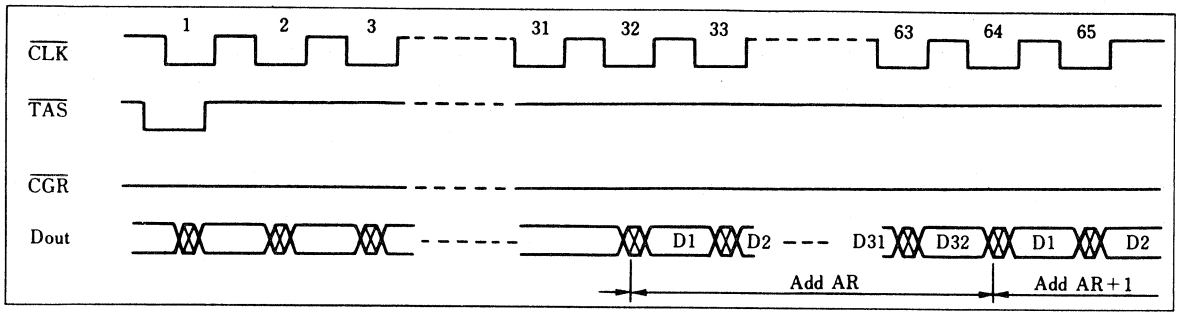
$\overline{MF}$	$\overline{WF}$	$\overline{RF}$	AW0	AR0	Mode
0	0	0	x	x	Write/read address asynchronous transfer
0	0	1	x	x	Write address asynchronous transfer
0	1	0	x	x	Read address asynchronous transfer
0	1	1	x	x	–
1	0	0	x	x	Write/read address synchronous transfer
1	0	1	x	x	Write address synchronous transfer
1	1	0	x	x	Read address synchronous transfer
1	1	1	1	1	System reset
1	1	1	0	0	Inhibit
1	1	1	0	1	
1	1	1	1	0	

Note) x means Don't care.

Read/Write Address Asynchronous Transfer Mode

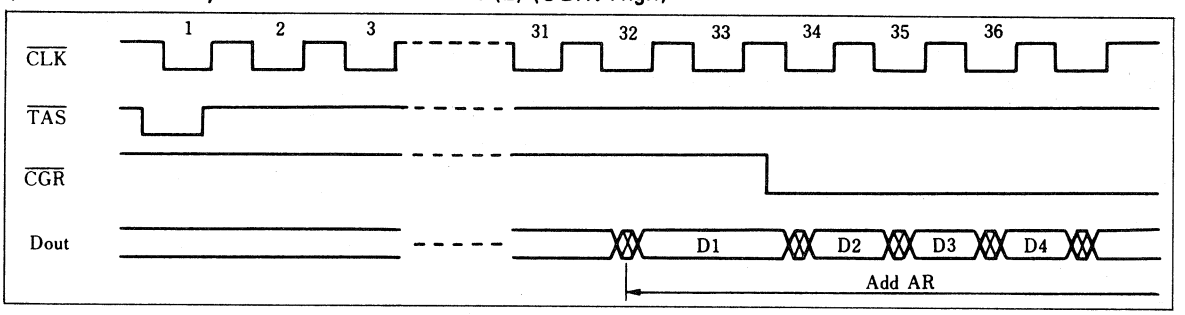
- **Read address asynchronous transfer mode**

(1) Read address asynchronous transfer mode (1) ($\overline{CGR}$: Low)



Note) The data block at read address AR, specified by SAD, is output starting from the 32-nd system clock after the of $\overline{TAS}$.

(2) Read address asynchronous transfer mode (2) ($\overline{CGR}$: High)

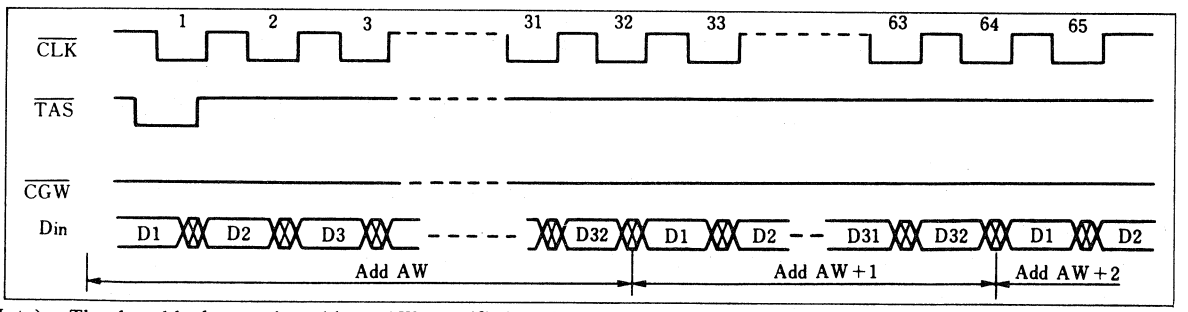


Notes) *1. The data block at read address AR, specified by SAD, is output starting from the 32-nd system clock after the falling of $\overline{TAS}$.

*2. If $\overline{CGR}$ is turned to low after 33-rd clock from the falling edge of $\overline{TAS}$, the data at read address AR (D2, D3, D4 . . .) is output with synchronous $\overline{CLK}$ while $\overline{CGR}$ is low.

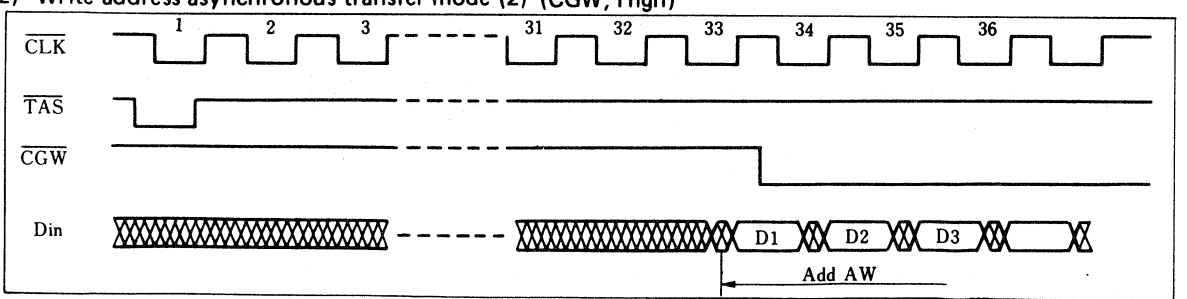
- **Write address asynchronous transfer mode**

(1) Write address asynchronous transfer mode (1) ($\overline{CGW}$: Low)



Note) The data block at write address AW, specified by SAD, is taken in starting from the 1-st clock after the falling edge of $\overline{TAS}$.

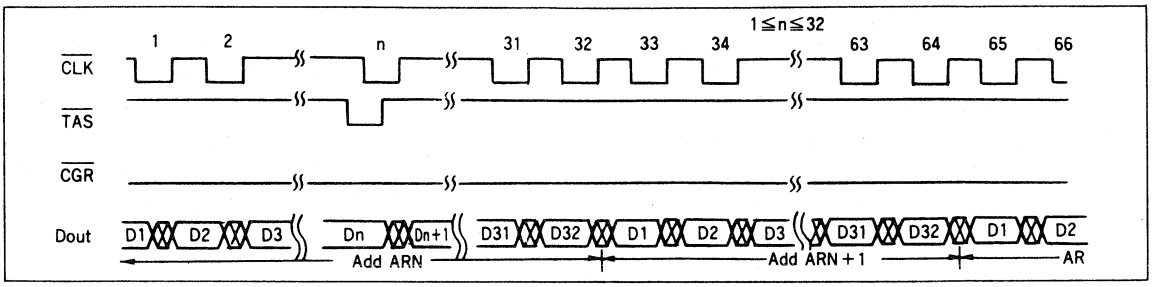
(2) Write address asynchronous transfer mode (2) ($\overline{CGW}$; High)



Note) If $\overline{CGW}$ is turned to low after falling of $\overline{TAS}$, the data block at write address AW is taken in with synchronous $\overline{CLK}$.

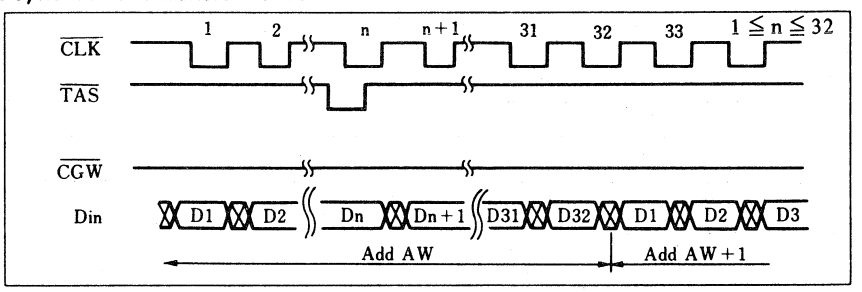
Read/Write Address Synchronous Transfer Mode

- Read address synchronous transfer mode



Note) When $\overline{TAS}$ turns to low, the data block at read address AR, specified by SAD, is output after the data block at the present read address ARN, and the next address ARN+1 is put out.

- Write address synchronous transfer mode



Note) When $\overline{TAS}$ turns to low, the data block being written is taken into write address AW.

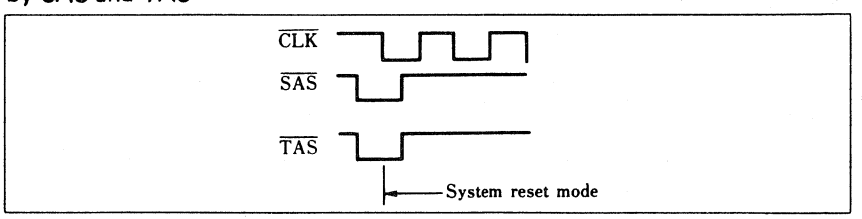
System Reset Mode

System reset mode is the same as read/write address asynchronous transfer mode except that read/write address are reset to 0.

- System reset by SAD

Note) System reset mode starts when $\overline{MF}$, $\overline{WF}$, $\overline{RF}$, AW0, and AR0 are all high.

- System reset by $\overline{SAS}$ and $\overline{TAS}$



Note) System reset mode starts when both $\overline{SAS}$ and $\overline{TAS}$ are low at the falling edge of the $\overline{CLK}$.

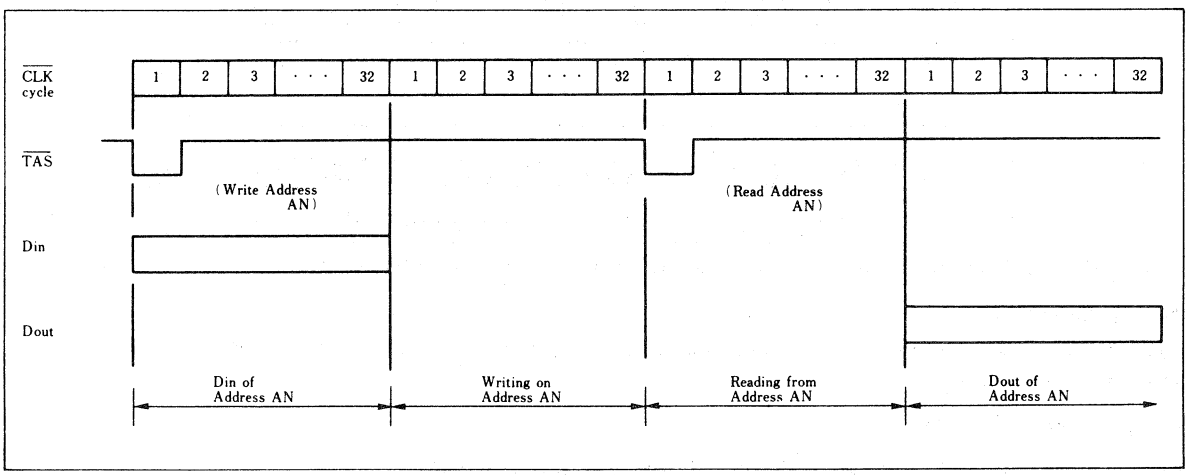
- 1 field delay

Note) Field-delayed data is output, when $\overline{CGR}$ and $\overline{CGW}$ turn to high before the system reset at the beginning of every field, and turn to low simultaneously after the 33rd clock from the system reset.

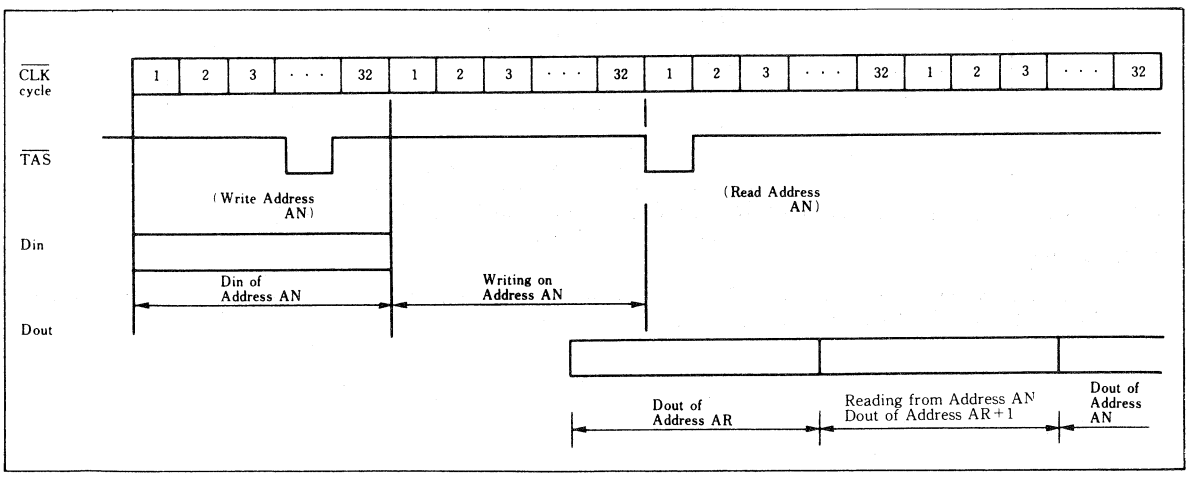
Notes on Using HM53051

- Input/output data of 32 words is not written or read in read/write address asynchronous transfer mode or during system reset. The data is written or read out in blocks of 32-word x 4-bit. Input data of less than 32 words is not written in write address asynchronous transfer mode or during system reset. When asynchronous read address transfer mode or system reset mode is activated, output from the current data block will continue. When output data from the current data block is finished, the next data block is not read out if it has less than 32 words.
- Input data is not read out immediately. The data (32 word x 4-bit) is written into the memory array in the next 32 cycles after it is taken in. The data can be read out only after writing to the memory array is completed. If read address transfer mode is programmed after the 33 word clock from on input data block, new data can be read out. If this mode is programmed before the 33 word clock, new data or old data is output.

(1) Read/write address asynchronous transfer mode



(2) Read/write address synchronous transfer mode

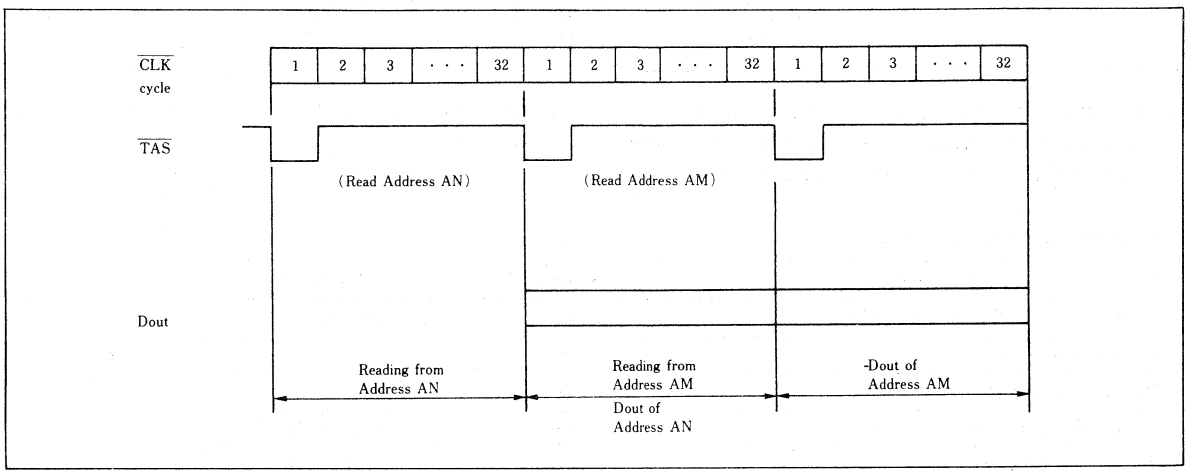


- **Mode programming**

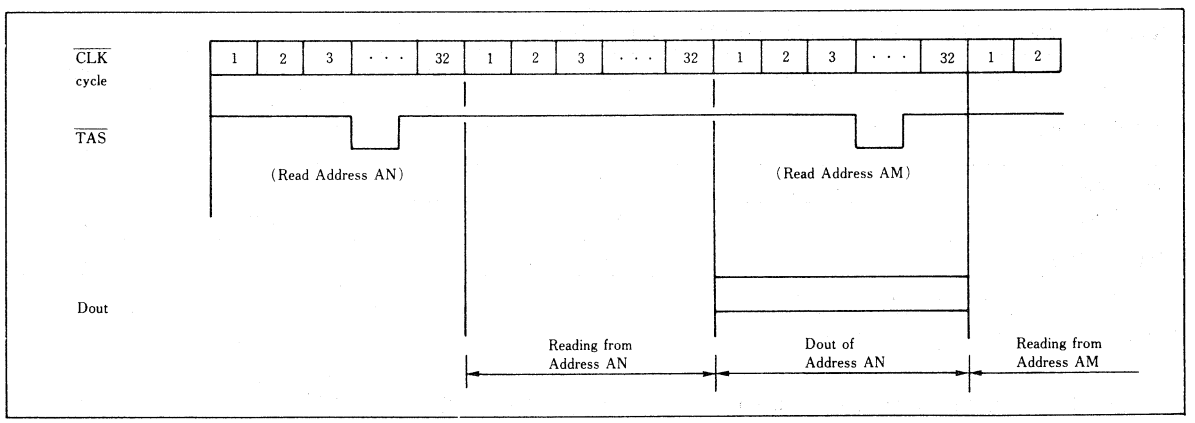
  Do not reprogram read address transfer mode before a read operation of the previous read address transfer mode or system reset mode is completed. If it is reprogrammed during a read operation, address becomes invalid, and the device may malfunction.

  Do not reprogram write address transfer mode or system reset mode before a write operation of the previous write address transfer mode or system reset mode is completed. If it is reprogrammed during a write operation, address become invalid, and the device may malfunction.

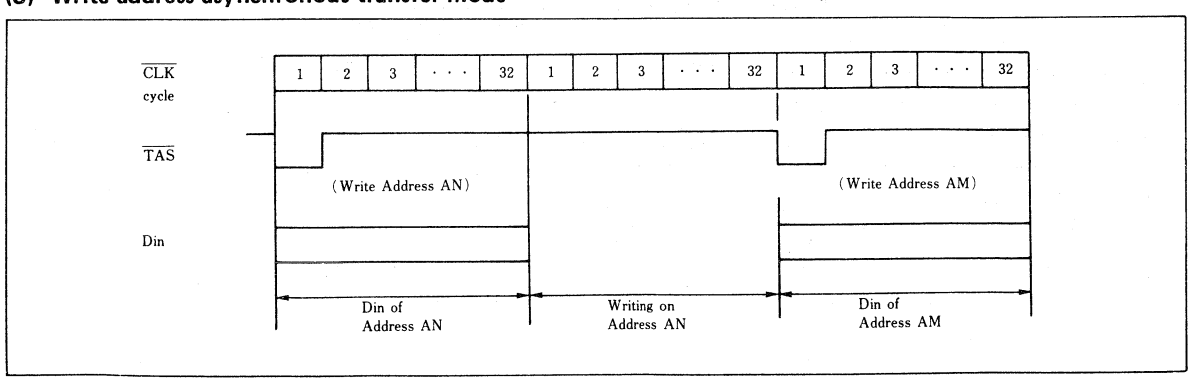
(1) Read address asynchronous transfer mode



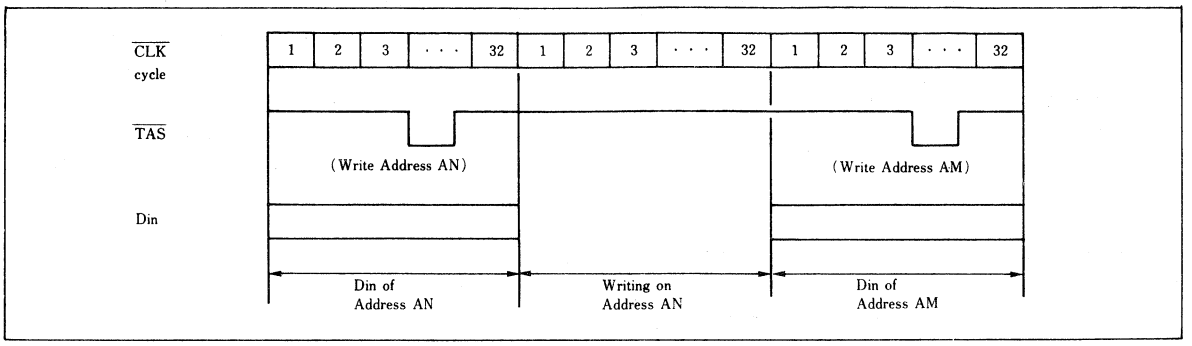
(2) Read address synchronous transfer mode



(3) Write address asynchronous transfer mode



(4) Write address synchronous transfer mode



- Addresses must be set by read and write address asynchronous transfer or system reset 100μs after power on. Before an address can be set, 32 $\overline{CLK}$ initialization cycles or more are required.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	−55 to +125	°C
Storage Temperature (under bias)	Tbias	−10 to +85	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.7	—	6.5	V
($\overline{CLK}$, $\overline{SAS}$)	V_{IL}	−0.5*1	—	0.8	V
Input Voltage	V_{IH}	2.4	—	6.5	V
(All pins except $\overline{CLK}$ and $\overline{SAS}$)	V_{IL}	−0.5*1	—	0.8	V

Note) *1. −3.0V for pulse width $\leq$ 10ns.

DC and Operating Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	HM53051-34			HM53051-45/60			Unit
			min	typ	max	min	typ	max	
Operating Power Supply Current	I_{CC}	Min. cycle Iout=0 mA	—	45	60	—	40	60	mA
Input Leakage Current	I_{LI}	VCC=5.5V Vin=Vss to Vcc	−10	—	10	−10	—	10	μA
Output Leakage Current	I_{LO}	$\overline{OE}$=VIH Vout=Vss to Vcc	−10	—	10	−10	—	10	μA
Output Voltage	V_{OL}	I_{OL}=4.2mA	—	—	0.4	—	—	0.4	V
	V_{OH}	I_{OH}=−2 mA	2.4	—	—	2.4	—	—	V

Capacitance (Ta = 25°C, f = 1.0 MHz)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Capacitance	Cin	Vin = 0 V	–	–	5	pF
Output Capacitance	Cout	Vout = 0 V	–	–	7	pF

Note) This parameter is sampled and not 100% tested.

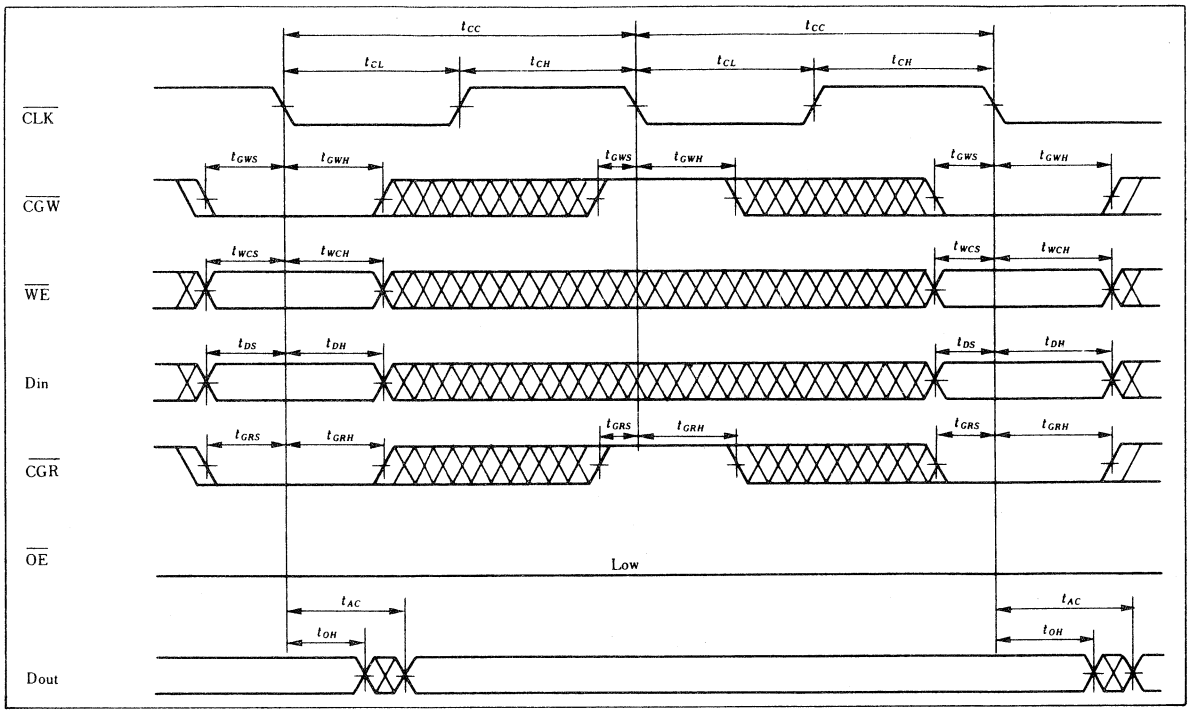
AC Characteristics (V_{CC} = 5 V ± 10%, Ta = 0 to +70°C)

AC Test Conditions

- Input and output timing reference levels: 1.5 V
- Input pulse levels: V_{SS} to 3 V
- Input rise and fall times: 5 ns
- Output Load: 2 TTL + 50 pF
  (Including scope and jig)

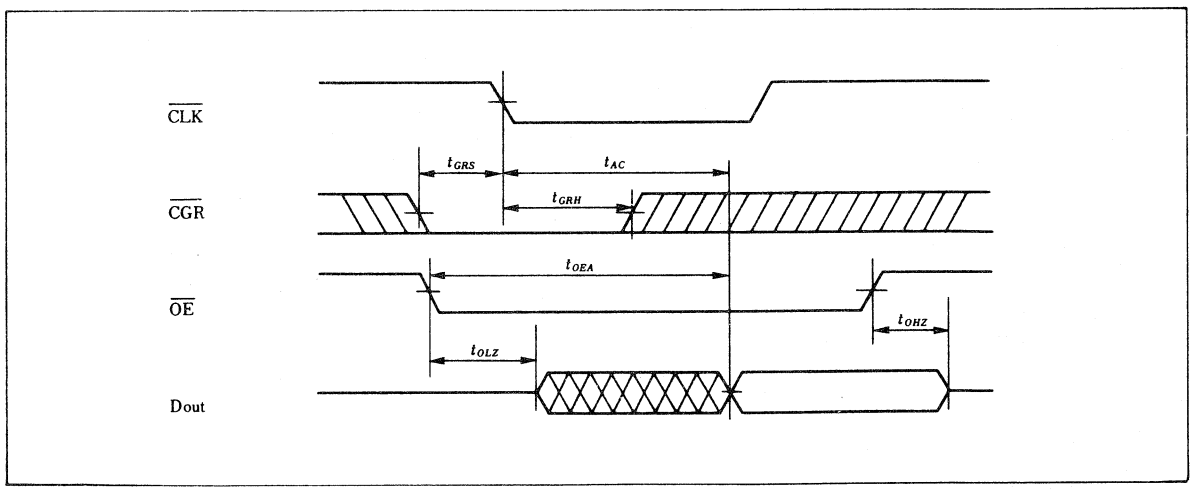
Parameter	Symbol	HM53051-34		HM53051-45		HM53051-60		Unit
		min	max	min	max	min	max	
System Clock Cycle Time	t_{CC}	34	300	45	300	60	300	ns
$\overline{CLK}$ Pulse Width	t_{CL}	15	—	15	—	15	—	ns
	t_{CH}	15	—	15	—	15	—	ns
Access Time from $\overline{CLK}$	t_{AC}	—	30	—	35	—	40	ns
Output Hold Time	t_{OH}	5	—	5	—	8	—	ns
Output Enable Access Time	t_{OEA}	—	25	—	25	—	30	ns
Output Enable to Output in Low Z	t_{OLZ}	5	—	5	—	5	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	20	0	20	0	20	ns
$\overline{CGR}$ Setup Time	t_{GRS}	15	—	15	—	15	—	ns
$\overline{CGR}$ Hold Time	t_{GRH}	5	—	5	—	5	–	ns
$\overline{CGW}$ Setup Time	t_{GWS}	15	—	15	—	15	—	ns
$\overline{CGW}$ Hold Time	t_{GWH}	5	—	5	—	5	—	ns
Write Command Setup Time	t_{WCS}	15	—	15	—	15	—	ns
Write Command Hold Time	t_{WCH}	5	—	5	—	5	—	ns
Data Input Setup Time	t_{DS}	15	—	15	—	15	—	ns
Data Input Hold Time	t_{DH}	5	—	5	—	5	—	ns
$\overline{SAS}$ Cycle Time	t_{SC}	34	—	45	—	60	—	ns
$\overline{SAS}$ Pulse Width	t_{SL}	15	—	15	—	15	—	ns
	t_{SH}	15	—	15	—	15	—	ns
Serial Address Setup Time	t_{SAS}	15	—	15	—	15	—	ns
Serial Address Hold Time	t_{SAH}	5	—	5	—	5	—	ns
$\overline{SAS}$ Setup Time during Mode Programming	t_{SSH}	15	—	15	—	15	—	ns
$\overline{SAS}$ Hold Time during Mode Programming	t_{SHH}	5	—	5	—	5	—	ns
$\overline{TAS}$ Setup Time	t_{TS}	15	—	15	—	15	—	ns
$\overline{TAS}$ Hold Time	t_{TH}	5	—	5	—	5	—	ns
$\overline{SAS}$ Setup Time during System Reset by $\overline{SAS}$/$\overline{TAS}$	t_{SSL}	15	—	15	—	15	—	ns
$\overline{SAS}$ Hold Time during System Reset by $\overline{SAS}$/$\overline{TAS}$	t_{SHL}	5	—	5	—	5	—	ns

Read/Write Cycle



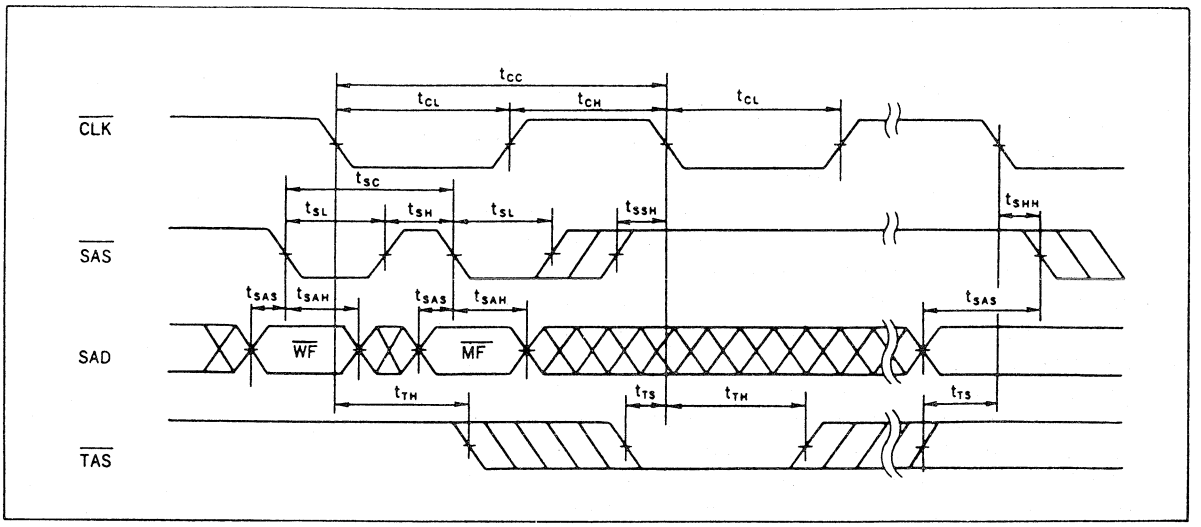
Notes) *1. Write Cycle starts when $\overline{CGW}$ is low and $\overline{WE}$ is low. Data are not written when $\overline{WE}$ is high. Time-compression mode is realized by controlling $\overline{CGW}$.
*2. Read cycle starts when $\overline{CGR}$ is low. Time-expansion mode is realized by controlling $\overline{CGR}$.

Read Cycle ($\overline{OE}$ control)



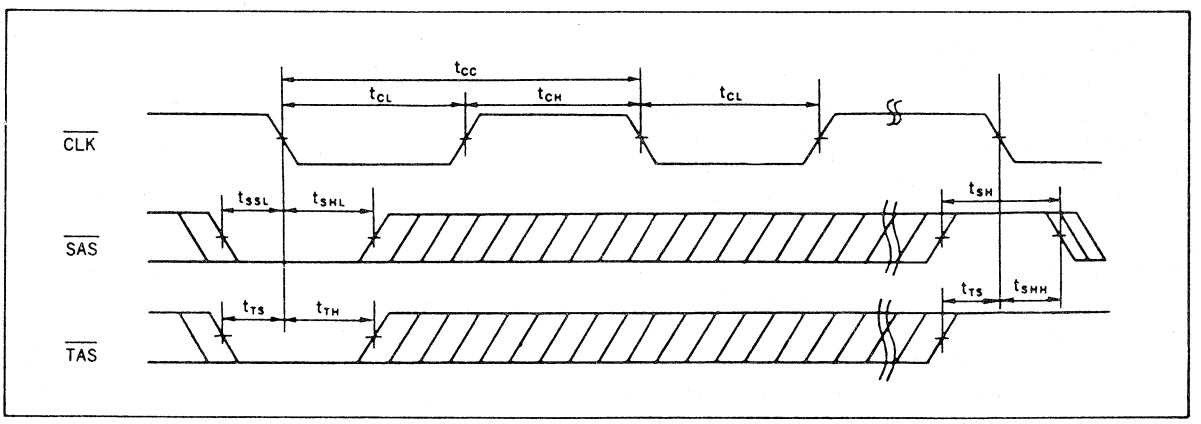
Notes) *1. t_{OHZ} is defined by the time at which the output achieves the open circuit condition.
*2. t_{OLZ} and t_{OHZ} are sampled and not 100% tested.

Mode Selection



Note) $\overline{SAS}$ operates asynchronously with $\overline{CLK}$. When $\overline{TAS}$ is low at the falling edge of the $\overline{CLK}$, the address transfer cycle starts. $\overline{SAS}$ should be high during the address transfer cycle.

$\overline{SAS}$, $\overline{TAS}$ Reset Mode



Note) The mode which was selected by SAD before $\overline{SAS}$ and $\overline{TAS}$ reset, if $\overline{SAS}$ and $\overline{TAS}$ are reset, should be changed because SAD is newly taken into by SAS. The mode should be reselected by SAD after $\overline{SAS}$ and $\overline{TAS}$ reset.

HM53461 Series
HM53462 Series

65,536-word x 4-bit Multiport CMOS Video RAM

The HM53461/HM53462 is a 262, 144-bit multiport memory equipped with a 64k-word x 4-bit Dynamic RAM port and a 256-word x 4-bit Serial Access Memory (SAM) port. The SAM port is connected to an internal 1,024-bit data register through a 256-word x 4-bit serial read or write access control. In the read transfer cycle, the memory cell data is transferred from a selected word line of the RAM port to the data register. The RAM port has a write mask capability in addition to the conventional operation mode. Write bit selection out of 4 data bit can be achieved.

Utilizing the Hitachi 2μm CMOS process, fast serial access operation and low power dissipation are realized. All inputs and outputs, including clocks, are TTL compatible.

In HM53462, RAM port has logic operation capability. By this function, logic operation between memory data and input data can be done in one cycle.

■ FEATURES

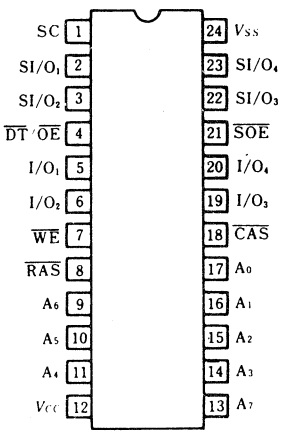
- Multiport organization
  (RAM; 64k-word x 4-bit and SAM; 256 word x 4-bit)
- Double layer polysilicon/polyicide n-well CMOS process
- Single 5V (±10%)
- Low power
  - Active: RAM; 380mW max.
  - Active: SAM; 220mW max.
  - Standby: 40mW max.
- Access Time
  - RAM; 100ns/120ns/150ns
  - SAM; 40ns/40ns/60ns
- Cycle Time
  - Random read or write cycle time (RAM)
    190ns/220ns/260ns
  - Serial read or write cycle time (SAM)
    40ns/40ns/60ns
- TTL compatible
- 256 refresh cycles 4ms
- Refresh function
  - $\overline{RAS}$ – only refresh
  - $\overline{CAS}$ – before – $\overline{RAS}$ refresh
  - Hidden refresh
- Data transfer operation (RAM⇄SAM)
- Fast serial access operation asynchronized with RAM port except data transfer cycle
- Real time read transfer capability
- Write mask mode capability
- Logic operation capability between Din and Dout (HM53462 Series)
- SAM organization can be changed to 1,024 x 1 (HM53462 Series)

■ ORDERING INFORMATION

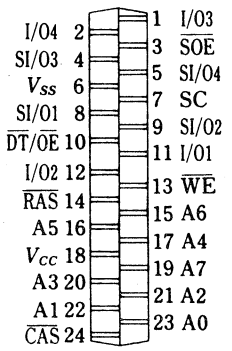
Type No.	Access Time	Package
HM53461P-10	100ns	400mil 24-pin
HM53461P-12	120ns	Plastic DIP
HM53461P-15	150ns	(DP-24A)
HM53461ZP-10	100ns	24-pin
HM53461ZP-12	120ns	Plastic ZIP
HM53461ZP-15	150ns	(ZP-24)
HM53461JP-10	100ns	24-pin
HM53461JP-12	120ns	Plastic SOJ
HM53461JP-15	150ns	(CP-24D)
HM53462P-10	100ns	400mil 24-pin
HM53462P-12	120ns	Plastic DIP
HM53462P-15	150ns	(DP-24A)
HM53462ZP-10	100ns	28-pin
HM53462ZP-12	120ns	Plastic ZIP
HM53462ZP-15	150ns	(ZP-24)
HM53462JP-10	100ns	300mil 24-pin
HM53462JP-12	120ns	Plastic SOJ
HM53462JP-15	150ns	(CP-24D)

■ PIN ARRANGEMENT

- HM53461P/JP Series
- HM53462P/JP Series
- HM53461ZP Series
- HM53462ZP Series



(Top View)



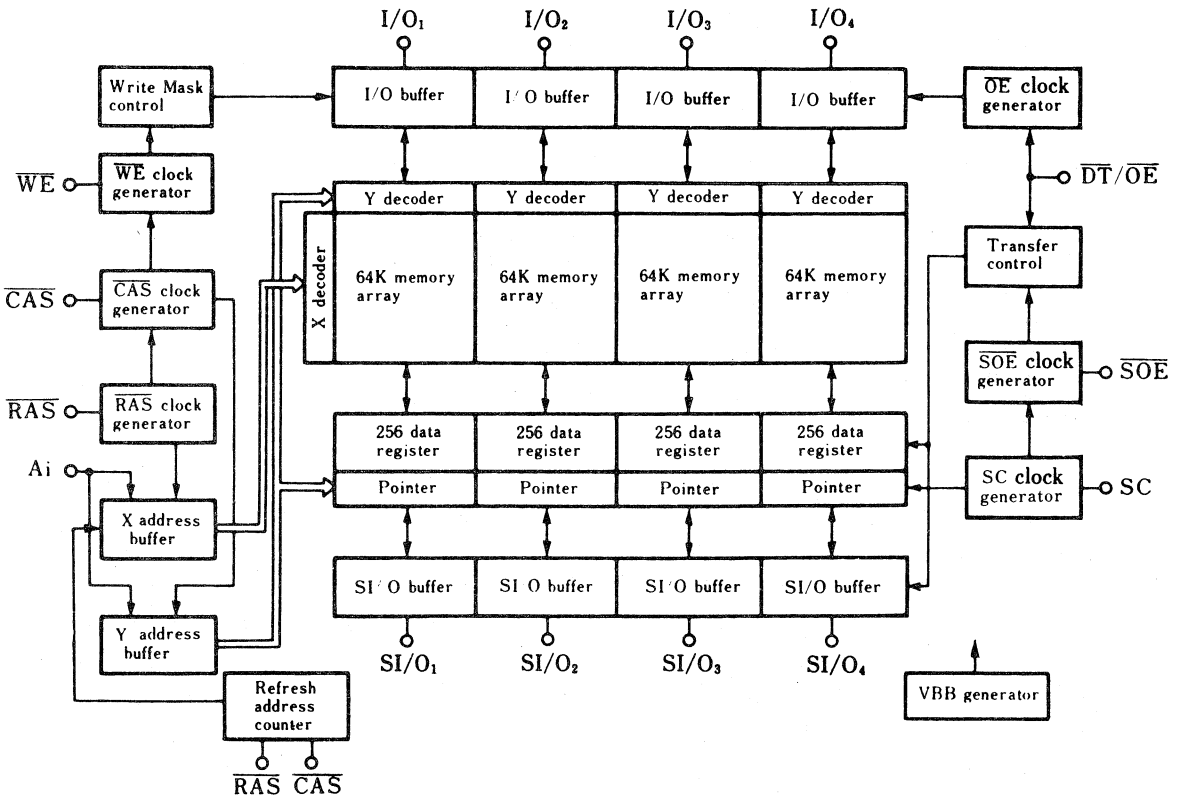
(Bottom View)

■ PIN DESCRIPTION

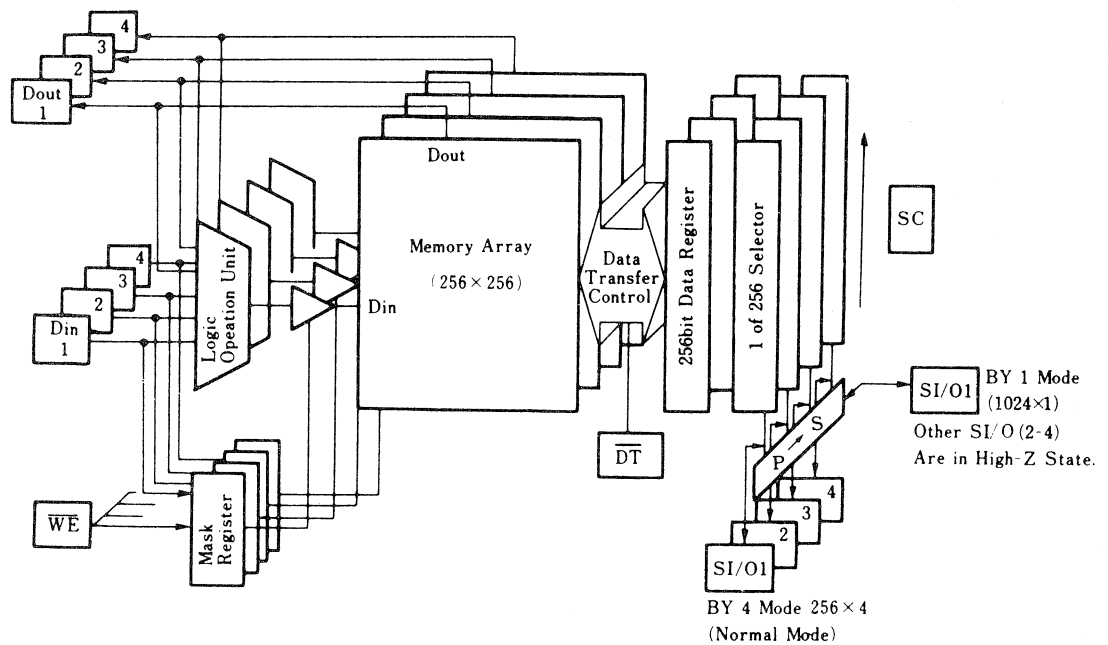
Pin Name	Function
A0 – A7	Address Inputs
I/O1 – I/O4	RAM Port Data Input/Output
SI/O1 – SI/O4	SAM Port Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
SC	Serial Clock
$\overline{WE}$	Write Enable
$\overline{DT}/\overline{OE}$	Data Transfer/Output Enable
$\overline{SOE}$	SAM Port Enable
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM

HM53461 Series



HM53462 Series



■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . -1V to +7V
Power supply voltage relative to V_{SS} . . . . . -0.5V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature . . . . . -55°C to +125°C
Short circuit output current 50mA
Power dissipation 1W

■ RECOMMENDED DC OPERATING CONDITIONS (T_a=0 to +70°C)

Parameter	Symbol	min.	typ.	max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input High voltage	V_{IH}	2.4	–	6.5	V
Input Low voltage	V_{IL}	-0.5*2	–	0.8	V

Notes: 1. All voltages referenced to V_{SS}.
2. -3.0V for pulse width ≦ 10ns.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

RAM PORT	Symbol	SAM PORT		HM53461-10 HM53462-10	HM53461-12 HM53462-12	HM53461-15 HM53462-15	Unit
		Standby	Active				
Operating current $\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min.	I_{CC1}	O	X	70	60	50	mA
	I_{CC7}	X	O	110	100	80	mA
Standby current $\overline{RAS}$, $\overline{CAS}$ = V_{IH}	I_{CC2}	O	X	7	7	7	mA
	I_{CC8}	X	O	40	40	30	mA
$\overline{RAS}$ only refresh current $\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling t_{RC} = min.	I_{CC3}	O	X	60	50	40	mA
	I_{CC9}	X	O	100	90	70	mA
Page mode current $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min.	I_{CC4}	O	X	50	40	35	mA
	I_{CC10}	X	O	90	80	65	mA
CBR refresh current $\overline{RAS}$ cycling t_{RC} = min.	I_{CC5}	O	X	60	50	40	mA
	I_{CC11}	X	O	100	90	70	mA
Data transfer current $\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min.	I_{CC6}	O	X	75	65	55	mA
	I_{CC12}	X	O	115	105	85	mA

Parameter	Symbol	min.	max.	Unit
Input leakage	I_{LI}	-10	10	μA
Output leakage	I_{LO}	-10	10	μA
Output high voltage I_{OH}=-2mA	V_{OH}	2.4	–	V
Output low voltage I_{OL}=4.2mA	V_{OL}	–	0.4	V

■ INPUT/OUTPUT CAPACITANCE

Parameter	Symbol	typ.	max.	Unit
Address	CI1	–	5	pF
Clocks	CI2	–	5	pF
I/O, SI/O	$C_{I/O}$	–	7	pF

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (T_a=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)[1), 10), 11)]

Parameter	Symbol	HM53461-10 HM53462-10		HM53461-12 HM53462-12		HM53461-15 HM53462-15		Unit	Note
		min.	max.	min.	max.	min.	max.		
Random Read or Write Cycle Time	t_{RC}	190	–	220	–	260	–	ns	
Read-Modify-Write Cycle Time	t_{RWC}	260	–	300	–	355	–	ns	
Page Mode Cycle Time	t_{PC}	70	–	85	–	105	–	ns	
Access Time from $\overline{RAS}$	t_{RAC}	–	100	–	120	–	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	–	50	–	60	–	75	ns	3, 4
Output Buffer Turn Off Delay referenced to $\overline{CAS}$	t_{OFF1}	–	25	–	30	–	40	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
$\overline{RAS}$ Precharge Time	t_{RP}	80	–	90	–	100	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	50	25	60	30	75	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	50	–	60	–	75	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	–	120	–	150	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	10	–	ns	
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	15	–	15	–	20	–	ns	
Column Address Setup Time	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	20	–	20	–	25	–	ns	
Write Command Setup Time	t_{WCS}	0	–	0	–	0	–	ns	8
Write Command Hold Time	t_{WCH}	25	–	25	–	30	–	ns	
Write Command Pulse Width	t_{WP}	15	–	20	–	25	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	35	–	40	–	45	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	35	–	40	–	45	–	ns	
Data-in Setup Time	t_{DS}	0	–	0	–	0	–	ns	9
Data-in Hold Time	t_{DH}	25	–	25	–	30	–	ns	8, 9
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Refresh Period	t_{REF}	–	4	–	4	–	4	ms	
$\overline{RAS}$ Pulse Width (Read-Modify-Write Cycle)	t_{RWS}	170	10000	200	10000	245	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	85	–	100	–	125	–	ns	8
$\overline{CAS}$ Setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20	–	25	–	30	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	15	–	20	–	ns	
Access Time from $\overline{OE}$	t_{OAC}	–	30	–	35	–	40	ns	
Output Buffer Turn-off Delay referenced to $\overline{OE}$	t_{OFF2}	–	25	–	30	–	40	ns	
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	25	–	30	–	40	–	ns	
$\overline{OE}$ Hold Time referenced to $\overline{WE}$	t_{OEH}	10	–	15	–	20	–	ns	
Data-in to $\overline{CAS}$ Delay Time	t_{DZC}	0	–	0	–	0	–	ns	
Data-in to $\overline{OE}$ Delay Time	t_{DZO}	0	–	0	–	0	–	ns	
$\overline{OE}$ to $\overline{RAS}$ Delay Time	t_{ORD}	35	–	40	–	45	–	ns	
Serial Clock Cycle Time	t_{SCC}	40	–	40	–	60	–	ns	
Access Time from SC	t_{SCA}	–	40	–	40	–	60	ns	10
Access Time from $\overline{SOE}$	t_{SEA}	–	25	–	30	–	40	ns	10
SC Pulse Width	t_{SC}	10	–	10	–	10	–	ns	

(to be continued)

Parameter	Symbol	HM53461-10 HM53462-10		HM53461-12 HM53462-12		HM53461-15 HM53462-15		Unit	Note
		min.	max.	min.	max.	min.	max.		
SC Precharge Width	t_{SCP}	10	–	10	–	10	–	ns	
Serial Data-out Hold Time after SC High	t_{SOH}	10	–	10	–	10	–	ns	
Serial Output Buffer Turn-off Delay from $\overline{SOE}$	t_{SEZ}	–	25	–	25	–	30	ns	
Serial Data-in Setup Time	t_{SIS}	0	–	0	–	0	–	ns	
Serial Data-in Hold Time	t_{SIH}	15	–	20	–	25	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	–	0	–	0	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time(Read Transfer Cycle)	t_{RDH}	80	–	90	–	110	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	15	–	15	–	20	–	ns	
$\overline{DT}$ to $\overline{CAS}$ Hold Time	t_{CDH}	20	–	30	–	45	–	ns	
Last SC to $\overline{DT}$ Delay Time	t_{SDD}	5	–	5	–	10	–	ns	
First SC to $\overline{DT}$ Hold Time	t_{SDH}	25	–	25	–	30	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Delay Time	t_{DTR}	10	–	10	–	10	–	ns	
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	–	0	–	0	–	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	–	15	–	20	–	ms	
I/O to $\overline{RAS}$ Setup Time	t_{MS}	0	–	0	–	0	–	ns	
I/O to $\overline{RAS}$ Hold Time	t_{MH}	15	–	15	–	20	–	ns	
Serial Output Buffer Turn-off Delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	75	ns	
$\overline{SC}$ to $\overline{RAS}$ Setup Time	t_{SRS}	30	–	40	–	45	–	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	–	30	–	35	–	ns	
Serial Data Input Delay Time from $\overline{RAS}$	t_{SID}	50	–	60	–	75	–	ns	
Serial Data Input to $\overline{DT}$ Delay Time	t_{SZD}	0	–	0	–	0	–	ns	
$\overline{SOE}$ to $\overline{RAS}$ Setup Time	t_{ES}	0	–	0	–	0	–	ns	
$\overline{SOE}$ to $\overline{RAS}$ Hold Time	t_{EH}	15	–	15	–	20	–	ns	
Serial Write Enable Setup Time	t_{SWS}	0	–	0	–	0	–	ns	
Serial Write Enable Hold Time	t_{SWH}	35	–	35	–	55	–	ns	
Serial Write Disable Setup Time	t_{SWIS}	0	–	0	–	0	–	ns	
Serial Write Disable Hold Time	t_{SWIH}	35	–	35	–	55	–	ns	
$\overline{DT}$ to Sout in Low-Z Delay Time	t_{DLZ}	5	–	10	–	10	–	ns	

Notes)

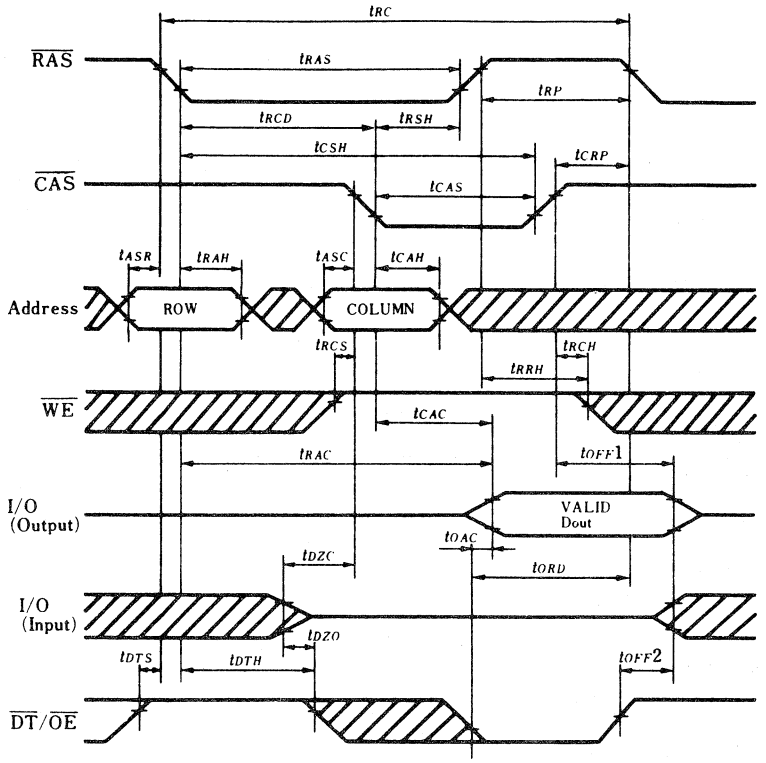
1. AC measurements assume t_T=5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$(max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$(max).
5. t_{OFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD}(max) limit insures that t_{RAC} (max) can be met, t_{RCD}(max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$(min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycle and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. Measured with a load circuit equivalent to 2TTL and 50pF.
11. An initial pause of 100μs is required after power-up. Then execute at least 8 initialization cycles.

    (HM53461 Series)

    After power-up, pause for more than 100μs and execute at least 8 initialization cycles. Then execute at least one logic reset cycle including write mask reset (on the falling edge of $\overline{RAS}$, $\overline{WE}$ = "Low" and I/O1 – I/O4="High"), and execute one or more transport cycle for initiation of SAM port. (HM53462 Series)
12. After a read transfer cycle, the first SAM is needed to be read out before $\overline{CAS}$ falling edge in the succeeding read transfer cycle. When SAM is not read out after a read transfer cycle or when SAM read out is not used as valid data, the restriction mentioned above is not required.

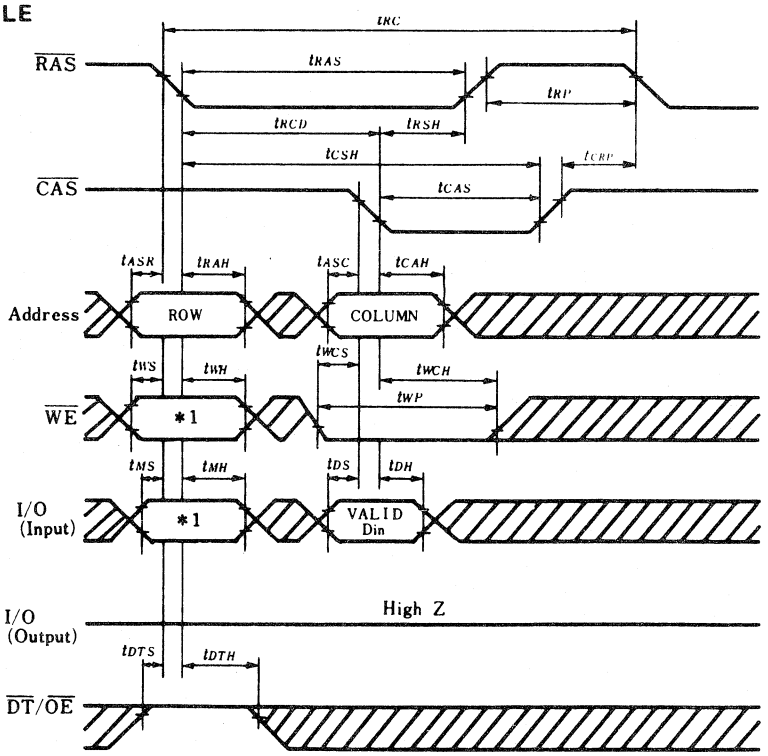
■ WAVE FORMS

● READ CYCLE



Do not care

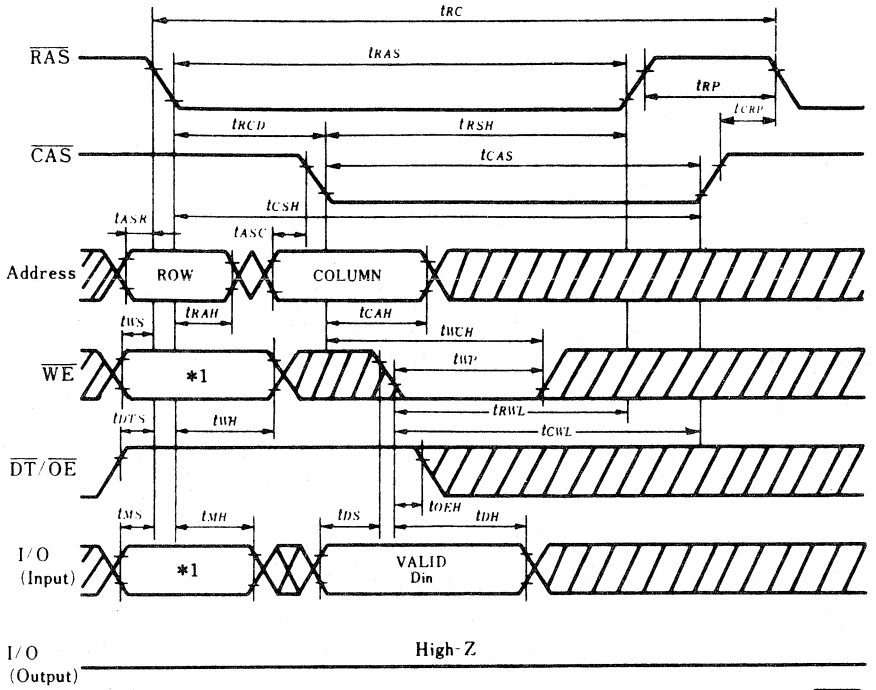
● EARLY WRITE CYCLE



Do not care

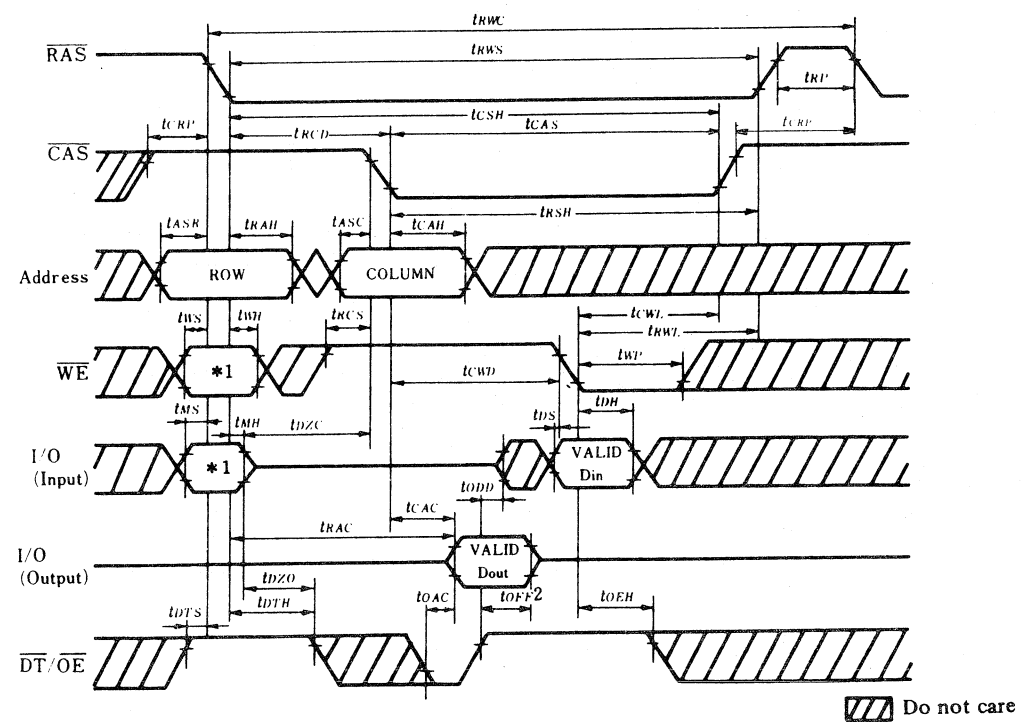
Note) *1. When $\overline{WE}$ is "H" level, all the data on the I/O can be written into the cell.
When $\overline{WE}$ is "L" level, the data on the I/O are not written except for when I/O is 'high' at the falling edge of $\overline{RAS}$.

• DELAYED WRITE CYCLE



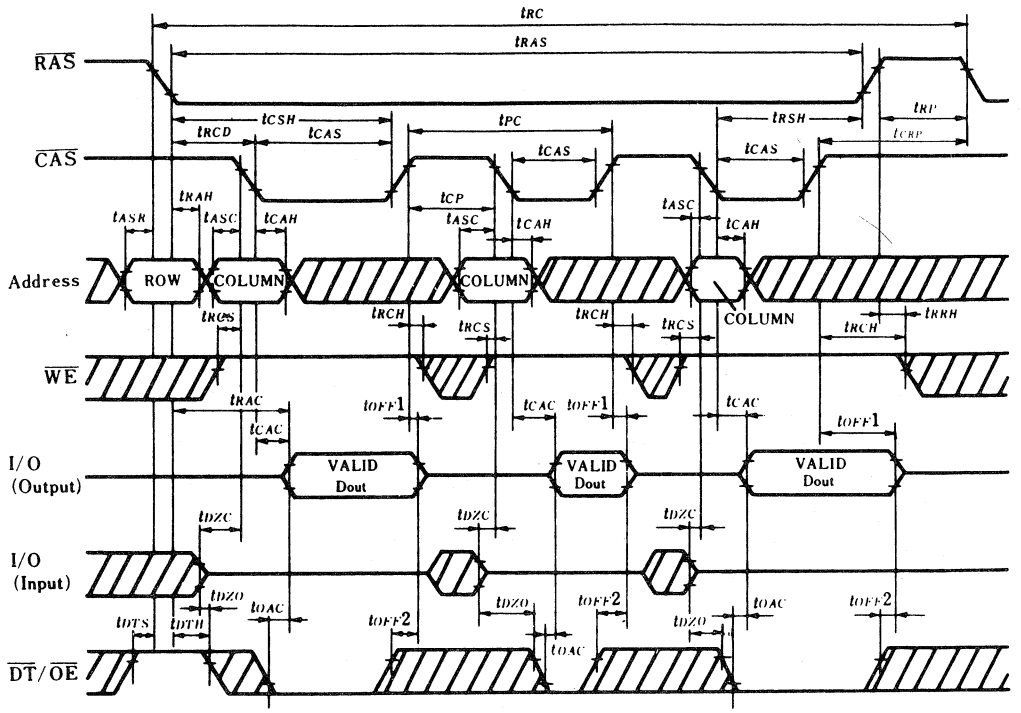
Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O1-I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written exept for when I/O="H" at the falling edge of $\overline{RAS}$.

• READ MODIFY WRITE CYCLE

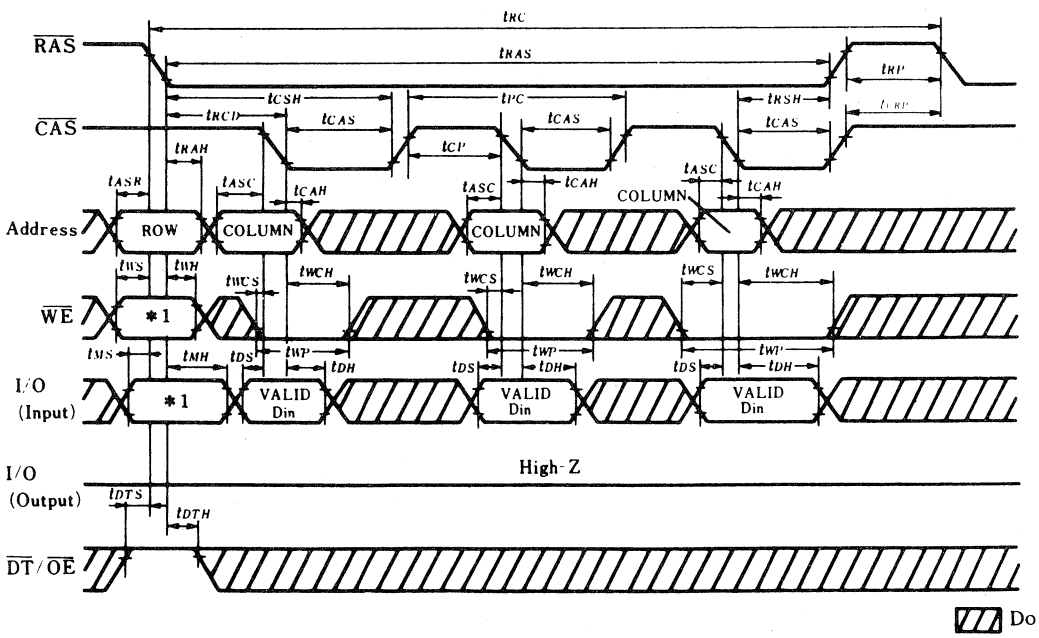


Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O1-I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O="H" at the falling edge of $\overline{RAS}$.

• PAGE MODE READ CYCLE

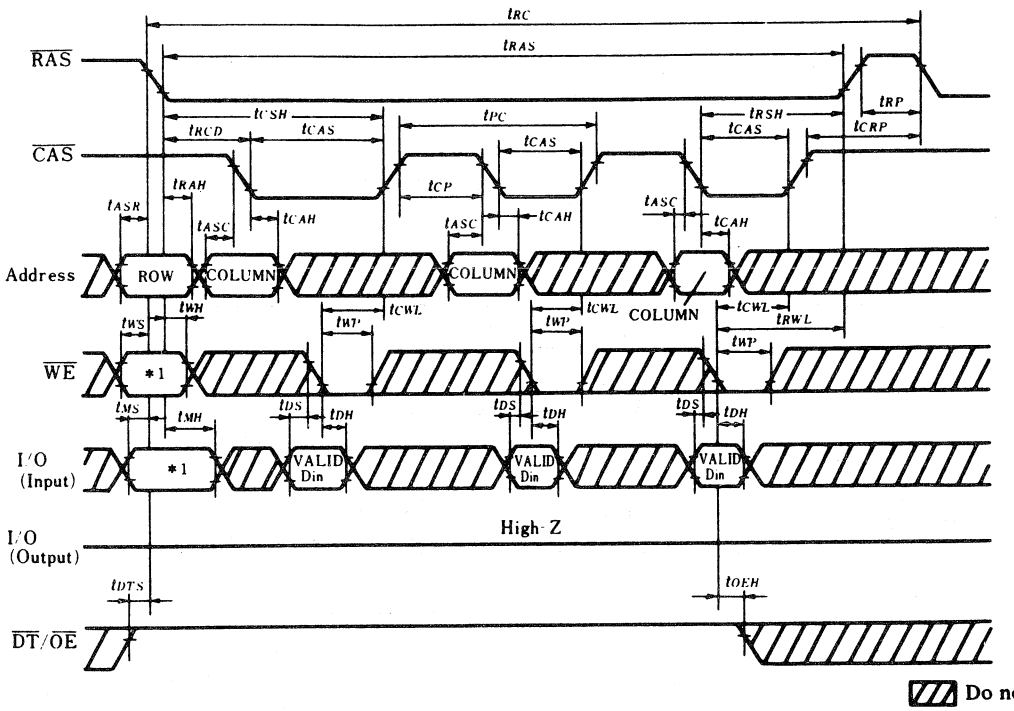


• PAGE MODE WRITE CYCLE (Early Write)



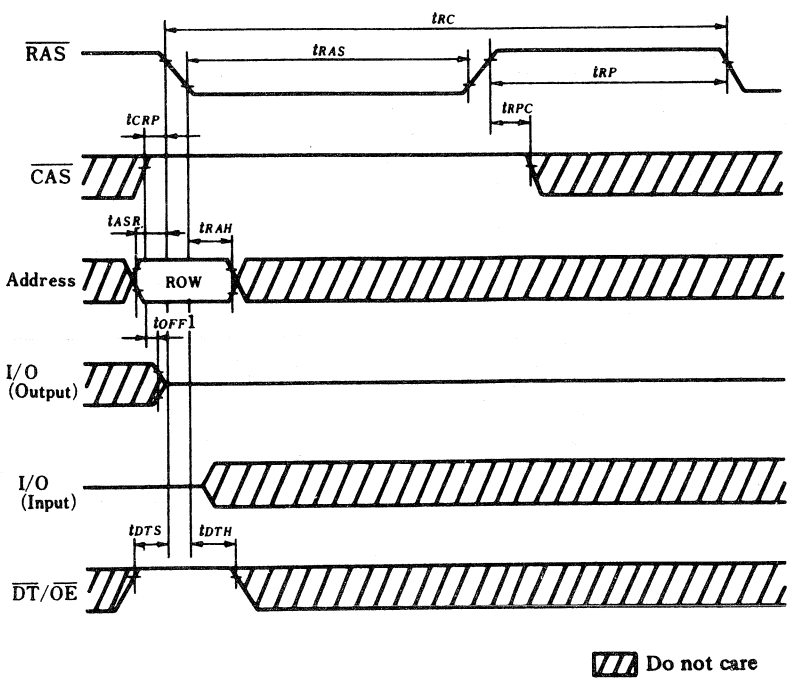
Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O1-I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O="H" at the falling edge of $\overline{RAS}$.

• PAGE MODE WRITE CYCLE (Delayed Write)

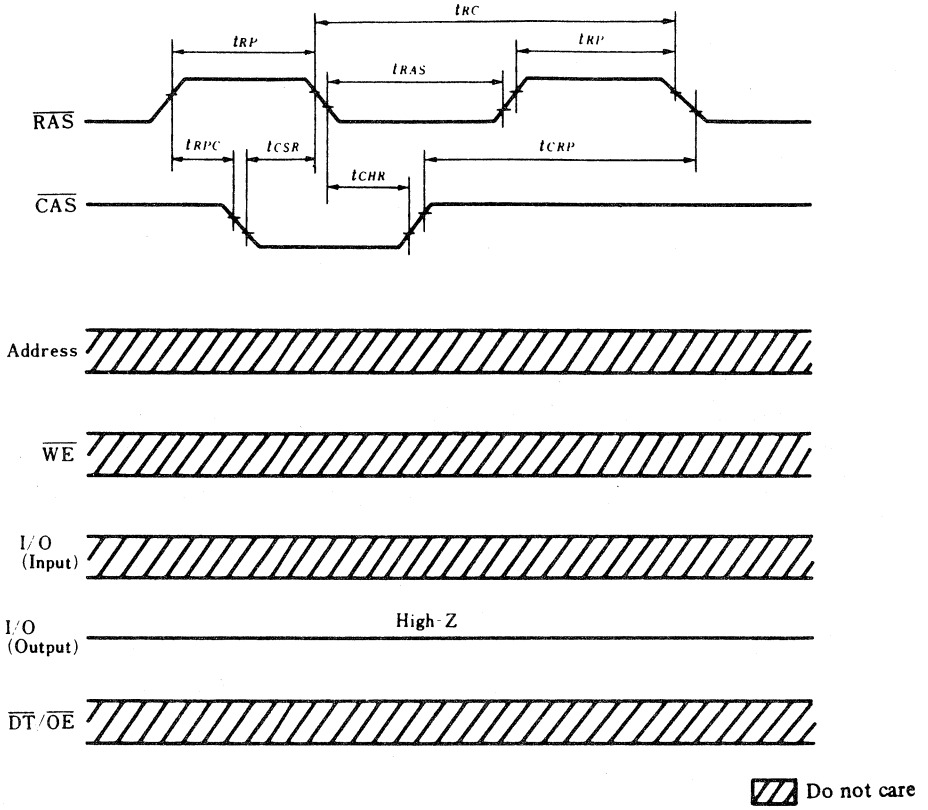


Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O1–I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O="H" at the falling edge of $\overline{RAS}$.

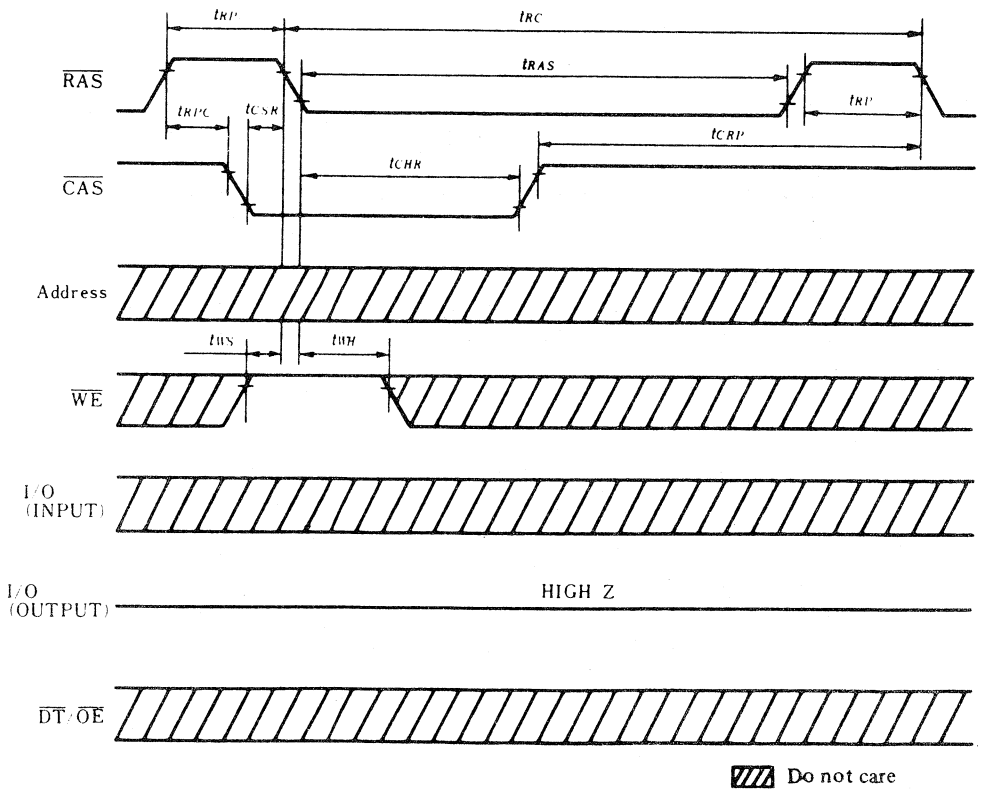
• $\overline{RAS}$-ONLY REFRESH CYCLE



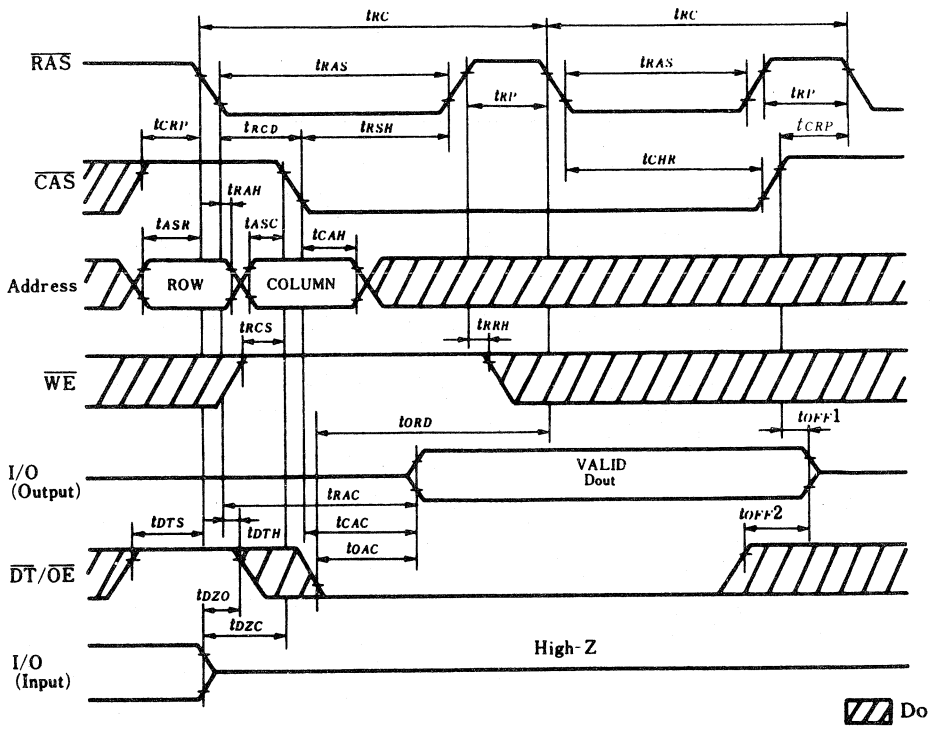
• $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH (HM53461 Series)



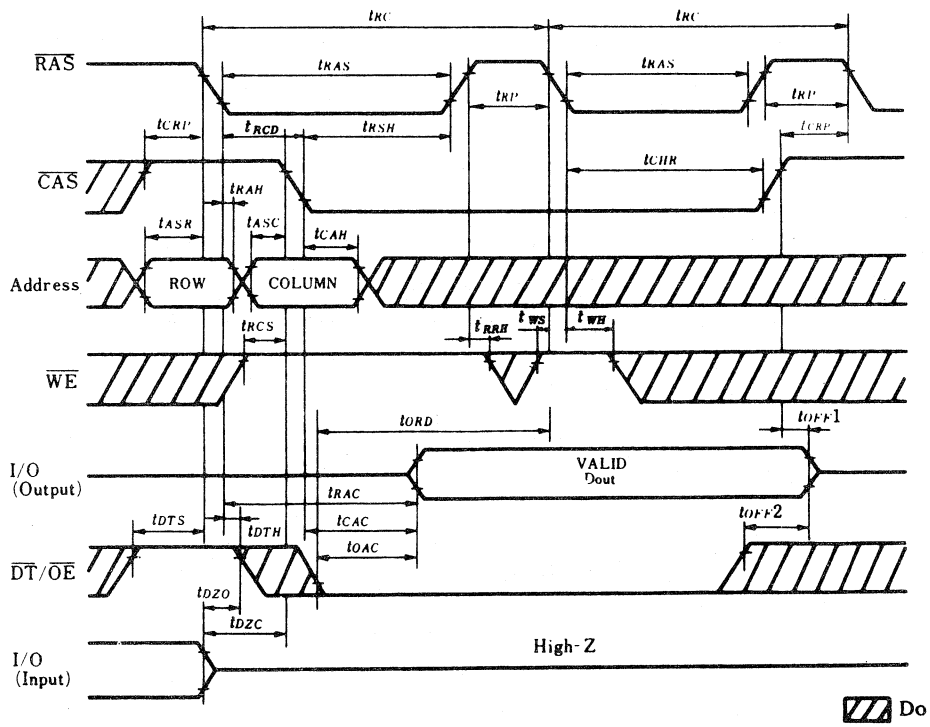
• $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (HM53462 Series)



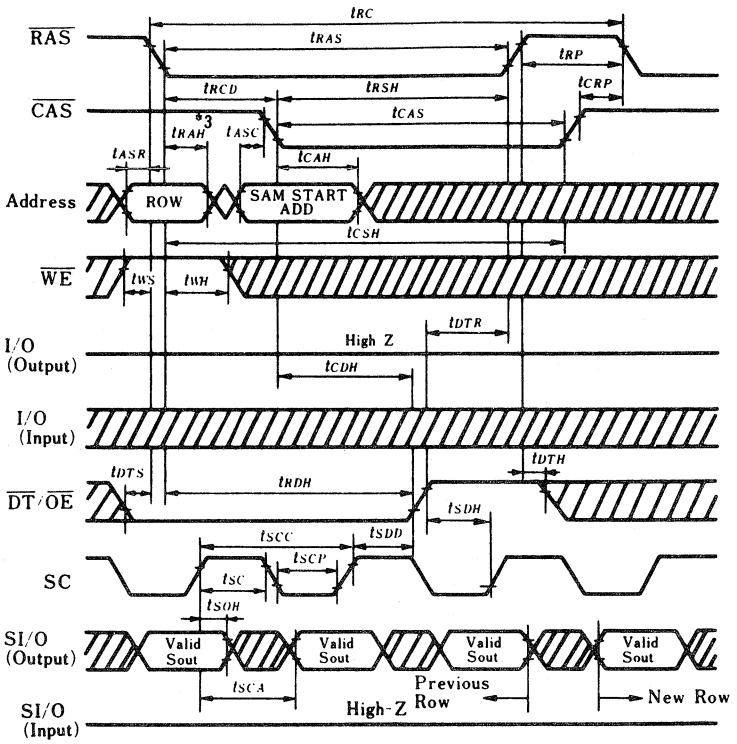
● HIDDEN REFRESH CYCLE (HM53461 Series)



● HIDDEN REFRESH CYCLE (HM53462 Series)



● READ TRANSFER CYCLE (1)*1,*2



Note

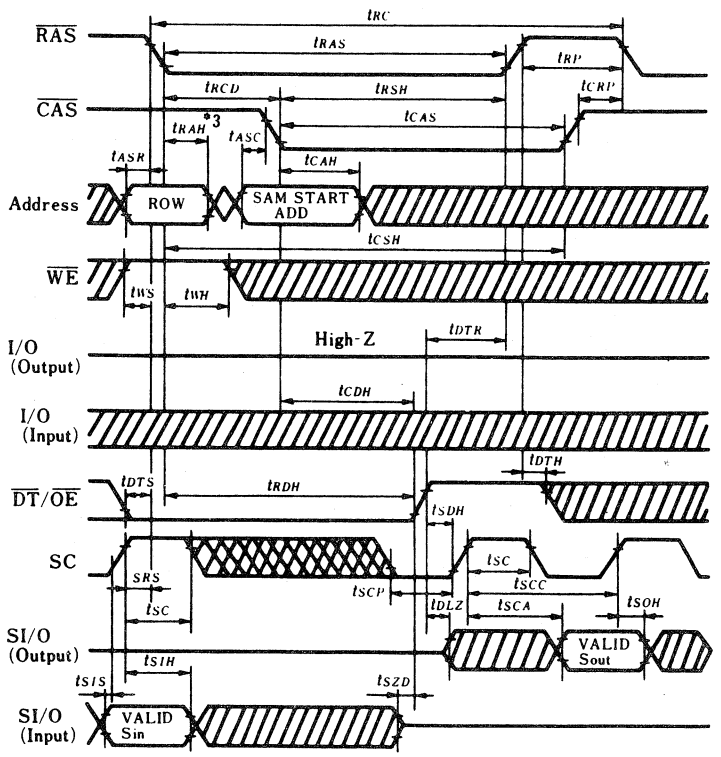
*1) In the case that the previous data transfer cycle was read transfer.

*2) Assume that $\overline{SOE}$ is "L" level.

*3) $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

Do not care

● READ TRANSFER CYCLE (2)*1,*2



Do not care

Inhibit rising transient

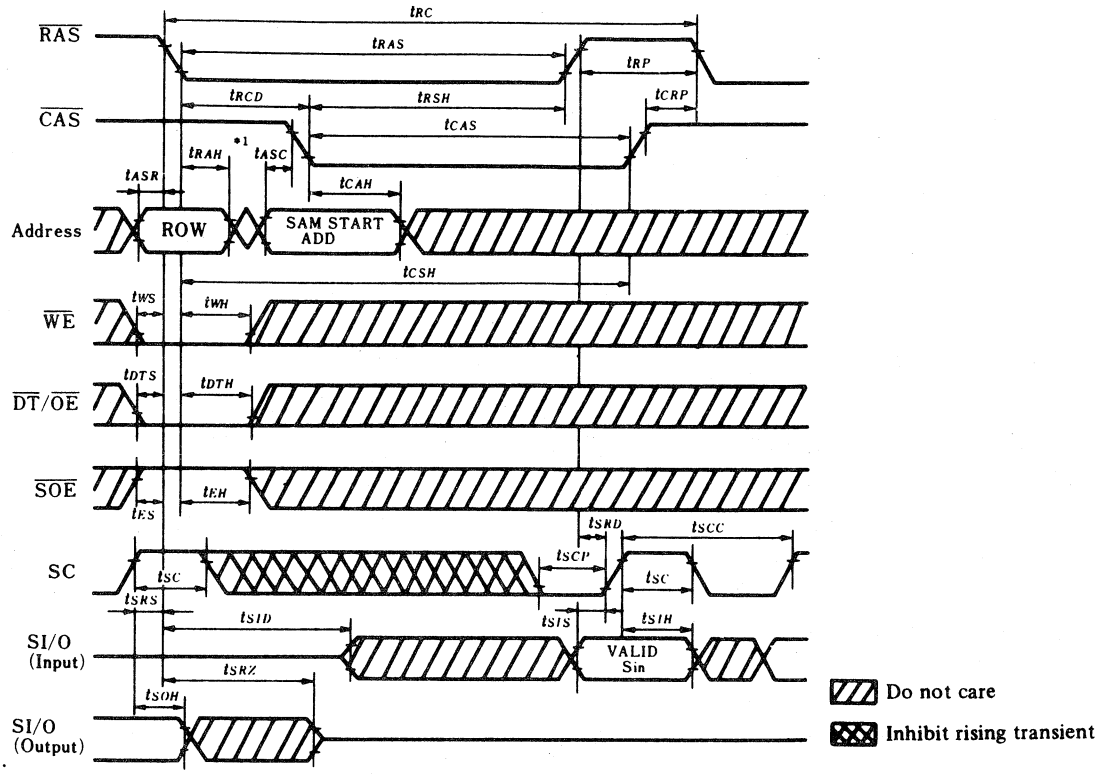
Note)

*1) In the case that the previous data transfer cycle was write transfer or pseudo transfer.

*2) Assume that $\overline{SOE}$ is "L" level,

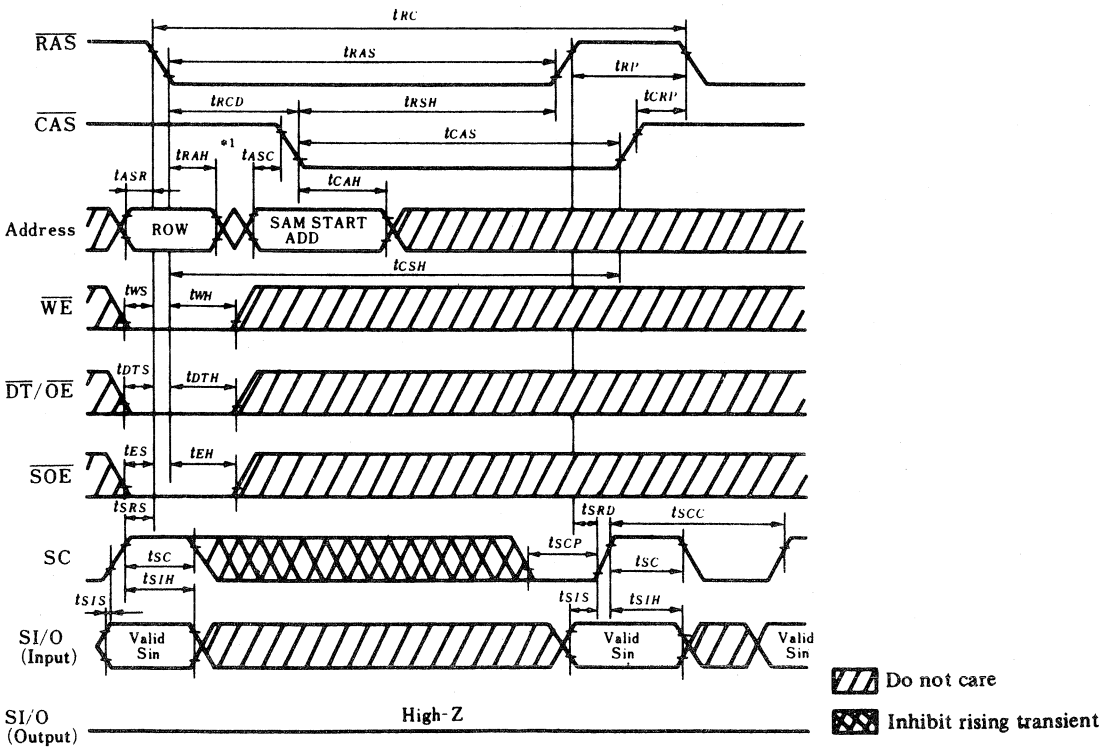
*3) $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• PSEUDO TRANSFER CYCLE



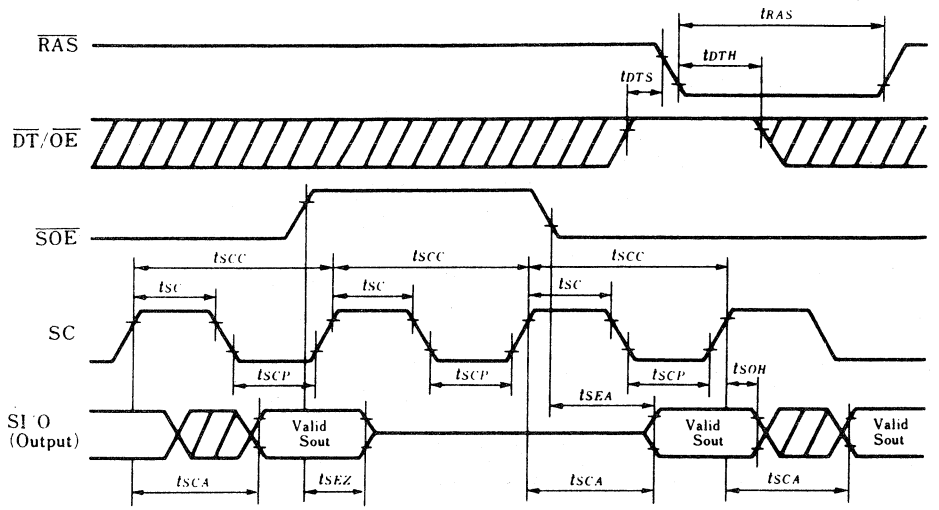
Note) *1. $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• WRITE TRANSFER CYCLE



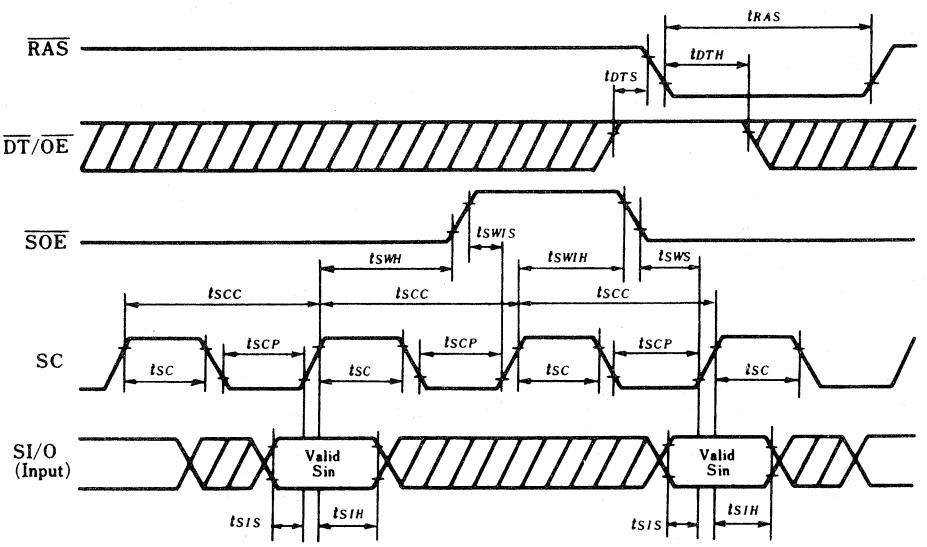
Note) *1. $\overline{CAS}$ and SAM start Address need not be supplied every cycle, only when it is desired to change to a new SAM start Address.

• SERIAL READ CYCLE



Do not care

• SERIAL WRITE CYCLE



Do not care

■ ELECTRICAL AC CHARACTERISTICS (Logic operation mode) (HM53462 Series)

Parameter	Symbol	HM53462-10		HM53462-12		HM53462-15		Unit
		min.	max.	min.	max.	min.	max.	
Write cycle time	t_{FRC}	230	–	265	–	310	–	ns
$\overline{RAS}$ pulse width in write cycle	t_{RFS}	140	10000	165	10000	200	10000	ns
$\overline{CAS}$ pulse width in write cycle	t_{CFS}	80	10000	95	10000	105	10000	ns
$\overline{CAS}$ hold time in write cycle	t_{FCSH}	140	–	165	–	200	–	ns
$\overline{RAS}$ hold time in write cycle	t_{FRSH}	80	–	95	–	105	–	ns
Page mode cycle time (Write cycle)	t_{FPC}	100	–	120	–	135	–	ns
$\overline{CAS}$ hold time (Logic operation set/reset cycle)	t_{FCHR}	90	–	100	–	120	–	ns
$\overline{CAS}$ hold time from $\overline{RAS}$ precharge (x4 → x1 set cycle)	t_{PSCH}	10	–	10	–	10	–	ns

■ LOGIC CODE (FC0 – 3 are AX0 – AX3 in Logic Operation Set Cycle) (HM53462 Series)

FC3	FC2	FC1	FC0	LOGIC	
				Symbol	Write Data
0	0	0	0	0	Zero
0	0	0	1	AND1	Di · Mi
0	0	1	0	AND2	$\overline{Di}$ · Mi
0	0	1	1	X4 →X1	–
0	1	0	0	AND3	Di · $\overline{Mi}$
0	1	0	1	THROUGH	Di
0	1	1	0	EOR	$\overline{Di}$ · Mi + Di · $\overline{Mi}$
0	1	1	1	OR1	Di + Mi
1	0	0	0	NOR	$\overline{Di}$ · $\overline{Mi}$
1	0	0	1	ENOR	Di · Mi + $\overline{Di}$ · $\overline{Mi}$
1	0	1	0	INV1	$\overline{Di}$
1	0	1	1	OR2	$\overline{Di}$ + Mi
1	1	0	0	INV2	$\overline{Mi}$
1	1	0	1	OR3	Di + $\overline{Mi}$
1	1	1	0	NAND	$\overline{Di}$ + $\overline{Mi}$
1	1	1	1	1	ONE

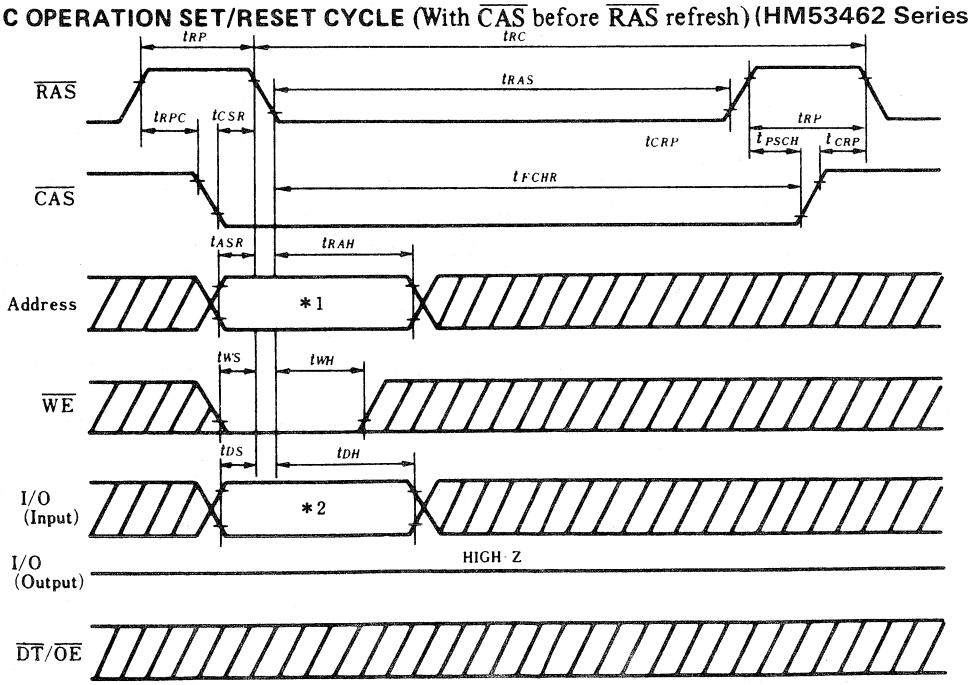
→ SAM organization changes to 1024 x 1

→ Logic operation mode reset

Di : External Data-in

Mi : The data of the memory cell

● LOGIC OPERATION SET/RESET CYCLE (With $\overline{CAS}$ before $\overline{RAS}$ refresh) (HM53462 Series)



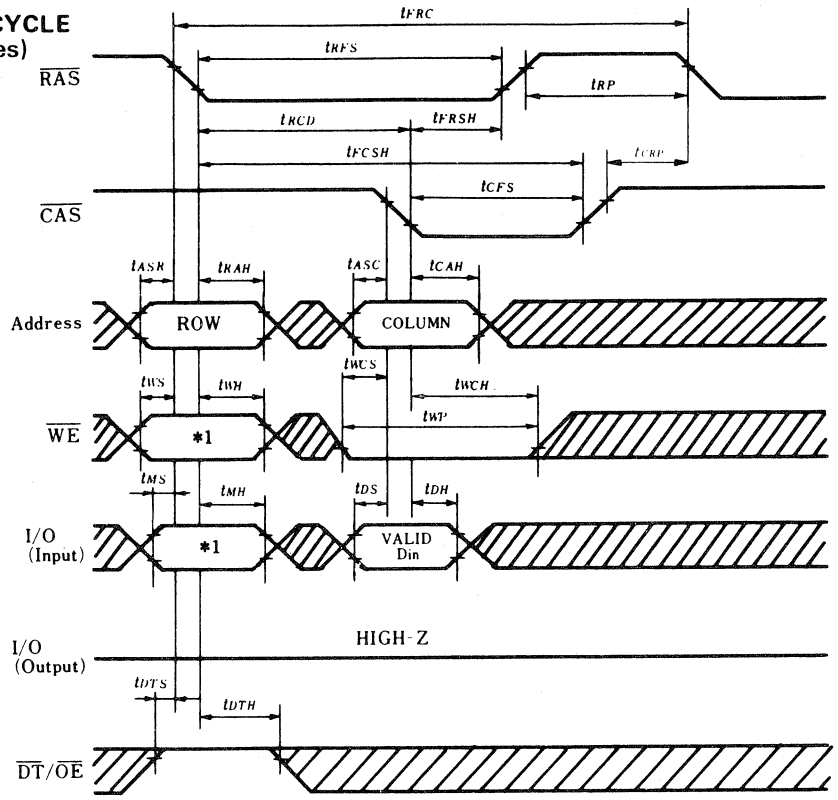
*1) Logic code A0-A3 (A4-A7: don't care)

*2) Write mask data

▨ Do not care

■ LOGIC OPERATION MODE

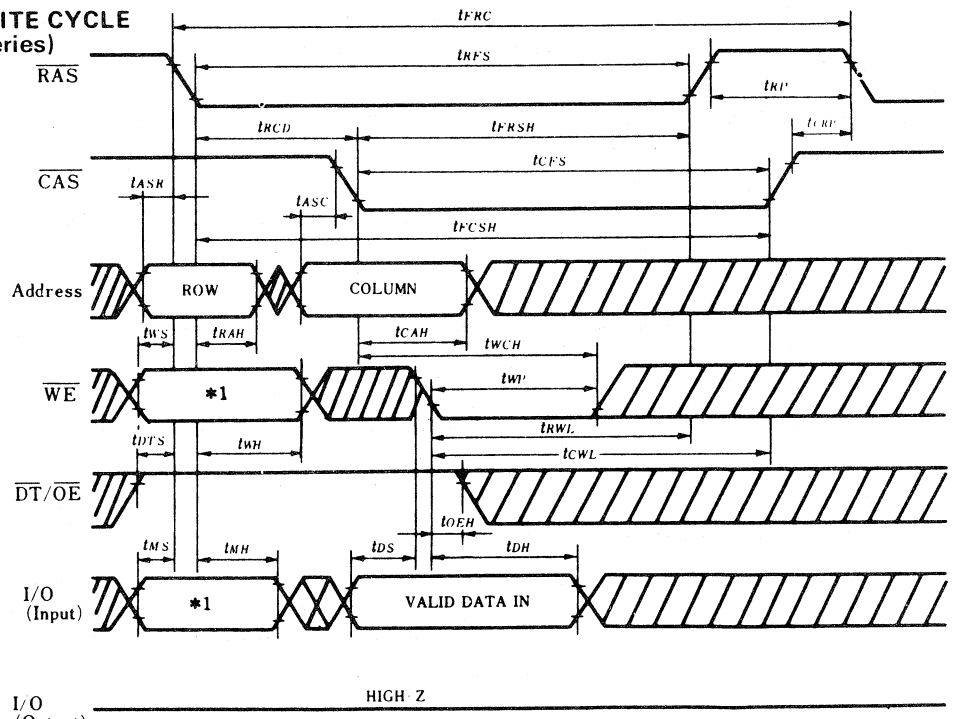
● EARLY WRITE CYCLE (HM53462 Series)



Note) *1. When $\overline{WE}$ is 'high', the all data on the I/O can be written into the cell.
When $\overline{WE}$ is 'low', the data on the I/O are not written except for when I/O is 'high' at the falling edge of $\overline{RAS}$.

▨ Do not care

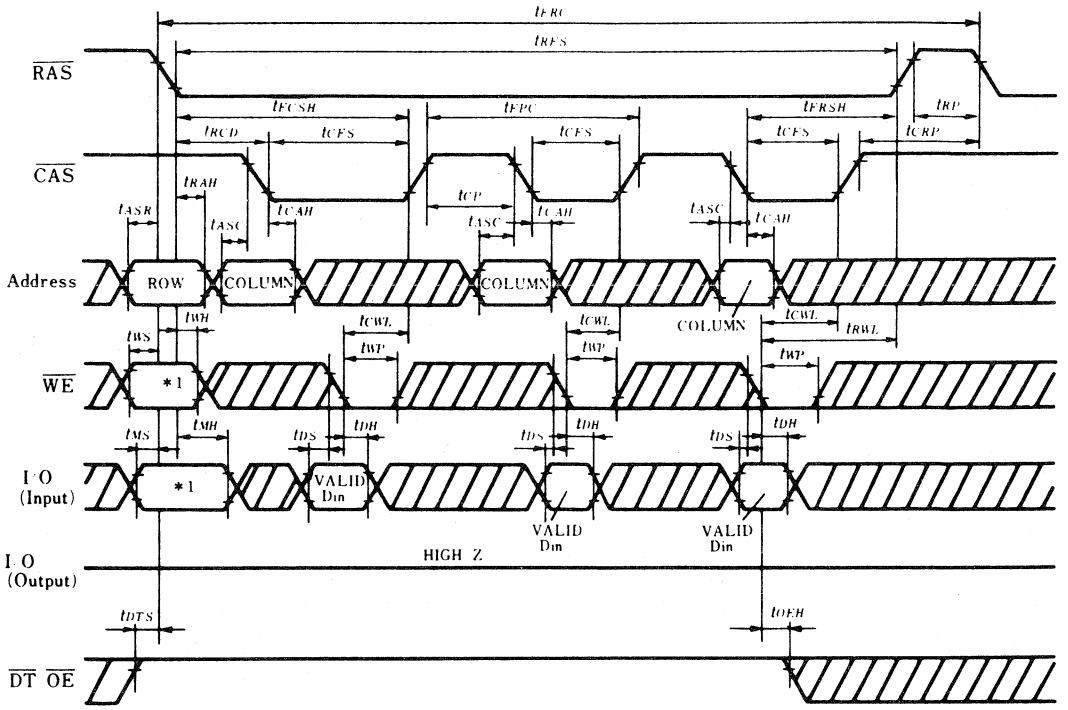
● DELAYED WRITE CYCLE (HM53462 Series)



NOTE 1) When $\overline{WE}$ is "H" level, all the data on I/01-4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

▨ Do not care

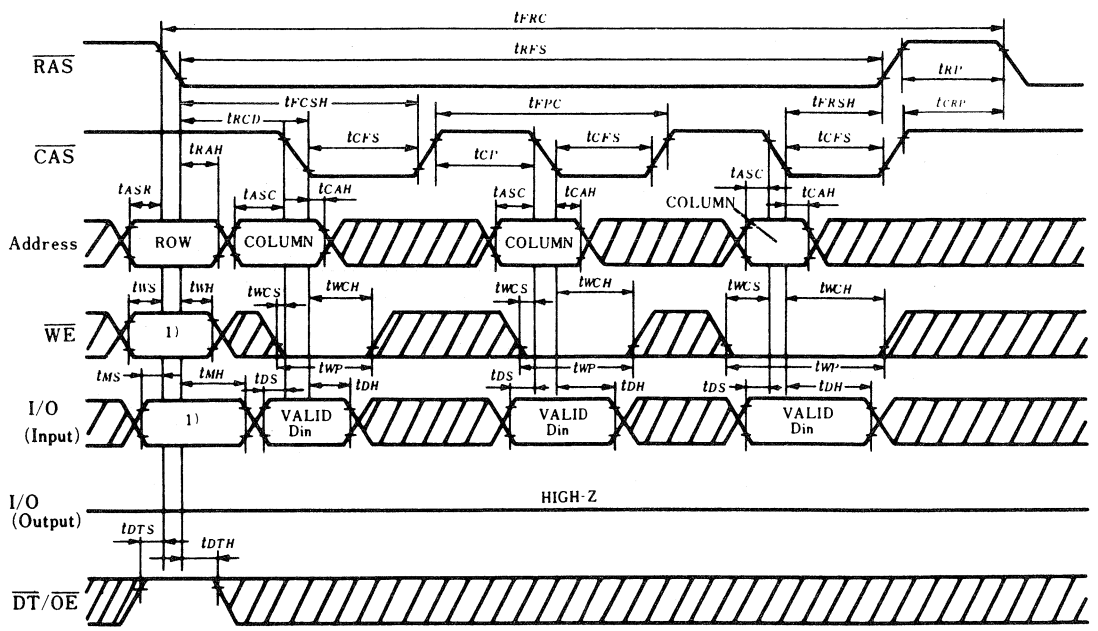
• PAGE MODE WRITE CYCLE (Delayed Write) (HM53462 Series)



Do not care

Note) *1. When $\overline{WE}$ is 'high', the all data on the I/O can be written into the cell.
When $\overline{WE}$ is 'low', the data on the I/O are not written except for when I/O is 'high' at the falling edge of $\overline{RAS}$.

• PAGE MODE WRITE CYCLE (Early Write) (HM53462 Series)



Do not care

Note) *1. When $\overline{WE}$ is 'high', the all data on the I/O can be written into the cell.
When $\overline{WE}$ is 'low', the data on the I/O are not written except for when I/O is 'high' at the falling edge of $\overline{RAS}$.

■ DESCRIPTION (HM53462 Series)

1. LOGIC OPERATION MODE

HM53462 has an internal logic operation unit which makes a process of graphics simple. The logic is determined in "Logic operation set/reset cycle", and the operation is executed in every write cycle succeeding to the logic operation set/reset cycle. In this mode the internal read-modify-write operation is executed and the cell data is converted into the new data given by the logic operation between Din and the old cell data.

2. LOGIC OPERATION SET/RESET CYCLE

A logic operation set/reset cycle is performed by bringing $\overline{CAS}$ and $\overline{WE}$ low when $\overline{RAS}$ falls (Fig. 1). The logic code and the bits to be masked are datermined respectively by Ax0-3 state and I/01-4 state at the falling edge of $\overline{RAS}$. Furthermore, in this cycle $\overline{CAS}$ – before – $\overline{RAS}$ refresh operation is executed, too. In the case of executing the conventional $\overline{CAS}$ – before – $\overline{RAS}$ refresh operation, $\overline{WE}$ must be high when $\overline{RAS}$ falls.

2.1. Logic code

The logic code is shown in Table 1. When power is turned on, at least one logic reset cycle including write mask reset is required to initialize logic code. If the logic code is (Ax3, Ax2, Ax1, Ax0) = (0, 0, 1, 1), the SAM organization is changed converter (Fig. 2). In the case that the SAM organization is changed to 1,024 x 1, one data transfer cycle is needed to initialie the SAM selector.

Once the SAM organization is changed to 1024 x 1, this code is maintained unless power is turned off.

2.2. Write mask

HM53462 has two kinds of mask registers (register 1, 2). The register 1 is set by bringing $\overline{WE}$ low at the falling edge of $\overline{RAS}$ during the write cycle, and the mask data is available only in this cycle. The register 2 is set by level of I/O in the logic operation set/reset cycle, and the mask data is available until the next logic operation set/reset cycle. If the register 1 is set during the current logic operation mode, the mask data of the register 1 is preferred (that of the register 2 is ignored) and the logic becomes "THROUGH" only in this cycle (Fig. 3).

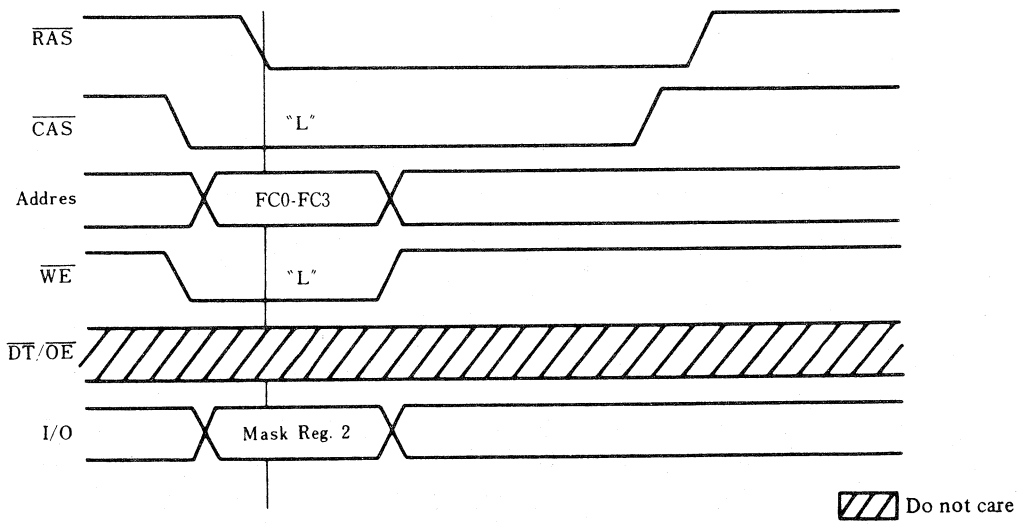


Fig. 1 LOGIC OPERATION SET/RESET CYCLE

Table 1. LOGIC CODE (FC0 – FC3 are AX0 – AX3 in Logic Operation Set Cycle)

FC3	FC2	FC1	FC0	LOGIC	
				Symbol	Write Data
0	0	0	0	0	Zero
0	0	0	1	AND1	$Di \cdot Mi$
0	0	1	0	AND2	$\overline{Di} \cdot Mi$
0	0	1	1	X4 →X1	–
0	1	0	0	AND3	$Di \cdot \overline{Mi}$
0	1	0	1	THROUGH	Di
0	1	1	0	EOR	$\overline{Di} \cdot Mi + Di \cdot \overline{Mi}$
0	1	1	1	OR1	$Di + Mi$
1	0	0	0	NOR	$\overline{Di} \cdot \overline{Mi}$
1	0	0	1	ENOR	$Di \cdot Mi + \overline{Di} \cdot \overline{Mi}$
1	0	1	0	INV1	$\overline{Di}$
1	0	1	1	OR2	$\overline{Di} + Mi$
1	1	0	0	INV2	$\overline{Mi}$
1	1	0	1	OR3	$Di + \overline{Mi}$
1	1	1	0	NAND	$\overline{Di} + \overline{Mi}$
1	1	1	1	1	ONE

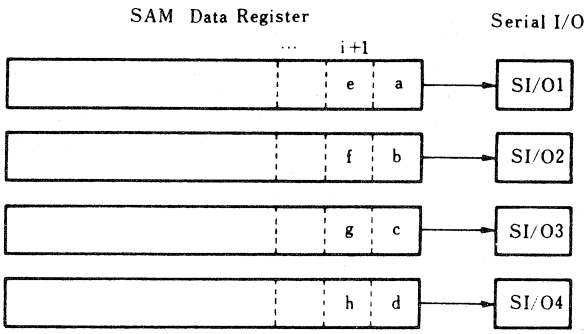
→ SAM organization changes to 1024 x 1

→ Logic operation mode reset

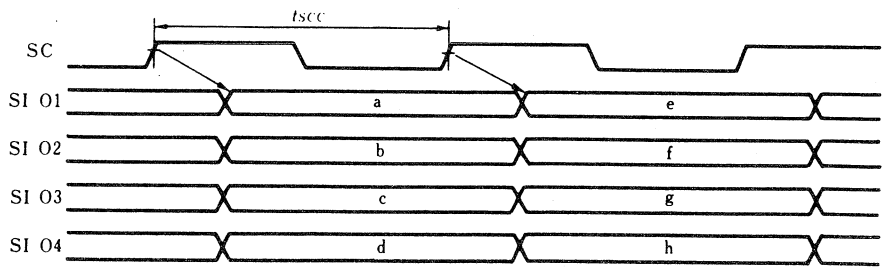
Di : External Data-in

Mi : The data of the memory cell

Fig. 2 THE SHIFT WAY OF SAM DATA



1) By 4 mode (SAM organization: 256 x 4)



2) By 1 mode (SAM organization: 1024 x 1)

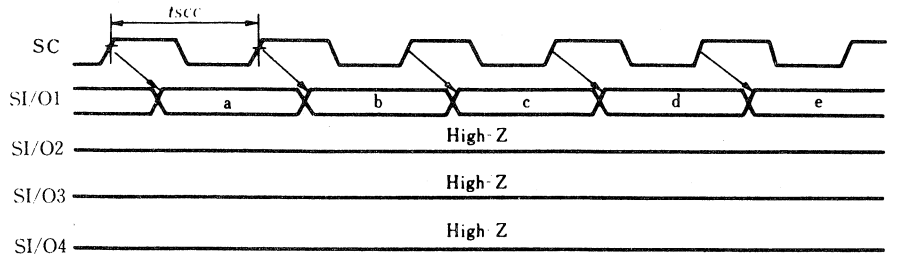


Fig. 3 EXAMPLE OF LOGIC OPERATION MODE

	Logic operation set/reset cycle	Write cycle	Write cycle	Write cycle	Write cycle
$\overline{RAS}$					
$\overline{CAS}$	"L"	"H"	"H"	"H"	"H"
$\overline{WE}$	"L"	"H"	"L"	"H"	"H"
I/O1		"0" Write	Masked	"1" Write	"0" Write
I/O2		Masked	"1" Write	Masked	Masked
I/O3		Masked	"0" Write	Masked	Masked
I/O4		"1" Write	Masked	"0" Write	"1" Write
Logic	—	AND1	THROUGH	AND1	AND1
	Mask reg.2 is set I/O 2,3 :Masked Assume that the logic is set to "AND1".		Mask reg.1 is set, and valid only in this cycle. I/O1,4:Masked		

HM534251 Series
HM534252 Series

262144-Word × 4-Bit Multiport CMOS Video RAM

The HM534251/HM534252 is a 1-Mbit multiport video RAM equipped with a 256-kword x 4-bit dynamic RAM and a 512-word x 4-bit SAM (serial access memory).

Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has a write mask function. It is suitable for a graphic processing buffer memory.

HM534252 also provides logic operation mode to simplify its operation. In this mode, logic operation between memory data and input data can be executed by using internal logic-arithmetic unit.

Features

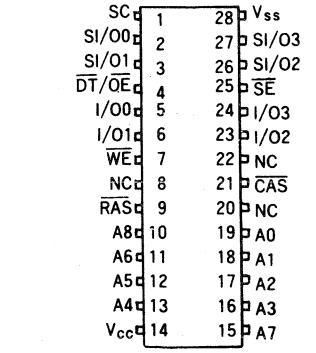
- Multiport organization
  - Asynchronous and simultaneous operation of RAM and SAM capability
  - RAM: 256-kword x 4-bit and SAM: 512-word x 4-bit
- Access time RAM: 100 ns/100 ns/120 ns/150 ns max
  SAM: 30 ns/35 ns/40 ns/50 ns max
- Cycle time RAM: 190 ns/190 ns/220 ns/260 ns min
  SAM: 30 ns/40 ns/40 ns/60 ns min
- Low power
  - Active RAM: 385 mW max
    SAM: 358 mW max
  - Standby 40 mW max
- High-speed page mode capability
- Logic operation mode capability (HM534252 Series)
- 2 types of mask write mode capability (HM534252 Series)
- Mask write mode capability (HM534251 Series)
- Bidirectional data transfer cycle between RAM and SAM capability
- Real time read transfer capability
- 3 variations of refresh (8 ms/512 cycles)
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access Time	Package
HM534251JP-10	100 ns	400-mil
HM534251JP-11	100 ns	28-pin
HM534251JP-12	120 ns	Plastic SOJ (CP-28D)
HM534251JP-15	150 ns	
HM534251ZP-10	100 ns	400-mil
HM534251ZP-11	100 ns	28-pin
HM534251ZP-12	120 ns	Plastic ZIP (ZP-28)
HM534251ZP-15	150 ns	
HM534252JP-10	100 ns	400-mil
HM534252JP-11	100 ns	28-pin
HM534252JP-12	120 ns	Plastic SOJ (CP-28D)
HM534252JP-15	150 ns	
HM534252ZP-10	100 ns	400-mil
HM534252ZP-11	100 ns	28-pin
HM534252ZP-12	120 ns	Plastic ZIP (ZP-28)
HM534252ZP-15	150 ns	

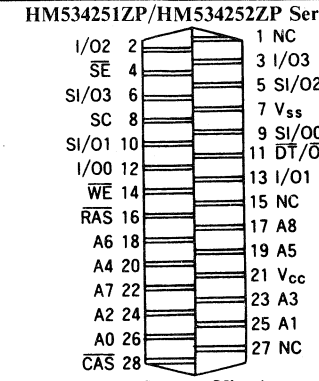
Pin Arrangement

HM534251JP/HM534252JP Series



(Top View)

HM534251ZP/HM534252ZP Series

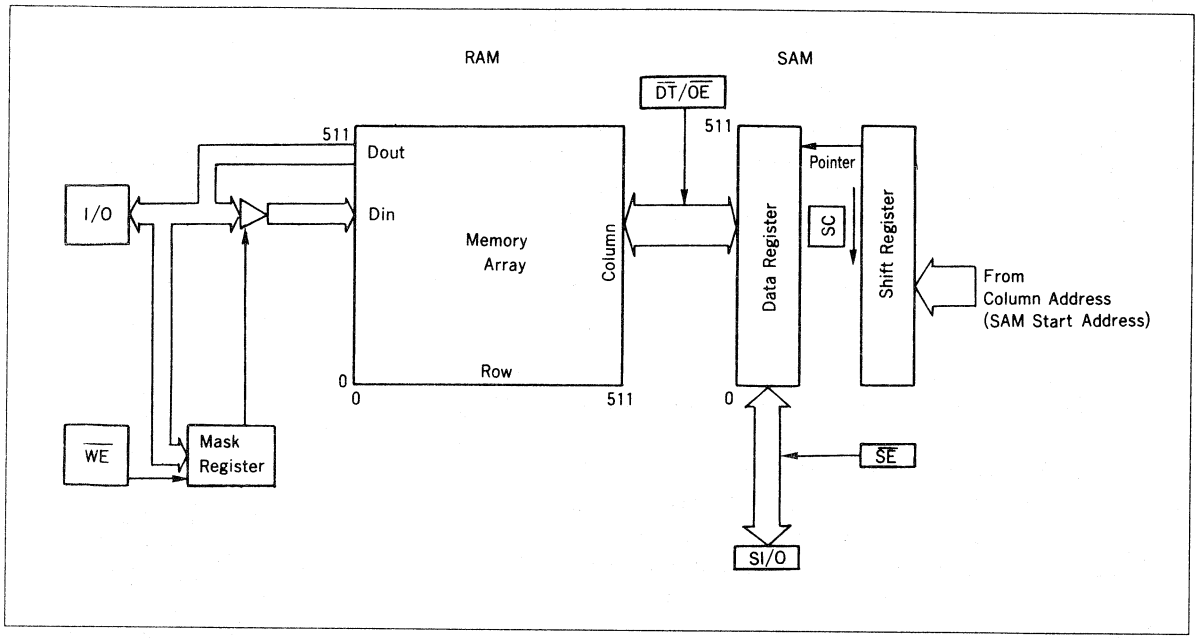


(Bottom View)

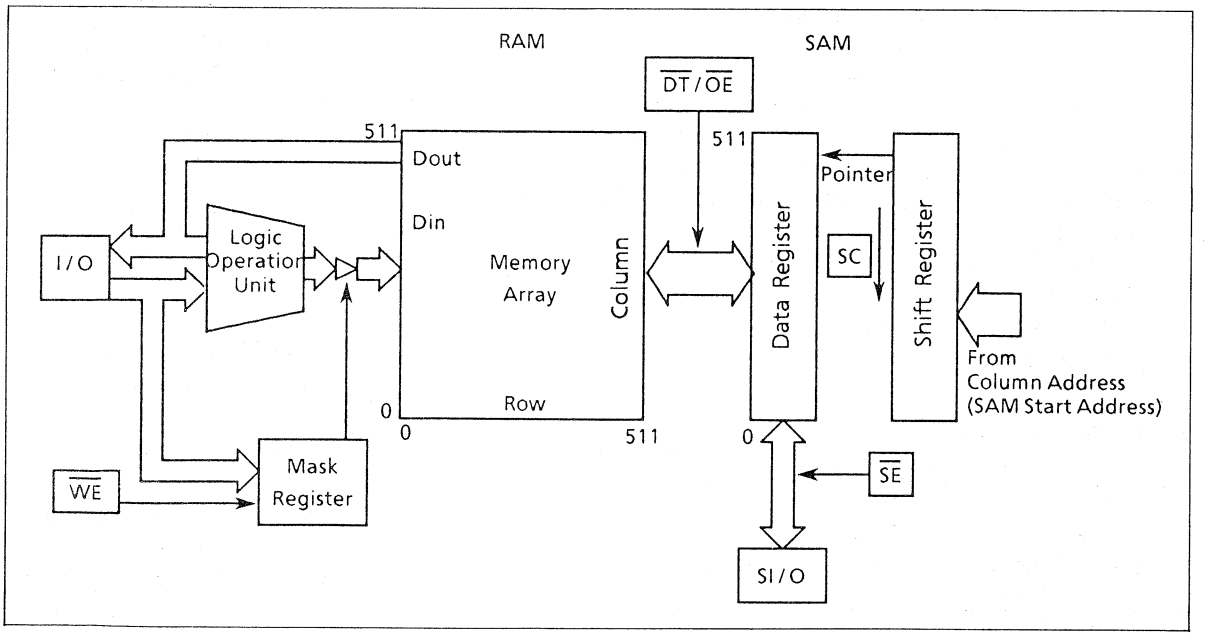
Pin Description

Pin Name	Function
A0–A8	Address inputs
I/O0–I/O3	RAM port data inputs/outputs
SI/O0–SI/O3	SAM port data inputs/outputs
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{CAS}}$	Column address strobe
$\overline{\text{WE}}$	Write enable
$\overline{\text{DT/OE}}$	Data transfer/Output enable
SC	Serial clock
$\overline{\text{SE}}$	SAM port enable
Vcc	Power supply
Vss	Ground
NC	No connection

Block Diagram (HM534251 Series)



Block Diagram (HM534252 Series)



Pin Function

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of those signals determine the operation cycle of the HM534251/HM534252.

Table 1. Operation Cycles of the HM534251/HM534252

Input level at the falling edge of $\overline{RAS}$				Operation Cycle
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	$\overline{SE}$	
H	H	H	×	RAM read/write
H	H	L	×	Mask write
H	L	H	×	Read transfer
H	L	L	H	Pseudo transfer
H	L	L	L	Write transfer
L	×	×	×	CBR refresh (HM534251 Series)
L	×	H	×	CBR refresh (HM534252 Series)
L	×	L	×	Logic operation set/reset (HM534252 Series)

Note: ×; Don't care.

$\overline{CAS}$ (input pin): Column address is put into chip at the falling edge of $\overline{CAS}$. $\overline{CAS}$ controls output impedance of I/O in RAM.

A0–A8 (input pins): Row address is determined by A0–A8 level at the falling edge of $\overline{RAS}$. Column address is determined by A0–A8 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM534251/HM534252 turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read /write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O0–I/O3 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only on high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data is output from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is put into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not put into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O0–SI/O3 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

Operation of HM534251/HM534252

Operation of RAM Port

RAM Read Cycle

($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high, at the falling edge of $\overline{RAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data is output through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle
(Early Write, Delayed Write, Read-Modify-Write)
($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

- Normal Mode Write Cycle
  ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after $\overline{RAS}$ is set low, a write cycle is executed and I/O data is written at the selected addresses. When all 4 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes high impedance. Data is entered at the $\overline{CAS}$ falling edge.

If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling edge. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables write after read to execute in the same address cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and setting $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is preserved. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode cycle, the mask data is preserved during the page access.

High-Speed Page Mode Cycle
($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle and is higher than the standard page mode cycle by 70–80%. This product is based on static column mode, therefore, address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 512-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 µs) and t_{RFSP} max (100µs). (t_{RFSP} is specified only for HM534252 series)

Transfer Operation

The HM534251/HM534252 provides the read transfer cycle, pseudo transfer cycle, and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$.

They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)

(2) Determine direction of data transfer
  (a) Read transfer cycle: RAM → SAM
  (b) Write transfer cycle: RAM ← SAM

(3) Determine input or output of SAM I/O pin (SI/O)
  Read transfer cycle: SI/O output
  Pseudo transfer cycle, write transfer cycle: SI/O input

(4) Determine first SAM address to access (SAM start address) after transferring at column address.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by setting $\overline{DT}/\overline{OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address data (512x4 bit) determined by this cycle is transferred synchronously at the rising edge of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address determined by column address.

This cycle can execute SAM access serially even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) is specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge, and t_{SDH}(min) between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge (see figure 1).

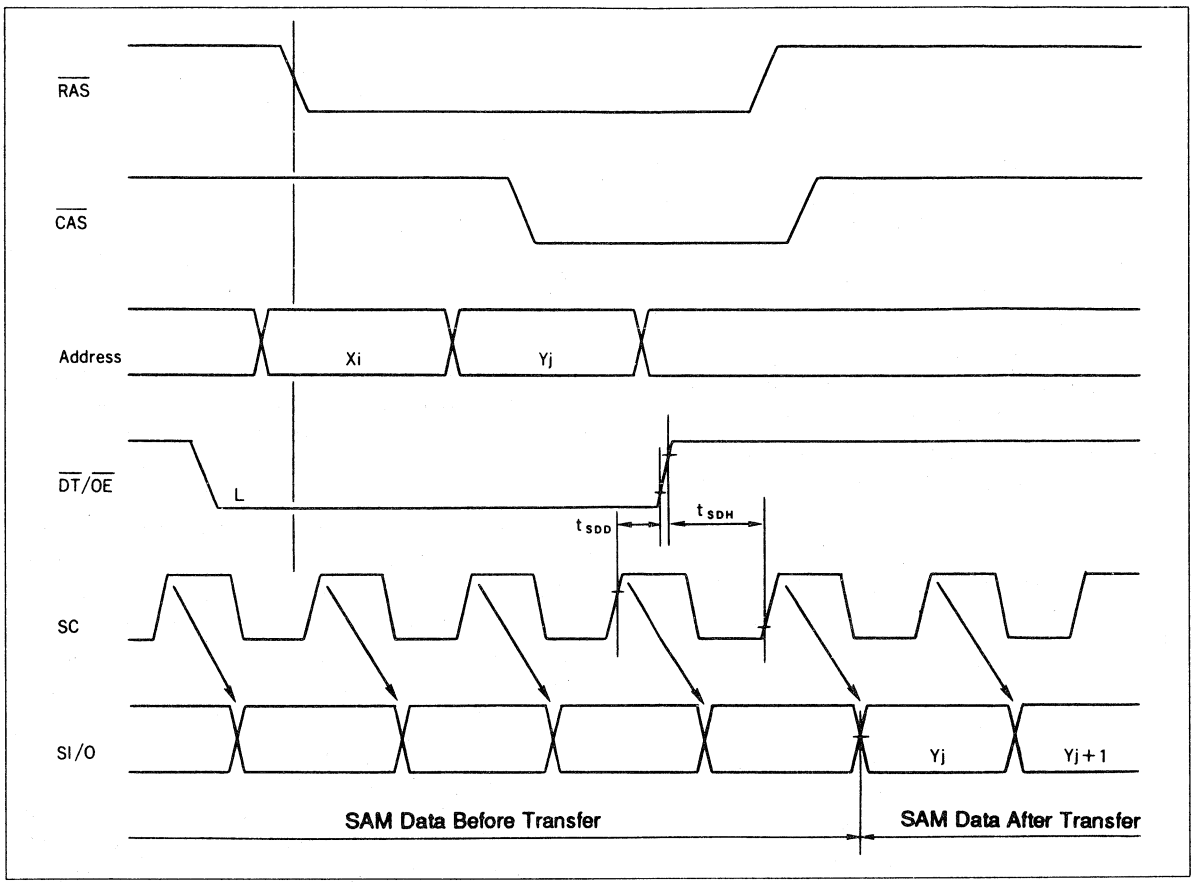


Figure 1. Real Time Read Transfer

If read transfer cycle is executed, SI/O becomes output state. When the previous transfer cycle is either pseudo transfer cycle or write transfer cycle and SI/O is in input state, uncertain data outputs after t_{RLZ} (min) after the $\overline{RAS}$ falling edge. Before that, input should be set high impedance to avoid data contention.

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle is available for switching SI/O from output state to input state because data in RAM isn't rewritten. This cycle starts when $\overline{CAS}$ is high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high, at the falling edge of $\overline{RAS}$. The output buffer in SI/O becomes high impedance within t_{SRZ} (max) from the $\overline{RAS}$ falling edge. Data should be input to SI/O later than t_{SID} (min) to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC should not be raised.

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address to serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC should not be raised.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. If $\overline{SE}$ is set high SI/O becomes high impedance and internal pointer is incremented at the SC rising edge.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is programmed into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't input into data resister. Internal pointer is incremented according to the SC rising edge, so $\overline{SE}$ high can mask data for SAM.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is performed by accessing all 512 row addresses every 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required for accessing all row addresses every 8 ms.

$\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is performed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high by inputting the row address (= refresh address) from external circuits. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ should be high at the falling edge of $\overline{RAS}$.

CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate. (HM534251 Series)

CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate. To distinguish this cycle from logic operation set/reset cycle, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$. (HM534252 Series)

Hidden Refresh Cycle: Hidden refresh cycle performs refresh by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register, selector), organized as fully static circuitry, don't require refresh.

Logic Operation Mode (HM534252 Series)

The HM534252 supports logic operation capability on RAM port. It performs logic operations between the memory cell data and input data in logic operation mode cycle, and writes the result into the memory cell (read modify write). This function realizes high speed raster operations and simplifies peripheral circuits for raster operations.

Logic Operation Set/Reset Cycle ($\overline{CAS}$ and $\overline{WE}$ Low at the falling edge of $\overline{RAS}$)

In logic operation set/reset cycle, the following operations are performed at the same time; 1. Selection of logic operations and logic operation mode set/reset, 2. Mask data programming, 3. $\overline{CAS}$-before-$\overline{RAS}$ refresh.

Figure 2 shows the timing for logic operation set/reset cycle. This cycle starts when $\overline{CAS}$ and $\overline{WE}$ are low at the falling edge of $\overline{RAS}$. In this cycle, logic operation codes and mask data are programmed by row address and I/O pin at the falling edge of $\overline{RAS}$ respectively. When write cycle is performed after this cycle, the logic operation write cycle starts. In the logic operation mode, the specification of cycle time is longer than that of normal mode because read-modify-write cycle is performed internally. In this cycle, logic operation codes and mask data programmed are available until reprogrammed. In normal mode, mask data is available only for one $\overline{RAS}$ cycle. Here, the mask data programmed in normal mode is named as "temporary mask data" and the one programmed in logic operation set/reset cycle is named as "mask data".

(1) Selection of logic operations and logic operation mode set/reset

Table 2 shows the logic operations. One operation is selected among sixteen ones by combinations of A0-A3 levels at the falling edge of $\overline{RAS}$. (A4–A8 are Don't care.) Logic operation codes (A3, A2, A1, A0) = (0,1,0,1) resets the logic operation mode. When write cycle is performed after that, normal write cycle starts. However, even in this case, mask data is still available. I/O should be at high level at the falling edge of $\overline{RAS}$ in logic operation set/reset cycle when mask data is not used.

(2) Mask data programming

High/low level of I/O at the falling edge of $\overline{RAS}$ functions as mask data. When I/O is high, the data is written in write cycle. When I/O is low, the input data is masked and the same memory cell data remains. Mask data, programmed in this cycle, is available until reprogrammed. It is advantageous when the same mask data continues.

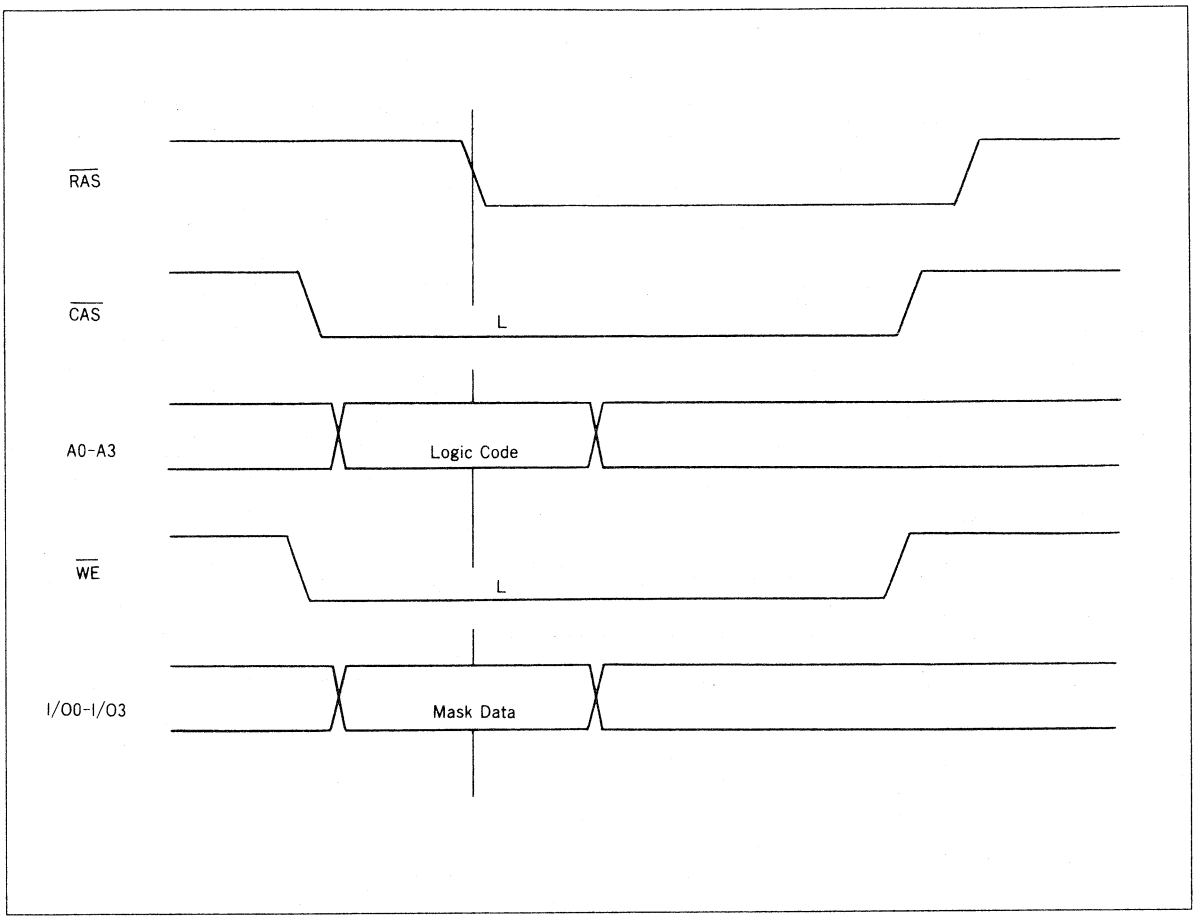


Figure 2. Logic Operation Set/Reset

Table 2. Logic Code

Logic Code				Symbol	Write Data	Note
A3	A2	A1	A0			
0	0	0	0	Zero	0	
0	0	0	1	AND1	$\overline{Di} \cdot Mi$	
0	0	1	0	AND2	$Di \cdot \overline{Mi}$	Logic operation mode set
0	0	1	1	—	Mi	
0	1	0	0	AND3	$Di \cdot \overline{Mi}$	
0	1	0	1	THROUGH	Di	Logic operation mode reset
0	1	1	0	EOR	$\overline{Di} \cdot Mi + Di \cdot \overline{Mi}$	
0	1	1	1	OR1	$\overline{Di} + Mi$	
1	0	0	0	NOR	$\overline{Di} \cdot \overline{Mi}$	
1	0	0	1	ENOR	$Di \cdot Mi + \overline{Di} \cdot \overline{Mi}$	
1	0	1	0	INV1	$\overline{Di}$	Logic operation mode set
1	0	1	1	OR2	$\overline{Di} + Mi$	
1	1	0	0	INV2	$\overline{Mi}$	
1	1	0	1	OR3	$Di + \overline{Mi}$	
1	1	1	0	NAND	$\overline{Di} + \overline{Mi}$	
1	1	1	1	One	1	

Notes: Di; External data-in
Mi; The data of the memory cell

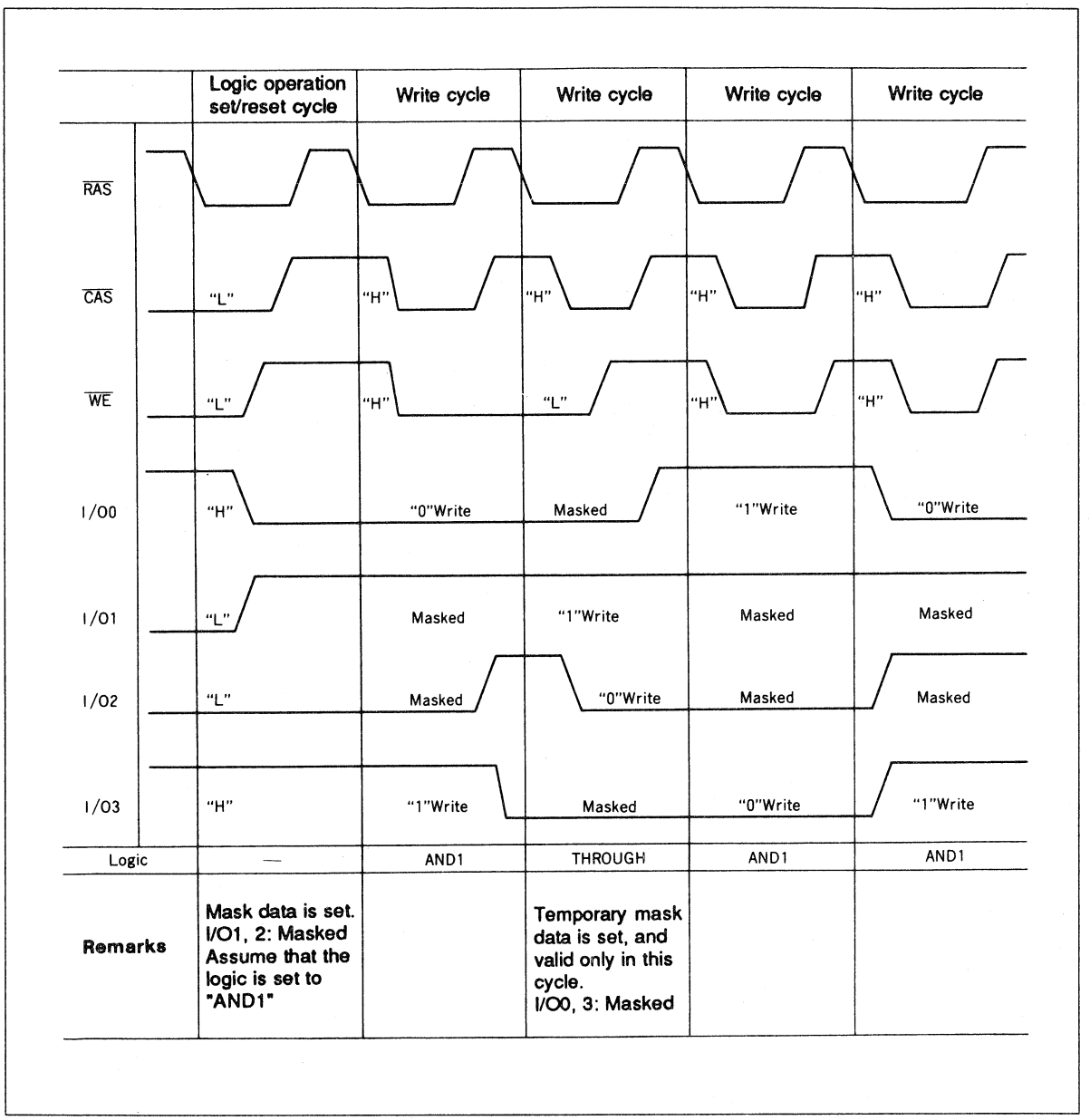


Figure 3. 2 Types of Mask Write Function and Logic Operation Function

Also, temporary mask data is programmed by falling $\overline{WE}$ at the falling edge of $\overline{RAS}$ in logic operation mode cycle after mask data is programmed in logic operation set/reset cycle. In this case, temporary mask data is available only for one cycle.

Logic operation is reset during temporary mask write cycle. It means that external input data is written into I/O when temporary mask data is set. Figure 4 shows write mask and logic operations. These functions are useful when RAM port is devided into frame buffer area and data area, as they save the need to reprogram logic operation codes and mask data.

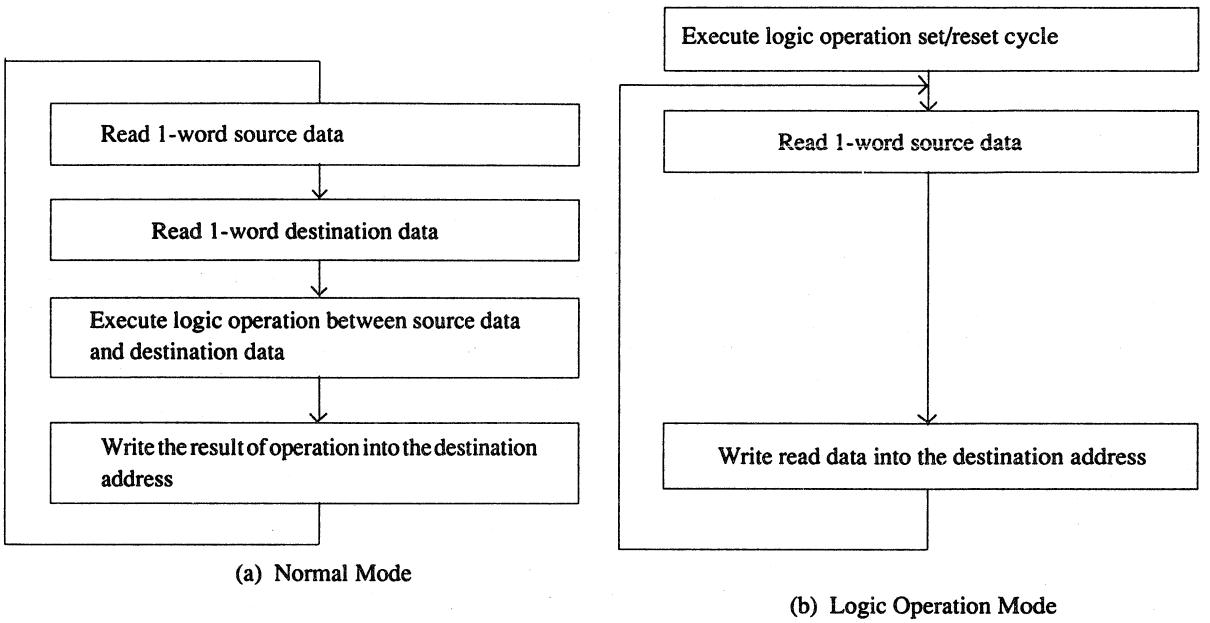
Write Cycle in Logic Operation Mode (Early Write, Delayed Write, Page Mode)

Write cycle after logic operation set cycle is logic operation mode cycle. In this cycle, the following read-modify-write operation is performed Internally.

(1) Reading memory data in given address into internal bus.

2) Performing operation between input data and memory data

(3) Writing the result of (2) into address given by (1)



(a) Normal Mode

(b) Logic Operation Mode

Figure 4. Sequence of Raster Operation

Figure 4 shows sequence of raster operation. Raster operation which needs 3 cycles (destination read, operation, destination write) in normal mode can be executed in one write cycle of logic operation mode. It makes raster operation faster and simplifies peripheral hardware for raster operation.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage *1	V_T	−1.0 to +7.0	V
Power supply voltage *1	V_{CC}	−0.5 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Note: *1. Relative to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage *1	V_{CC}	4.5	5.0	5.5	V
Input high voltage *1	V_{IH}	2.4	—	6.5	V
Input low voltage *1	V_{IL}	−0.5*2	—	0.8	V

Notes: *1. All voltages referenced to V_{SS}.
*2. −3.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Item	Symbol	HM534251-10 HM534252-10		HM534251-11 HM534252-11		HM534251-12 HM534252-12		HM534251-15 HM534252-15		Unit	Test Conditions		Note
		Min	Max	Min	Max	Min	Max	Min	Max		RAM port	SAM port	
Operating current	I_{CC1}	—	70	—	70	—	60	—	55	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	*1, *2
	I_{CC7}	—	120	—	120	—	100	—	85	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min	
Standby current	I_{CC2}	—	7	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}	*1, *4
	I_{CC8}	—	65	—	55	—	55	—	40	mA		$\overline{SE}$=V_{IL}, SC cycling t_{SCC} = Min	
$\overline{RAS}$-only refresh current	I_{CC3}	—	70	—	70	—	60	—	55	mA	$\overline{RAS}$ cycling $\overline{CAS}$ =V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}	*2
	I_{CC9}	—	120	—	120	—	100	—	85	mA	t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min	
Page mode current	I_{CC4}	—	80	—	80	—	70	—	60	mA	$\overline{CAS}$ cycling $\overline{RAS}$ = V_{IL}	SC = V_{IL}, $\overline{SE}$ = V_{IH}	*1, *3
	I_{CC10}	—	130	—	130	—	110	—	90	mA	t_{PC} = Min	$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min	
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	—	60	—	60	—	50	—	40	mA	$\overline{RAS}$ cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC11}	—	110	—	110	—	90	—	70	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min	
Data transfer current	I_{CC6}	—	95	—	95	—	90	—	85	mA	$\overline{RAS}$, $\overline{CAS}$ cycling	SC = V_{IL}, $\overline{SE}$ = V_{IH}	*2
	I_{CC12}	—	135	—	135	—	125	—	115	mA	t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min	
Input leakage current	I_{LI}	−10	10	−10	10	−10	10	−10	10	µA			
Output leakage current	I_{LO}	−10	10	−10	10	−10	10	−10	10	µA			
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V	I_{OH} = −2 mA		
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V	I_{OL} = 4.2 mA		

Notes: *1. I_{CC} depends on output loading condition when the device is selected.
I_{CC} max is specified at the output open condition.
*2. Address can be changed less than three times while one $\overline{RAS}$ cycle.
*3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
*4. Address must be fixed.

Capacitance (Ta = 25°C, V_{CC} = 5 V, f = 1MHz, Bias: Clock, I/O = V_{CC}, address = V_{SS})

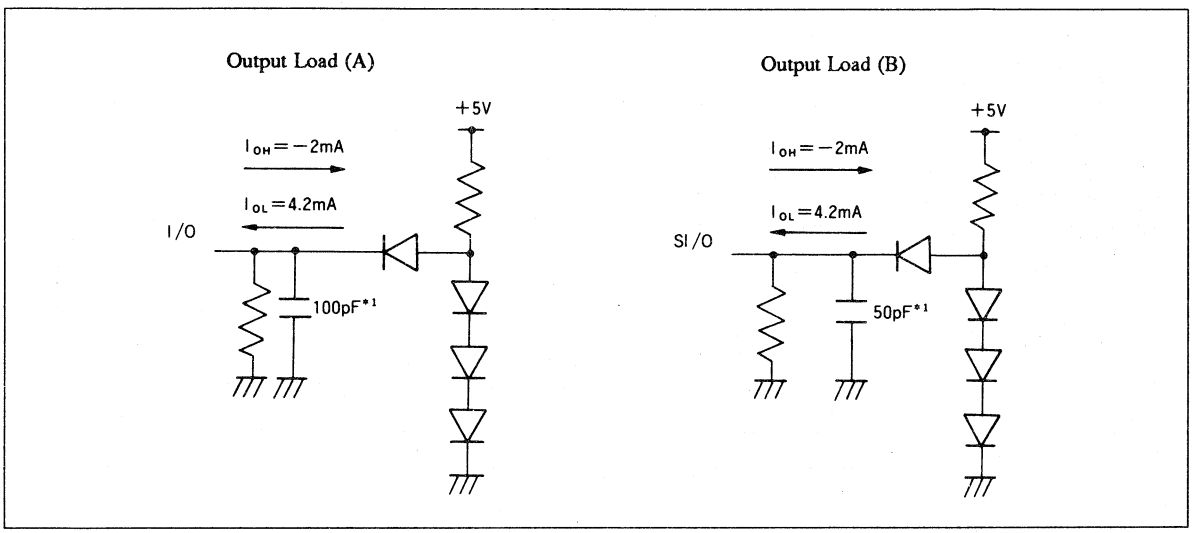
Item	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clock	C_{I2}	—	—	5	pF
I/O, SI/O	$C_{I/O}$	—	—	7	pF

Note: This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) *1, *11

Test Conditions

Input rise and fall time:	5 ns
Output load:	See figures
Input timing reference levels:	0.8 V, 2.4 V
Output timing reference levels:	0.4 V, 2.4 V



Note: *1. Including scope & jig.

Common Parameter

Item	Symbol	HM534251-10 HM534252-10		HM534251-11 HM534252-11		HM534251-12 HM534252-12		HM534251-15 HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	190	—	190	—	220	—	260	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	80	—	80	—	90	—	100	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	30	10000	30	10000	35	10000	40	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	15	—	15	—	15	—	20	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	20	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	70	25	70	25	85	30	110	ns	*5,*6
$\overline{RAS}$ hold time	t_{RSH}	30	—	30	—	35	—	40	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	—	100	—	120	—	150	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Transition time (rise to fall)	t_T	3	50	3	50	3	50	3	50	ns	*8
Refresh period	t_{REF}	—	8	—	8	–	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ setup time	t_{DTS}	0	—	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ hold time	t_{DTH}	15	—	15	—	15	—	20	—	ns	
Data-in to $\overline{OE}$ delay time	t_{DZO}	0	—	0	—	0	—	0	—	ns	
Data-in to $\overline{CAS}$ delay time	t_{DZC}	0	—	0	—	0	—	0	—	ns	

Read Cycle (RAM), Page Mode Read Cycle

Item	Symbol	HM534251-10 HM534252-10		HM534251-11 HM534252-11		HM534251-12 HM534252-12		HM534251-15 HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	—	100	—	100	—	120	—	150	ns	*2, *3
Access time from $\overline{CAS}$	t_{CAC}	—	30	—	30	—	35	—	40	ns	*3, *5
Access time from $\overline{OE}$	t_{OAC}	—	30	—	30	—	35	—	40	ns	*3
Address access time	t_{AA}	—	45	—	45	—	55	—	70	ns	*3, *6
Output buffer turn-off delay referenced to $\overline{CAS}$	t_{OFF1}	—	25	—	25	—	30	—	40	ns	*7
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	—	25	—	25	—	30	—	40	ns	*7
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	0	—	ns	*12
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	*12
$\overline{RAS}$ to column address delay time	t_{RAD}	20	55	20	55	20	65	25	80	ns	*5, *6
Page mode cycle time	t_{PC}	55	—	55	—	65	—	80	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	15	—	20	—	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	50	—	50	—	60	—	75	ns	
Page mode $\overline{RAS}$ pulse width	t_{RASP}	0.1	100	0.1	100	0.12	100	0.15	100	µs	

Write Cycle (RAM), Page Mode Write Cycle

Item	Symbol	HM534251-10 HM534252-10		HM534251-11 HM534252-11		HM534251-12 HM534252-12		HM534251-15 HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	0	—	ns	*9
Write command hold time	t_{WCH}	25	—	25	—	25	—	30	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	20	—	25	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	30	—	30	—	35	—	40	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30	—	30	—	35	—	40	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	*10
Data-in hold time	t_{DH}	25	—	25	—	25	—	30	—	ns	*10
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	15	—	20	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	15	—	15	—	15	—	20	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	10	—	10	—	15	—	20	—	ns	
Page mode cycle time	t_{PC}	55	—	55	—	65	—	80	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	15	—	20	—	ns	
Page mode $\overline{RAS}$ pulse width	t_{RASP}	0.1	100	0.1	100	0.12	100	0.15	100	µs	

Read-Modify-Write Cycle

Item	Symbol	HM534251-10 HM534252-10		HM534251-11 HM534252-11		HM534251-12 HM534252-12		HM534251-15 HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	t_{RWC}	255	—	255	—	295	—	350	—	ns	
$\overline{RAS}$ pulse width	t_{RWS}	165	10000	165	10000	195	10000	240	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	65	—	65	—	75	—	90	—	ns	*9
Column address to $\overline{WE}$ delay	t_{AWD}	80	—	80	—	95	—	120	—	ns	*9
$\overline{OE}$ to data-in delay time	t_{ODD}	25	—	25	—	30	—	40	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	100	—	100	—	120	—	150	ns	*2,*3
Access time from $\overline{CAS}$	t_{CAC}	—	30	—	30	—	35	—	40	ns	*3,*5
Access time from $\overline{OE}$	t_{OAC}	—	30	—	30	—	35	—	40	ns	*3
Address access time	t_{AA}	—	45	—	45	—	55	—	70	ns	*3,*6
$\overline{RAS}$ to column address delay	t_{RAD}	20	55	20	55	20	65	25	80	ns	*5,*6
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	—	25	—	25	—	30	—	40	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	30	—	30	—	35	—	40	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30	—	30	—	35	—	40	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	20	—	25	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	*10
Data-in hold time	t_{DH}	25	—	25	—	25	—	30	—	ns	*10
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	15	—	20	—	ns	
Mask data to RAS setup time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask data to RAS hold time	t_{MH}	15	—	15	—	15	—	20	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	10	—	10	—	15	—	20	—	ns	

Refresh Cycle

Item	Symbol	HM534251-10 HM534252-10		HM534251-11 HM534252-11		HM534251-12 HM534252-12		HM534251-15 HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20	—	20	—	25	—	30	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

Transfer Cycle

Item	Symbol	HM534251-10 HM534252-10		HM534251-11 HM534252-11		HM534251-12 HM534252-12		HM534251-15 HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	15	—	20	—	ns	
$\overline{SE}$ to $\overline{RAS}$ setup time	t_{ES}	0	—	0	—	0	—	0	—	ns	
$\overline{SE}$ to $\overline{RAS}$ hold time	t_{EH}	15	—	15	—	15	—	20	—	ns	
$\overline{RAS}$ to SC delay time	t_{SRD}	25	—	30	—	30	—	35	—	ns	
SC to $\overline{RAS}$ setup time	t_{SRS}	30	—	40	—	40	—	45	—	ns	
$\overline{DT}$ hold time from $\overline{RAS}$	t_{RDH}	80	—	90	—	90	—	110	—	ns	
$\overline{DT}$ hold time from $\overline{CAS}$	t_{CDH}	20	—	30	—	30	—	45	—	ns	
Last SC to $\overline{DT}$ delay time	t_{SDD}	5	—	5	—	5	—	10	—	ns	
First SC to $\overline{DT}$ hold time	t_{SDH}	20	—	25	—	25	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ lead time	t_{DTL}	50	—	50	—	50	—	50	—	ns	
$\overline{DT}$ hold time referenced to $\overline{RAS}$ high	t_{DTHH}	20	—	25	—	25	—	30	—	ns	
$\overline{DT}$ precharge time	t_{DTP}	30	—	35	—	35	—	40	—	ns	
Serial data input delay time from $\overline{RAS}$	t_{SID}	50	—	60	—	60	—	75	—	ns	
Serial data input to $\overline{RAS}$ delay time	t_{SZR}	10	—	10	—	10	—	10	—	ns	
Serial output buffer turn-off delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	60	10	75	ns	*7
$\overline{RAS}$ to Sout (Low-Z) delay time	t_{RLZ}	5	—	10	—	10	—	10	—	ns	
Serial clock cycle time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
Serial clock cycle time	t_{SCC}	40	—	40	—	40	—	60	—	ns	*13
Access time from SC	t_{SCA}	—	30	—	35	–	40	—	50	ns	*4
Serial data out hold time	t_{SOH}	7	—	7	—	7	—	7	—	ns	*4
SC pulse width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	20	—	20	—	25	—	ns	

Serial Read Cycle

Item	Symbol	HM534251-10 HM534252-10		HM534251-11 HM534252-11		HM534251-12 HM534252-12		HM534251-15 HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Serial clock cycle time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
Access time from SC	t_{SCA}	—	30	—	35	—	40	—	50	ns	*4
Access time from $\overline{SE}$	t_{SEA}	—	25	—	30	—	30	—	40	ns	*4
Serial data-out hold time	t_{SOH}	7	—	7	—	7	—	7	—	ns	*4
SC pulse width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial output buffer turn-off delay from $\overline{SE}$	t_{SEZ}	—	25	—	25	—	25	—	30	ns	*7

Serial Write Cycle

Item	Symbol	HM534251-10 HM534252-10		HM534251-11 HM534252-11		HM534251-12 HM534252-12		HM534251-15 HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Serial clock cycle time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
SC pulse width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	20	—	20	—	25	—	ns	
Serial write enable setup time	t_{SWS}	0	—	0	—	0	—	0	—	ns	
Serial write enable hold time	t_{SWH}	30	—	35	—	35	—	50	—	ns	
Serial write disable setup time	t_{SWIS}	0	—	0	—	0	—	0	—	ns	
Serial write disable hold time	t_{SWIH}	30	—	35	—	35	—	50	—	ns	

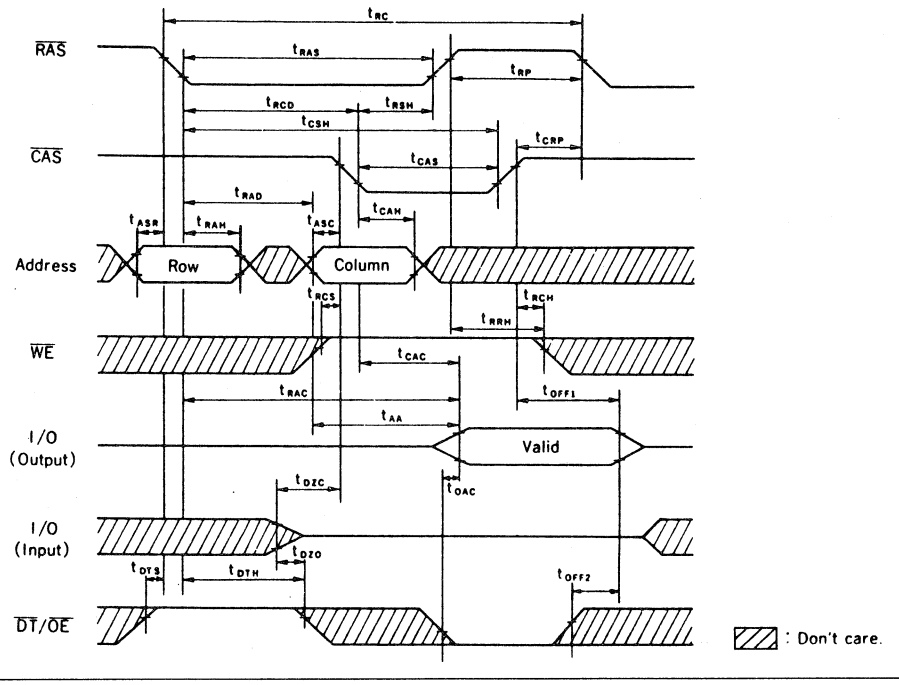
Logic Operation Mode (HM534252 Series)

Item	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ hold time (logic operation set/reset cycle	t_{FCHR}	90	—	90	—	100	—	120	—	ns	
$\overline{RAS}$ pulse width in write cycle	t_{RFS}	140	10000	140	10000	165	10000	200	10000	ns	
$\overline{CAS}$ pulse width in write cycle	t_{CFS}	60	10000	60	10000	70	10000	80	10000	ns	
$\overline{CAS}$ hold time in write cycle	t_{FCSH}	140	—	140	—	165	—	200	—	ns	
$\overline{RAS}$ hold time in write cycle	t_{FRSH}	60	—	60	—	70	—	80	—	ns	
Write cycle time	t_{FRC}	230	—	230	—	265	—	310	—	ns	
Page mode cycle time (write cycle)	t_{FPC}	85	—	85	—	100	—	120	—	ns	
Page mode $\overline{RAS}$ pulse width	t_{RFSP}	0.14	100	0.14	100	0.165	100	0.2	100	μs	

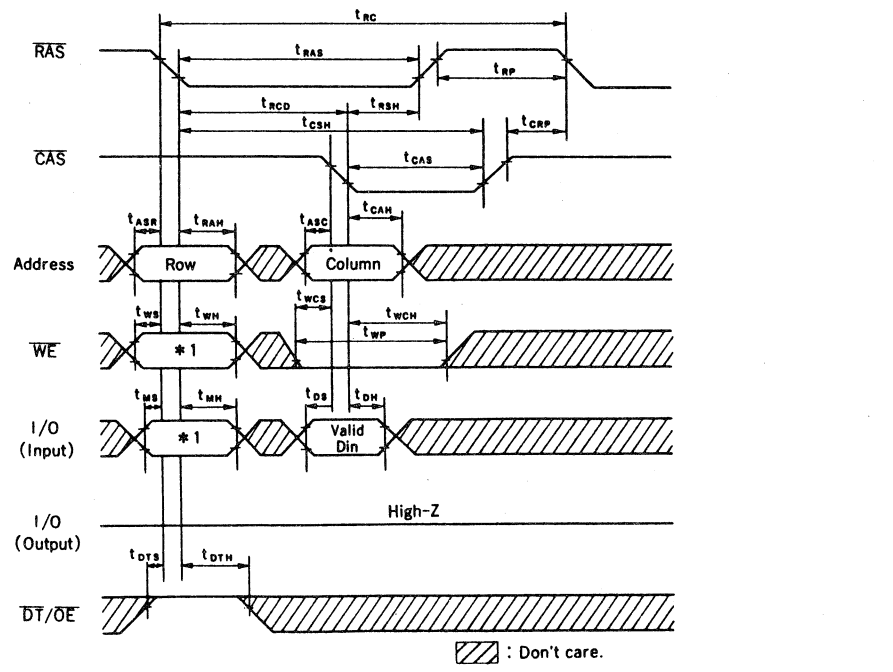
Notes:
*1. AC measurements assume t_T = 5 ns.
*2. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
*3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
*4. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
*5. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
*6. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
*7. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition (V_{OH} – 200 mV, V_{OL} + 200 mV).
*8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
*9. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read-modify-write cycle; the data of the selected address is read out from a data output pin and input data is written into the selected address. In this case, impedance on I/O pins is controlled by $\overline{OE}$.
*10. These parameters are referenced to $\overline{CAS}$ falling edge in early write cycles or to $\overline{WE}$ falling edge in delayed write or read-modify-write cycles.
*11. After power-up, pause for 100 μs or more and execute at least 8 initialization cycles (normal memory cycles or refresh cycles), then start operation.
*12. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.
*13. tSCC is applied to the last SAM access cycle of read transfer cycle-1 before transfer.
*14. When I/O or SI/O is in the output state, data input signals must not be applied to I/O or SI/O.
*15. When $\overline{SE}$ is low after power on, SI/O is in the output state. Data input signals must not be applied to SI/O in this time.
*16. When $\overline{CAS}$ and $\overline{DT}/\overline{OE}$ are both low after power on, it is possible that I/O is in the output state. Data input signals must not be applied to I/O in this time.

Timing Waveforms

Read Cycle

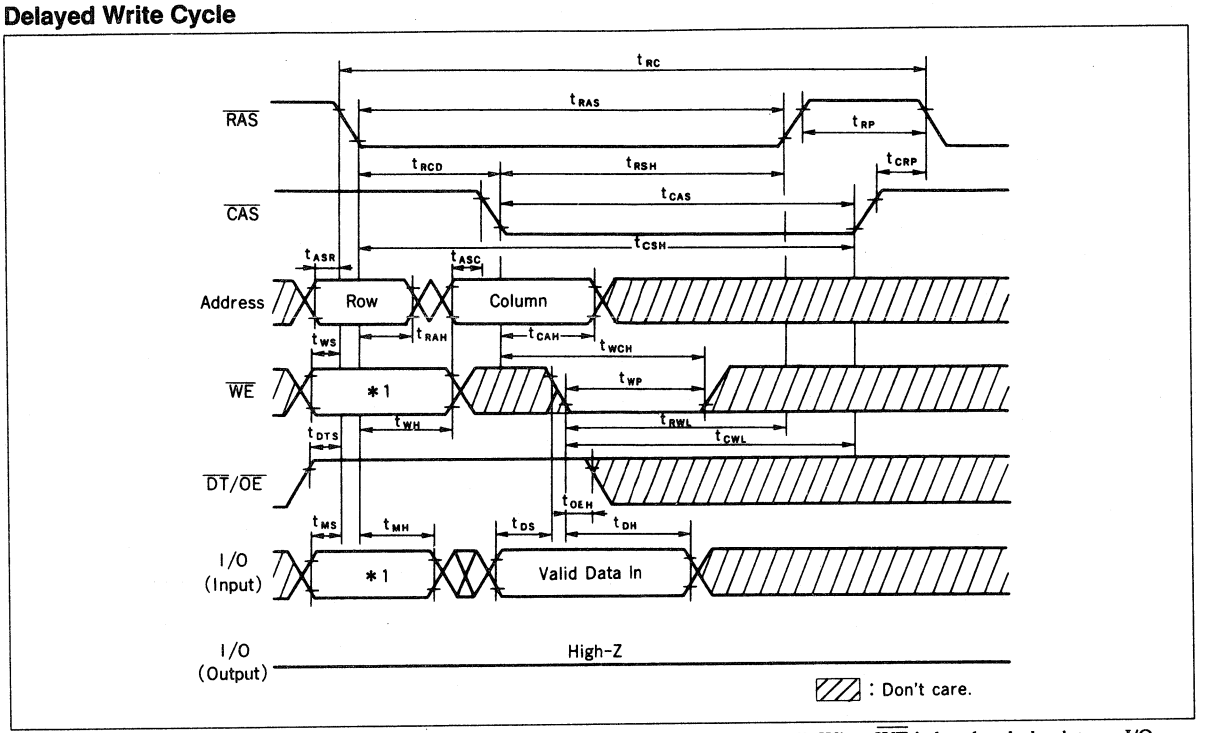


Early Write Cycle



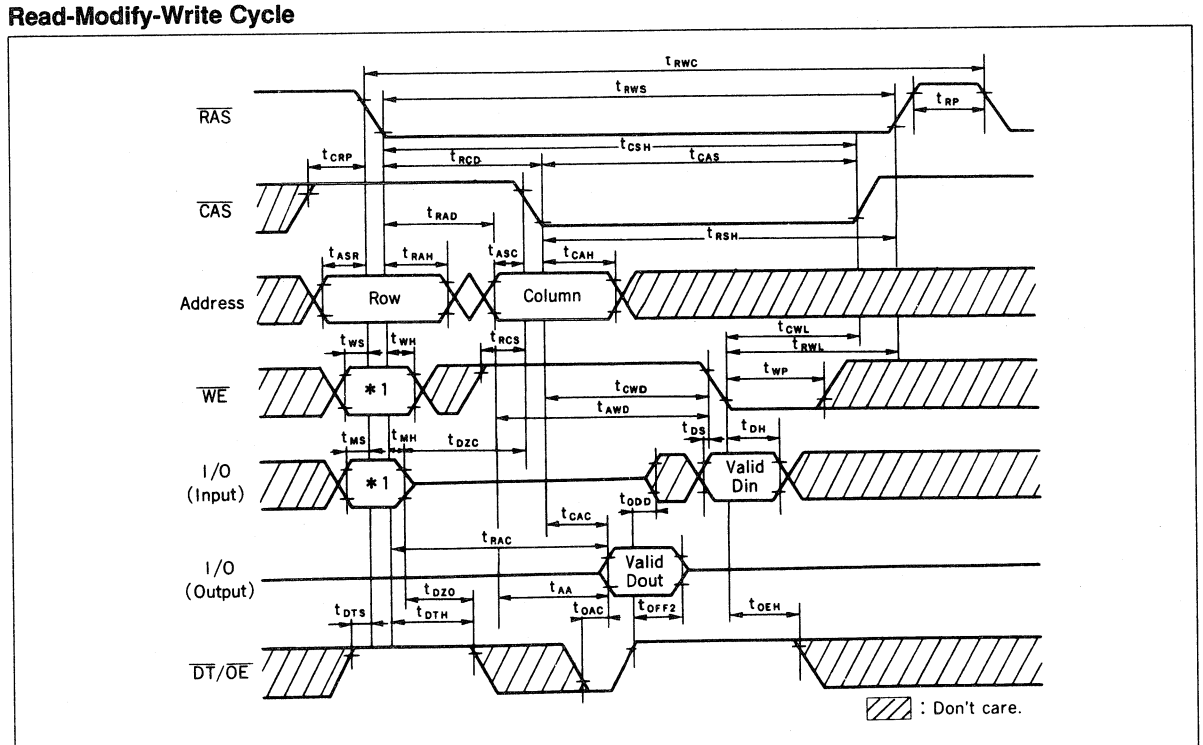
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Delayed Write Cycle



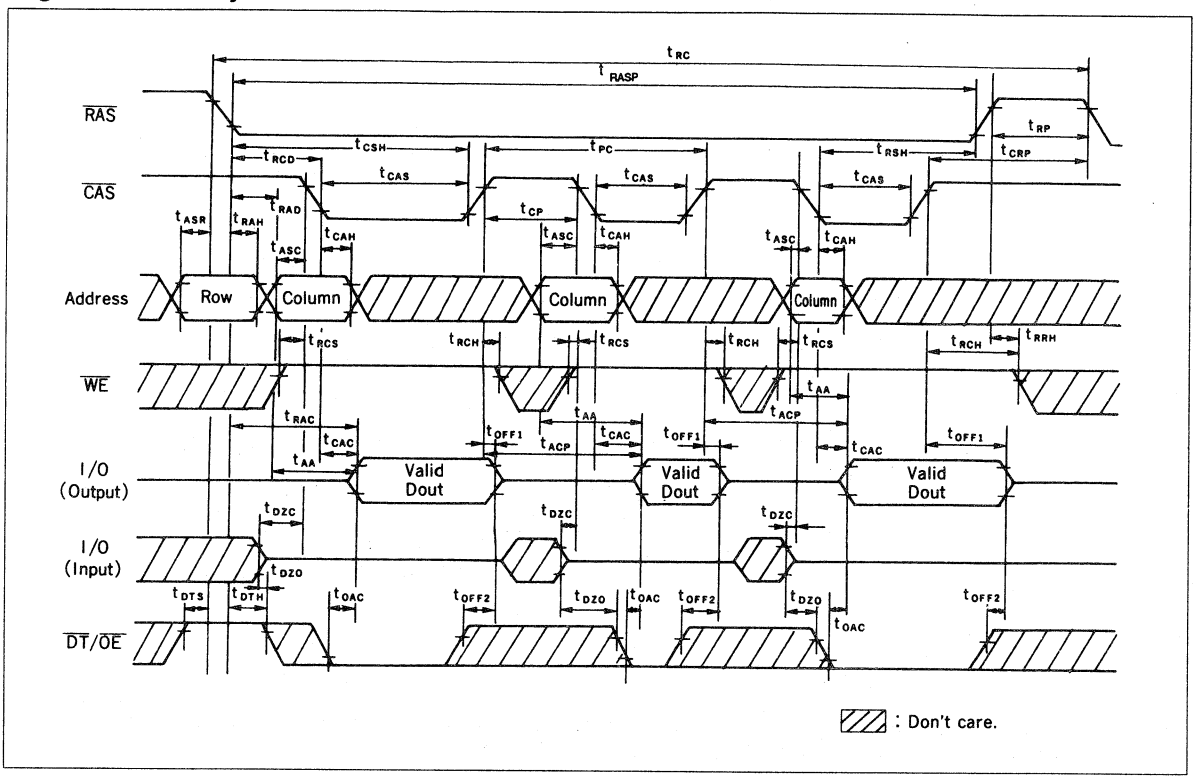
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Read-Modify-Write Cycle

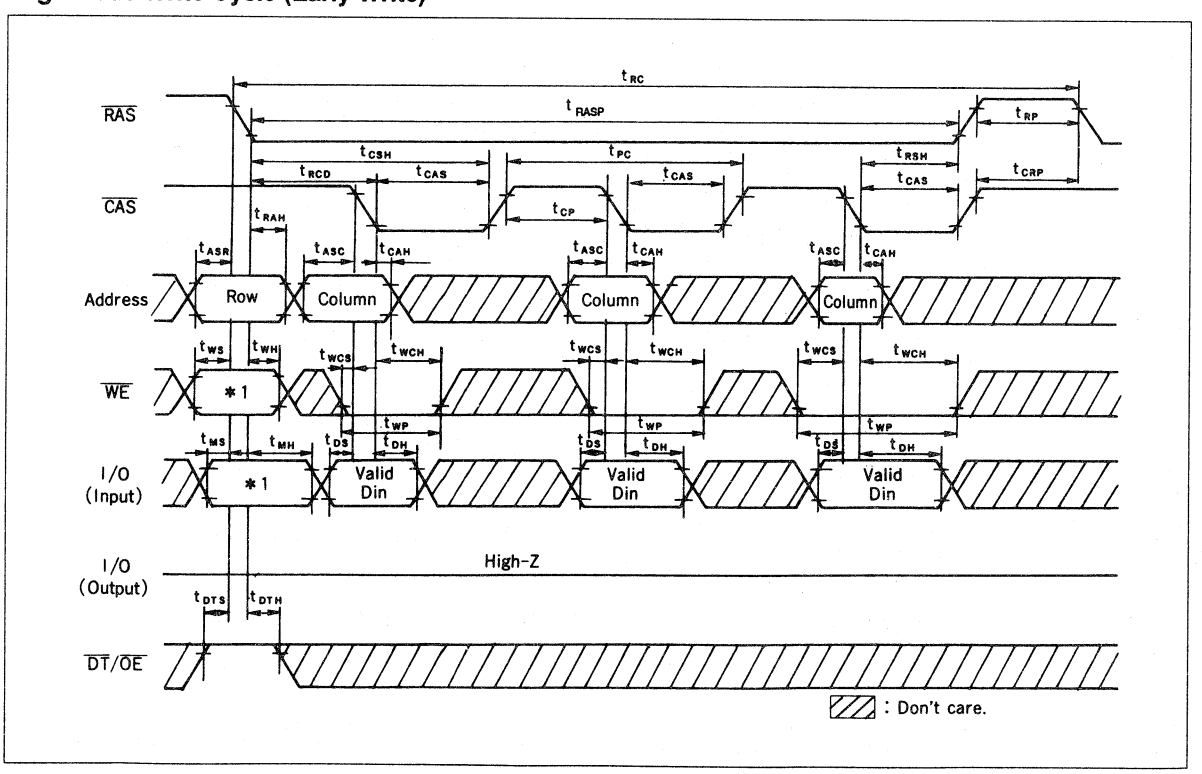


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Read Cycle

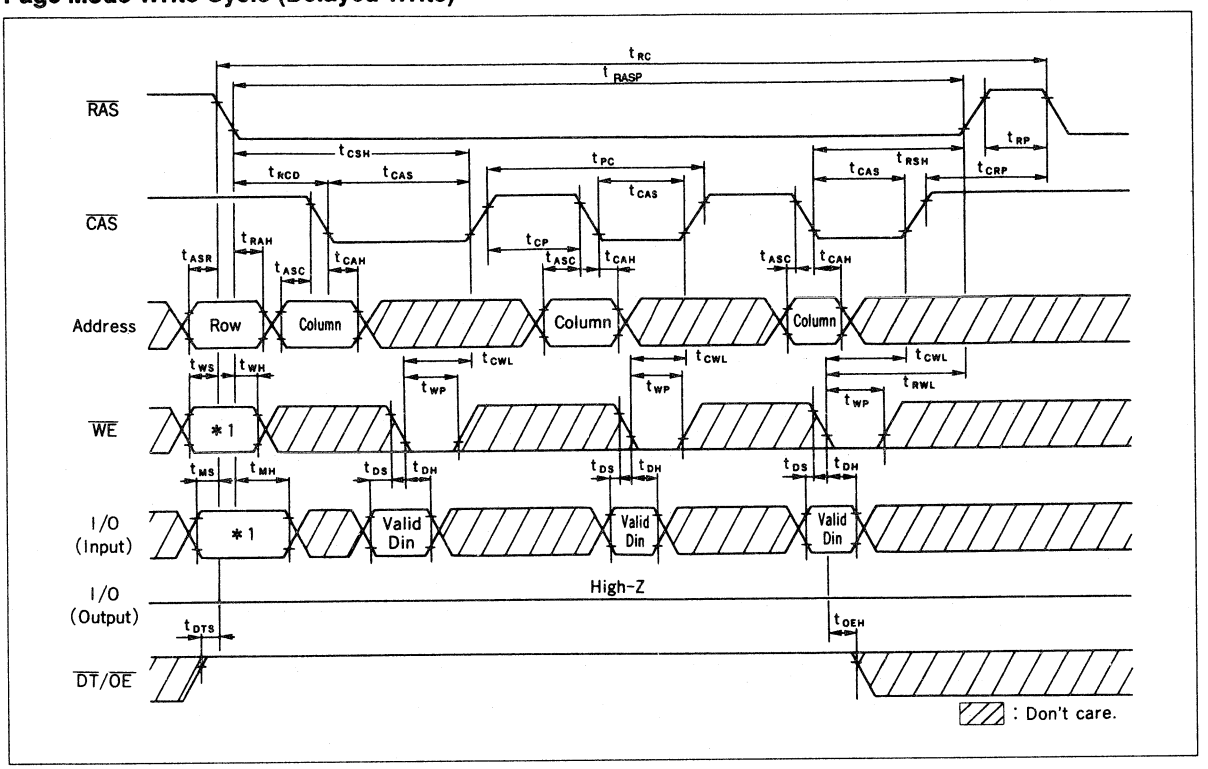


Page Mode Write Cycle (Early Write)



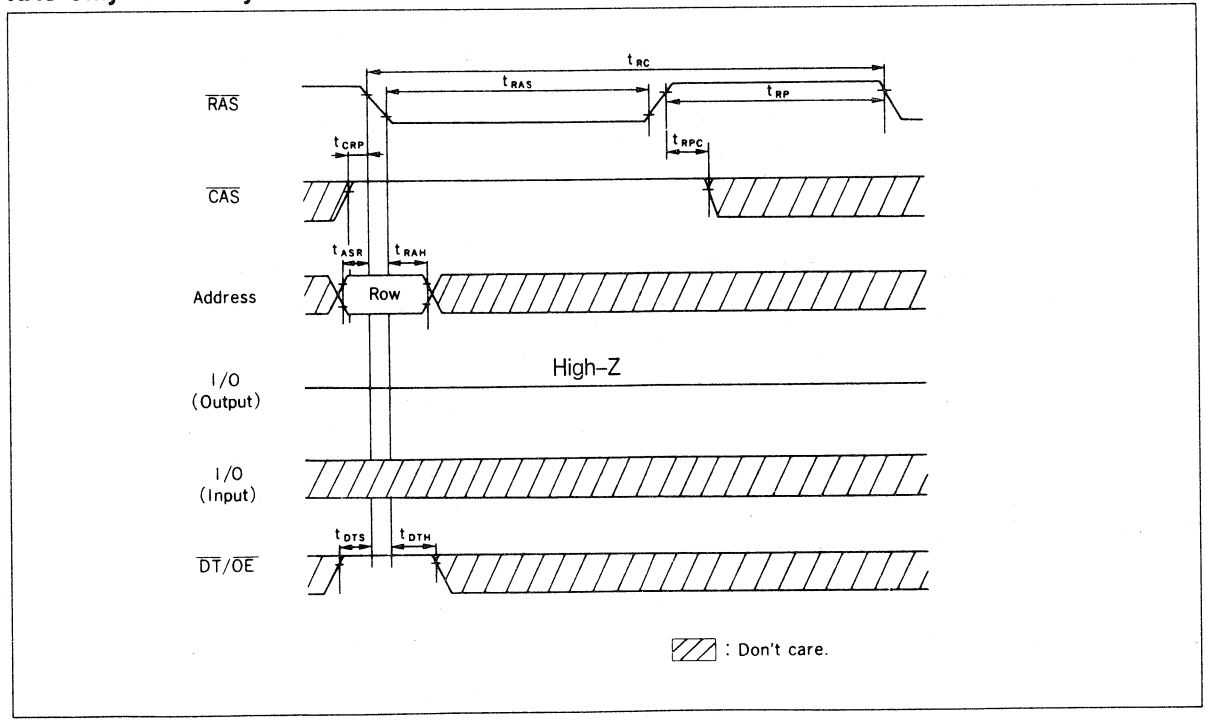
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Delayed Write)

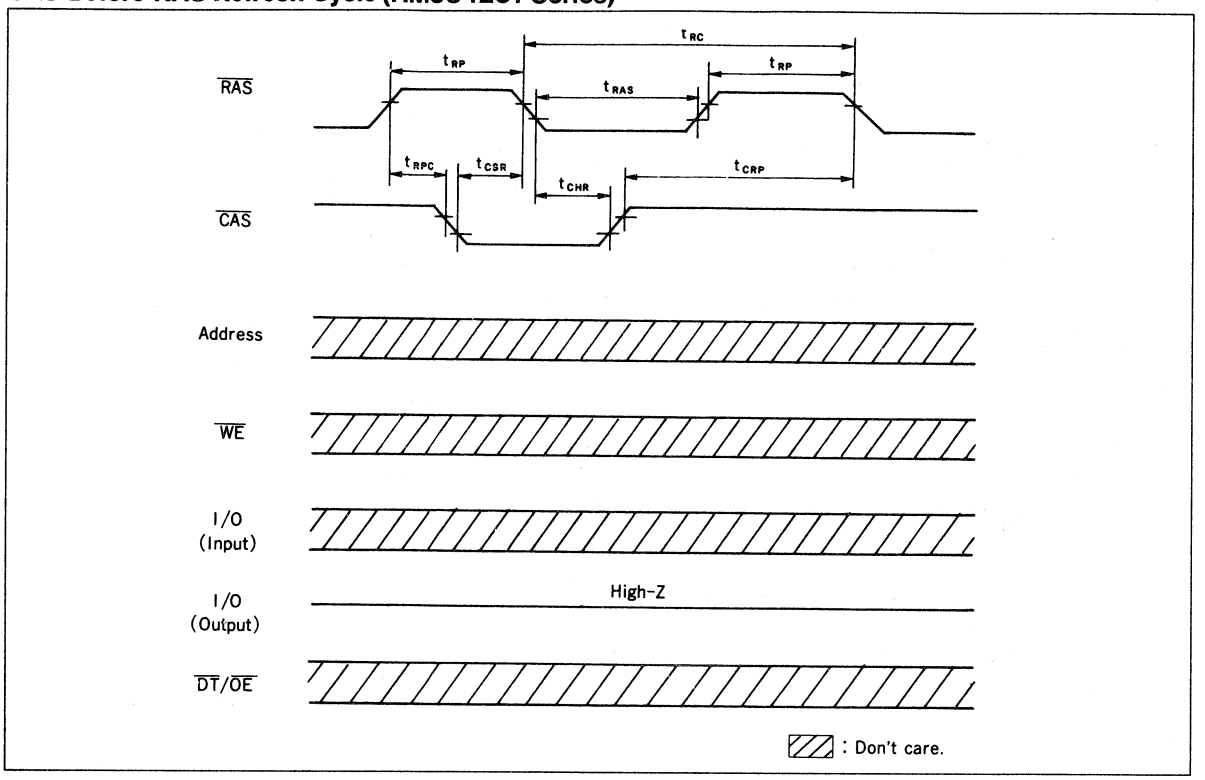


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

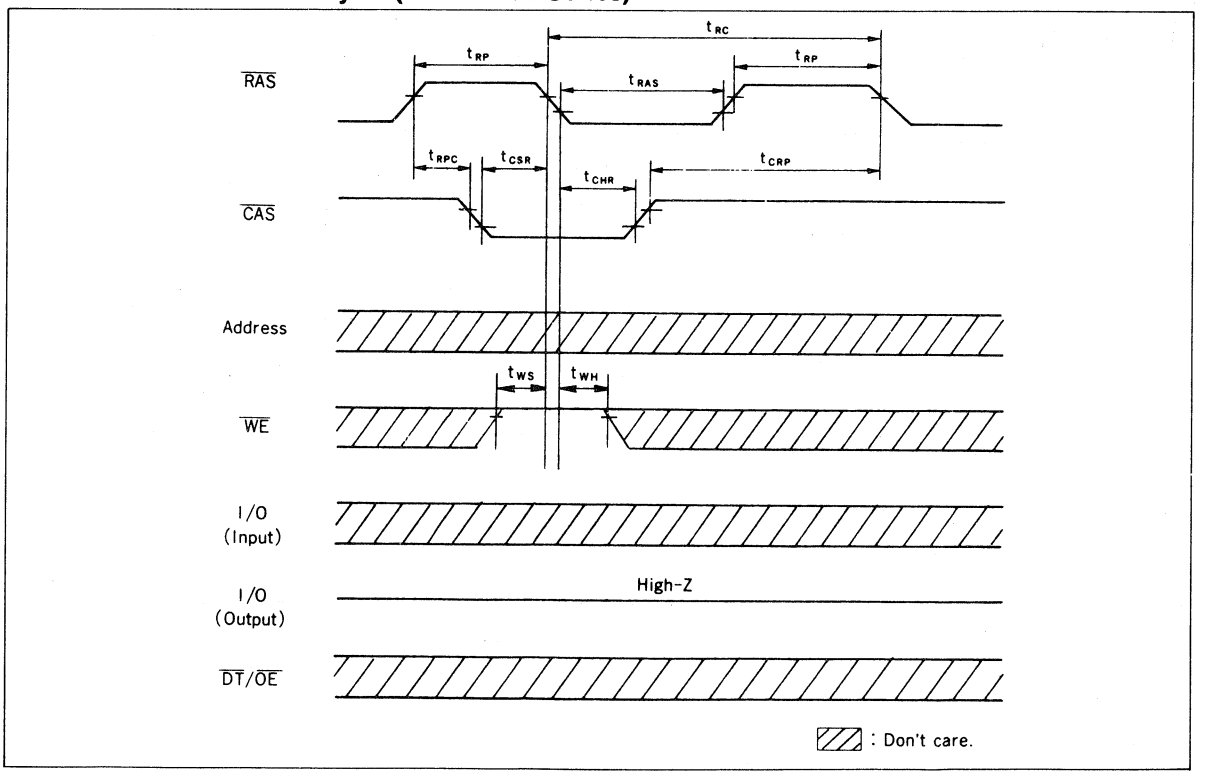
$\overline{RAS}$-Only Refresh Cycle



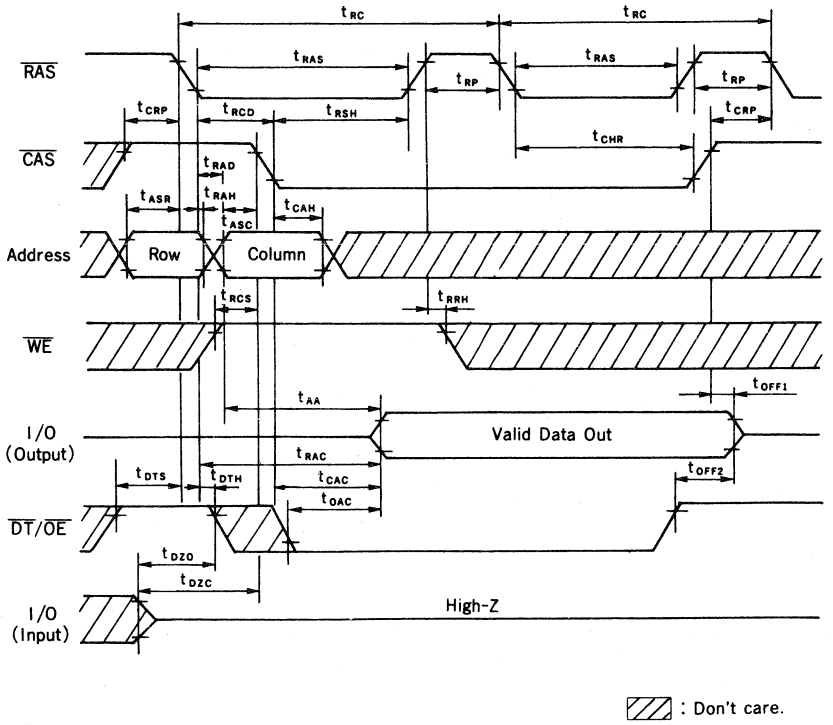
CAS-Before-RAS Refresh Cycle (HM534251 Series)



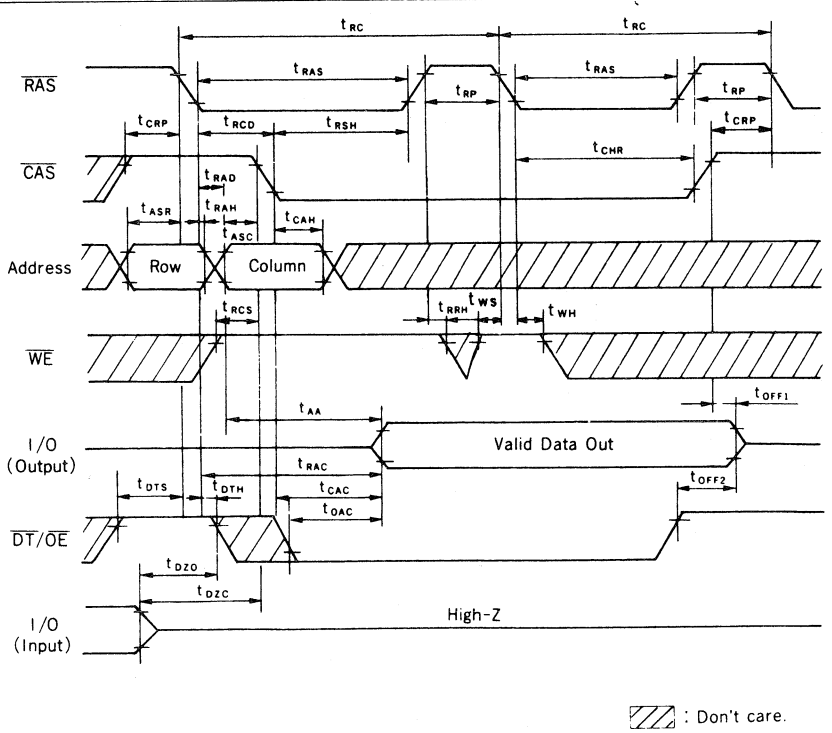
CAS-Before-RAS Refresh Cycle (HM534252 Series)



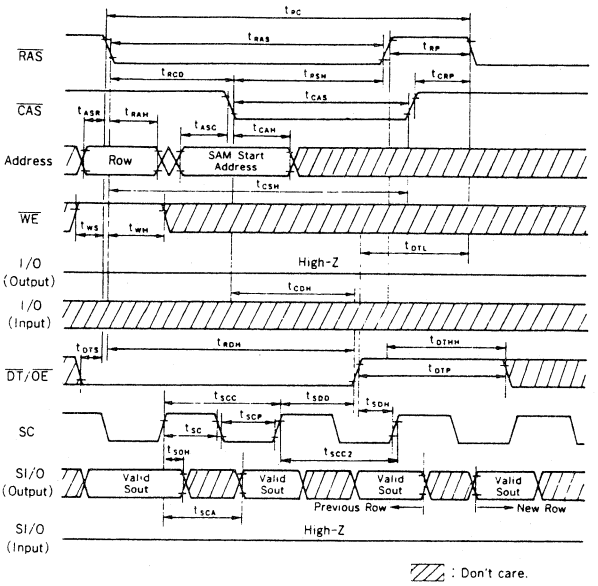
Hidden Refresh Cycle (HM534251 Series)



Hidden Refresh Cycle (HM534252 Series)

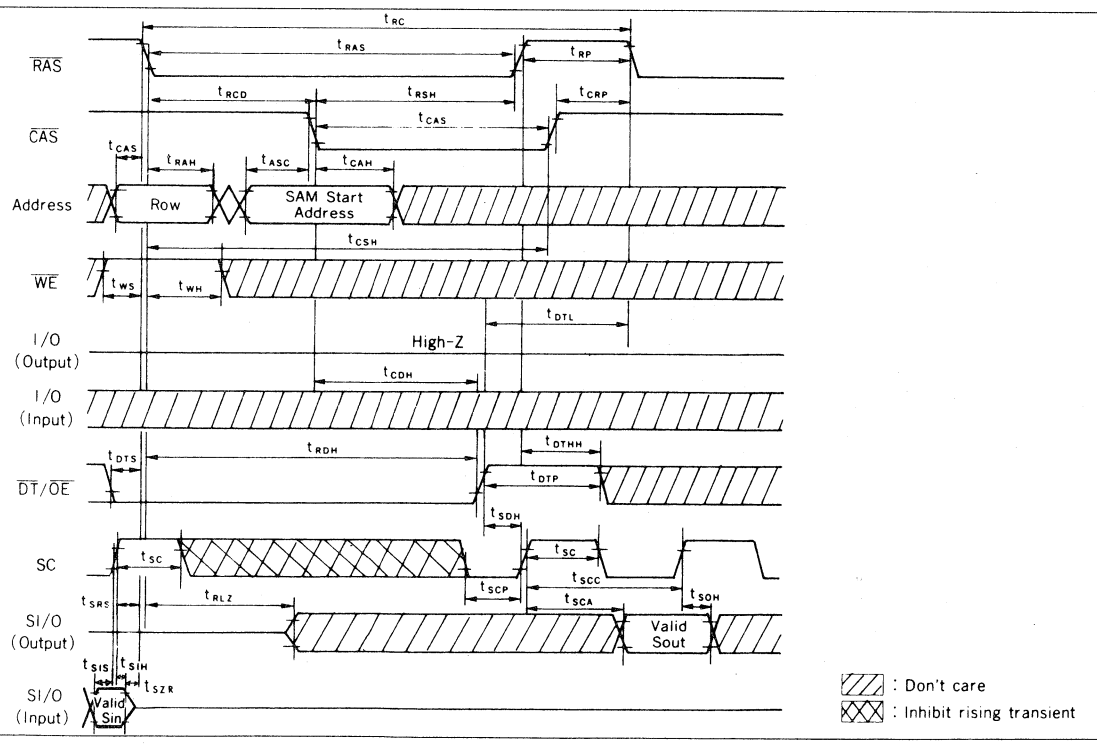


Read Transfer Cycle (1)*1,*2



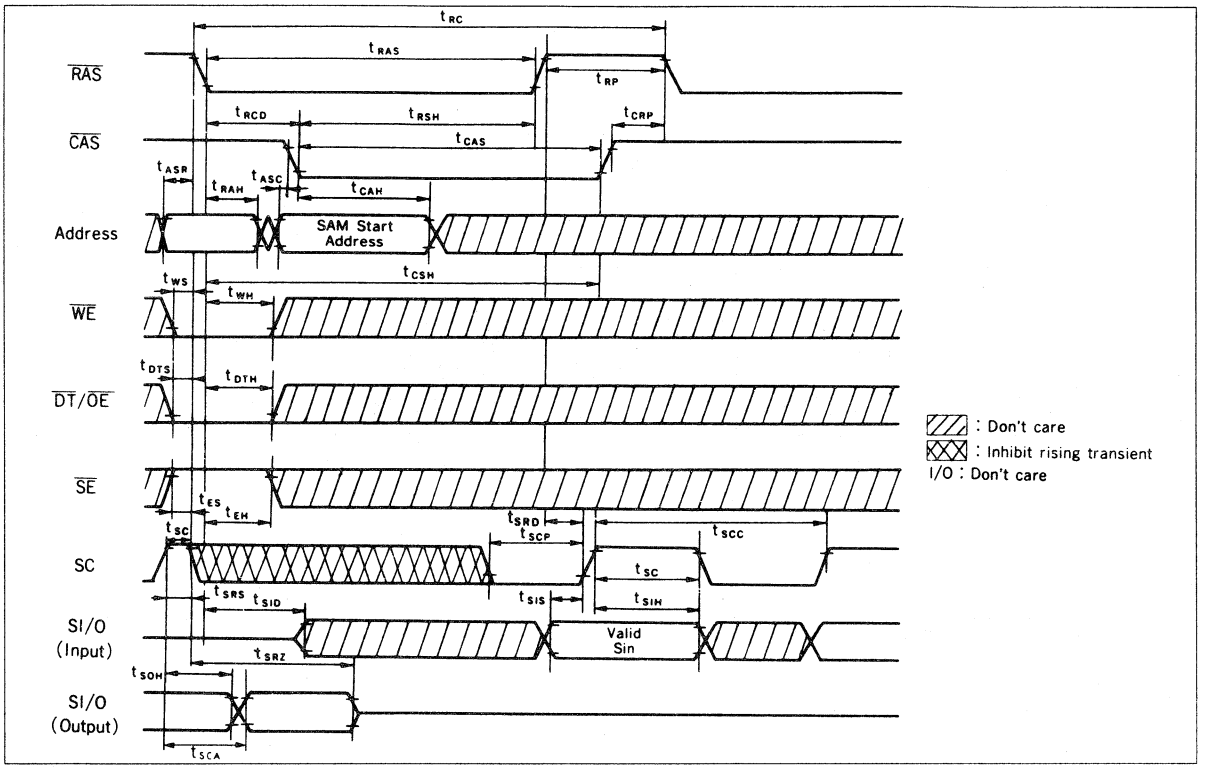
Notes: *1. When the previous data transfer cycle is a read transfer cycle, it is defined as read transfer cycle (1).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)

Read Transfer Cycle (2)*1,*2

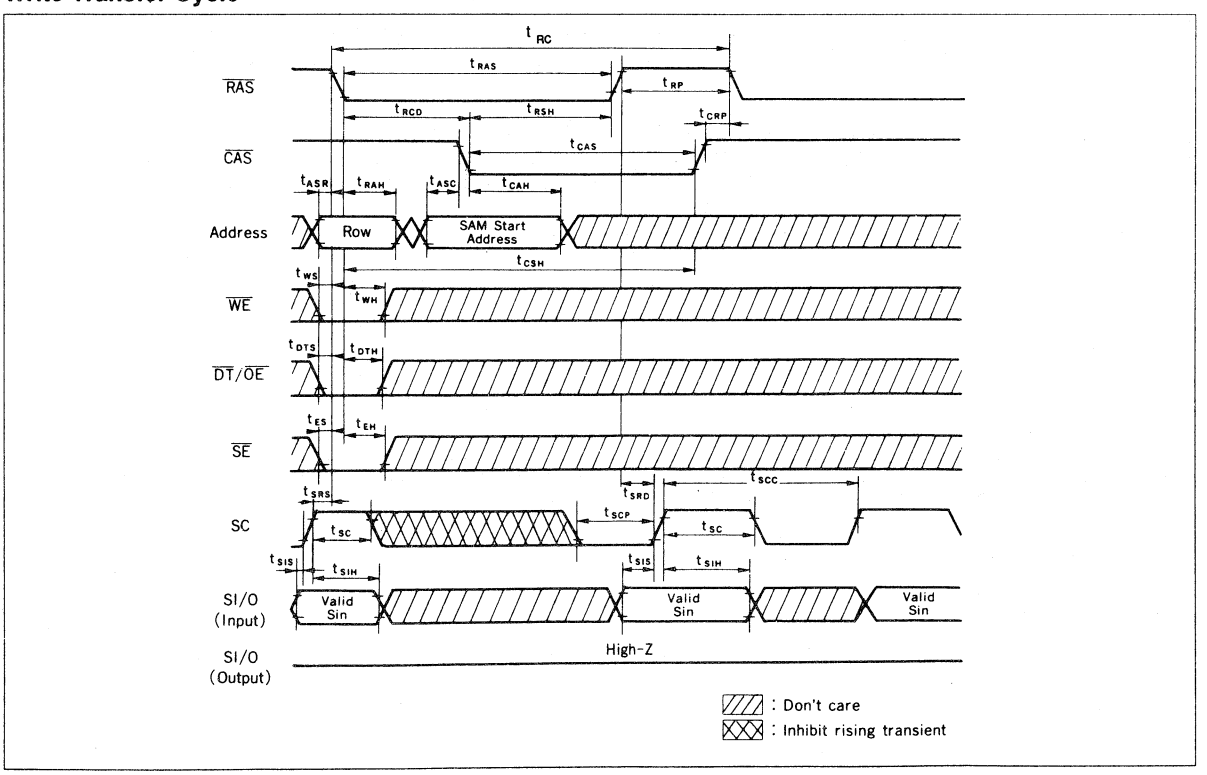


Notes: *1. When the previous data transfer cycle is a write or pseudo transfer cycle, it is defined as read transfer cycle (2).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)

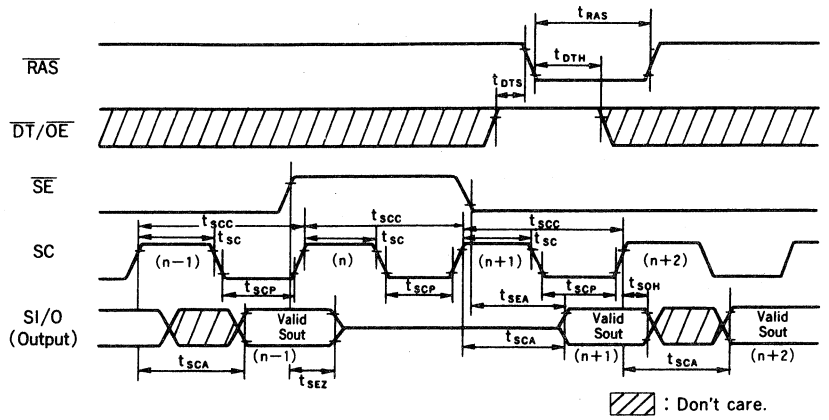
Pseudo Transfer Cycle



Write Transfer Cycle

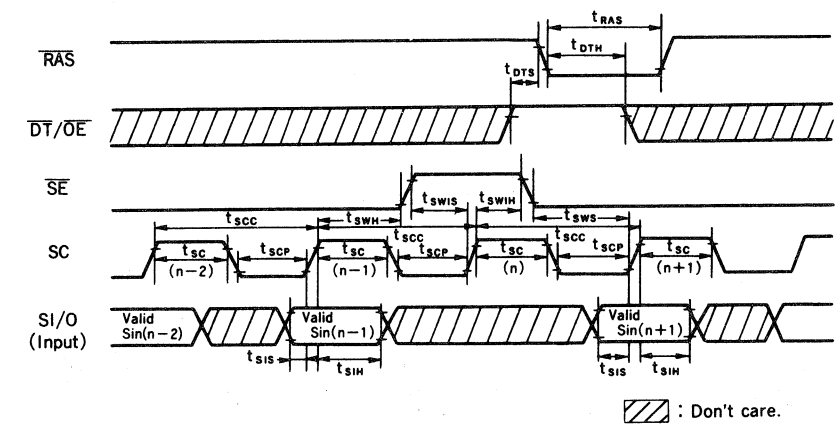


Serial Read Cycle



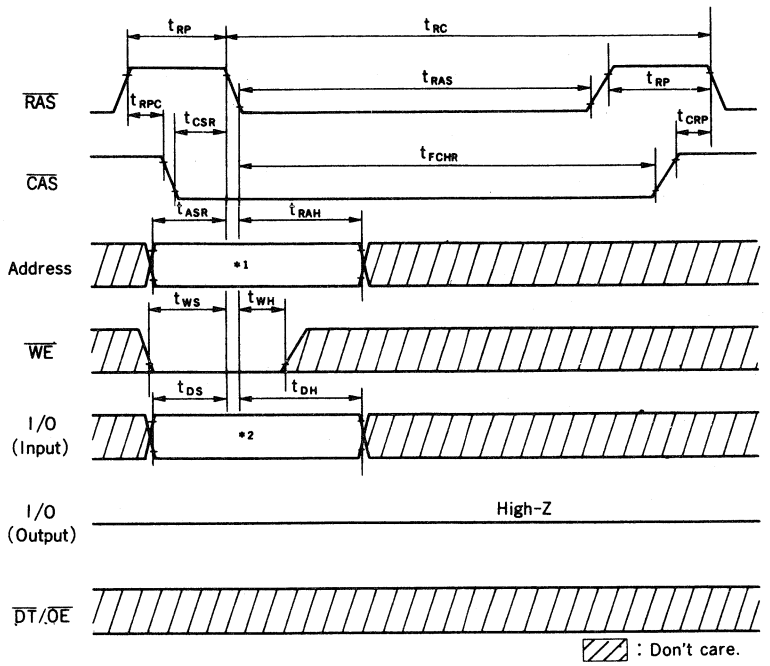
Note: *1. Address 0 is accessed next to address 511.

Serial Write Cycle



Notes: *1. When $\overline{SE}$ is high level in a serial write cycle, data is not written into SAM, however, the pointer is incremented.
*2. Address 0 is accessed next to address 511.

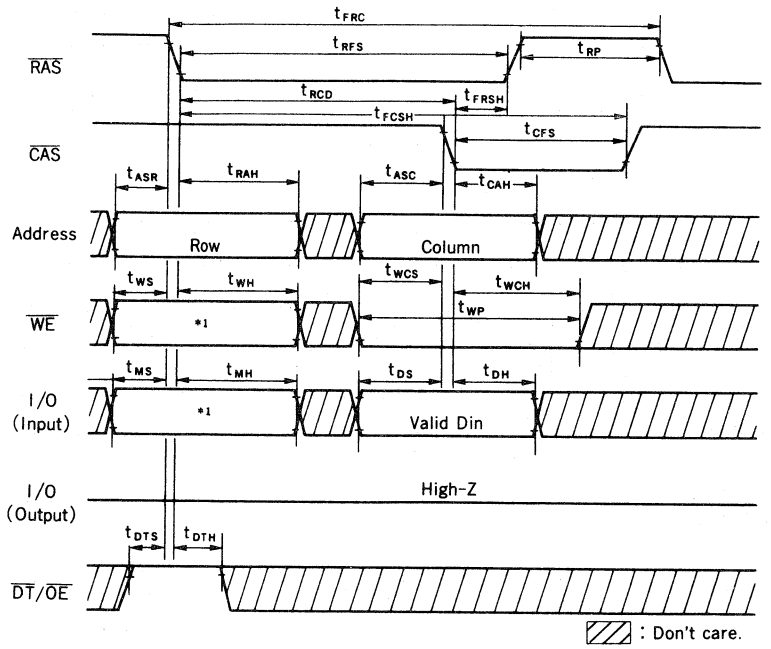
Logic Operation Set/Reset Cycle (HM534252 Series)



Notes: *1. Logic code A0–A3
*2. Write mask data

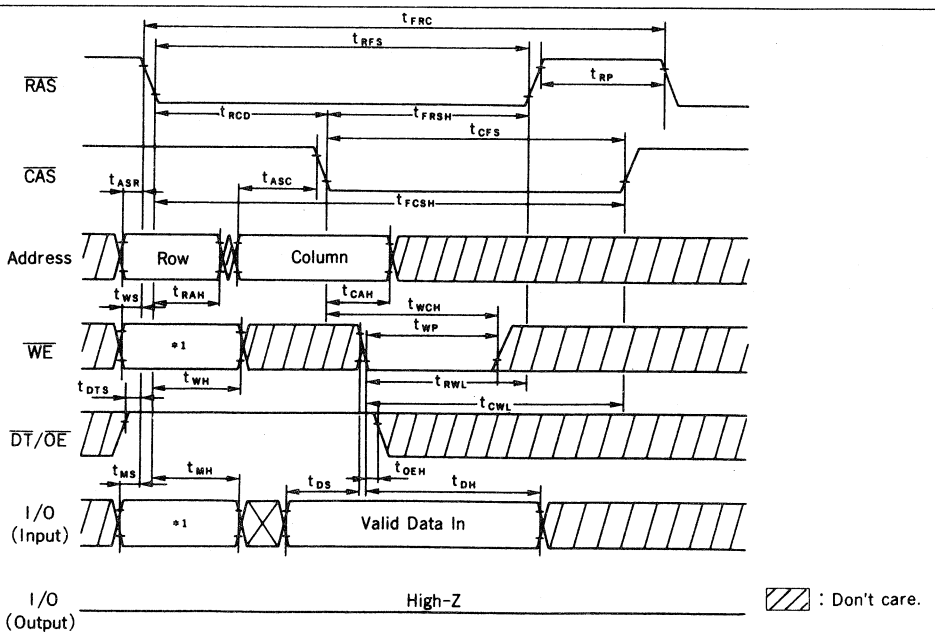
Logic Operation Mode Timing Waveforms

Early Write Cycle (HM534252 Series)



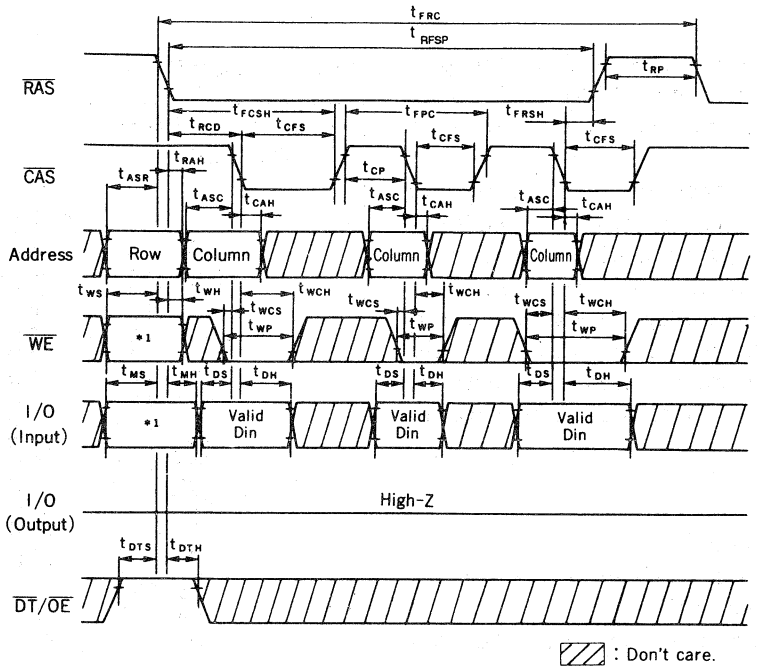
Note: *1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Delayed Write Cycle (HM534252 Series)



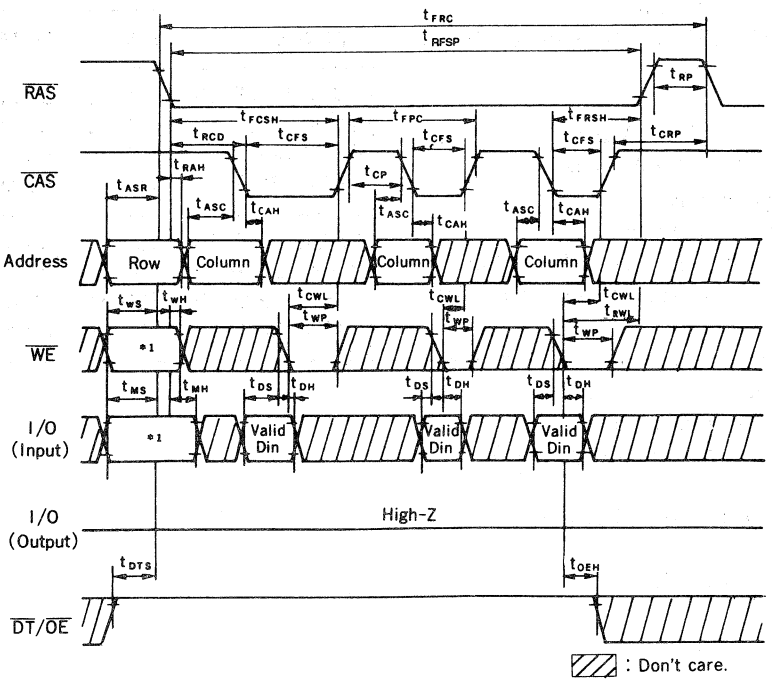
Note: *1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Early Write) (HM534252 Series)



Note: 1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Delayed Write) (HM534252 Series)



Note: 1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

HM538121, HM538122 Series

131072-word × 8-bit Multiport CMOS Video RAM

The HM538121/HM538122 is a 1-Mbit multiport video RAM equipped with a 128-kword × 8-bit dynamic RAM and a 256-word × 8-bit SAM (serial access memory).

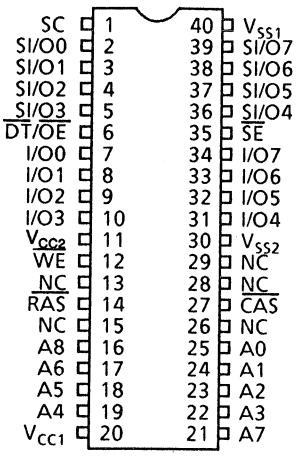
Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has a write mask function. It is suitable for a graphic processing buffer memory. HM538122 also provides logic operation mode to simplify its operation. In this mode, logic operation between memory data and input data can be executed by using internal logic-arithmetic unit.

Features

- Multiport organization
  - Asynchronous and simultaneous operation of RAM and SAM capability
    RAM: 128-kword × 8-bit and SAM: 256-word × 8-bit
- Access time RAM: 100 ns/100 ns/120 ns/150 ns max
  SAM: 30 ns/35 ns/40 ns/50 ns max
- Cycle time RAM: 190 ns/190 ns/220 ns/260 ns min
  SAM: 30 ns/40 ns/40 ns/60 ns min
- Low power
  - Active RAM : 495 mW max
    SAM: 468 mW max
  - Standby 40 mW max
- High-speed page mode capability
- Mask write mode capability (HM538121 Series)
- 2 types of mask write made capability (HM538122 series)
- Bidirectional data transfer cycle between RAM and SAM capability
- Real time read transfer capability
- Logic operation mode capability (HM538122 series)
- 3 variations of refresh (8 ms/512 cycles)
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- TTL compatible

Pin Arrangement

- HM538121JP Series
- HM538122JP Series



(Top View)

Ordering Information

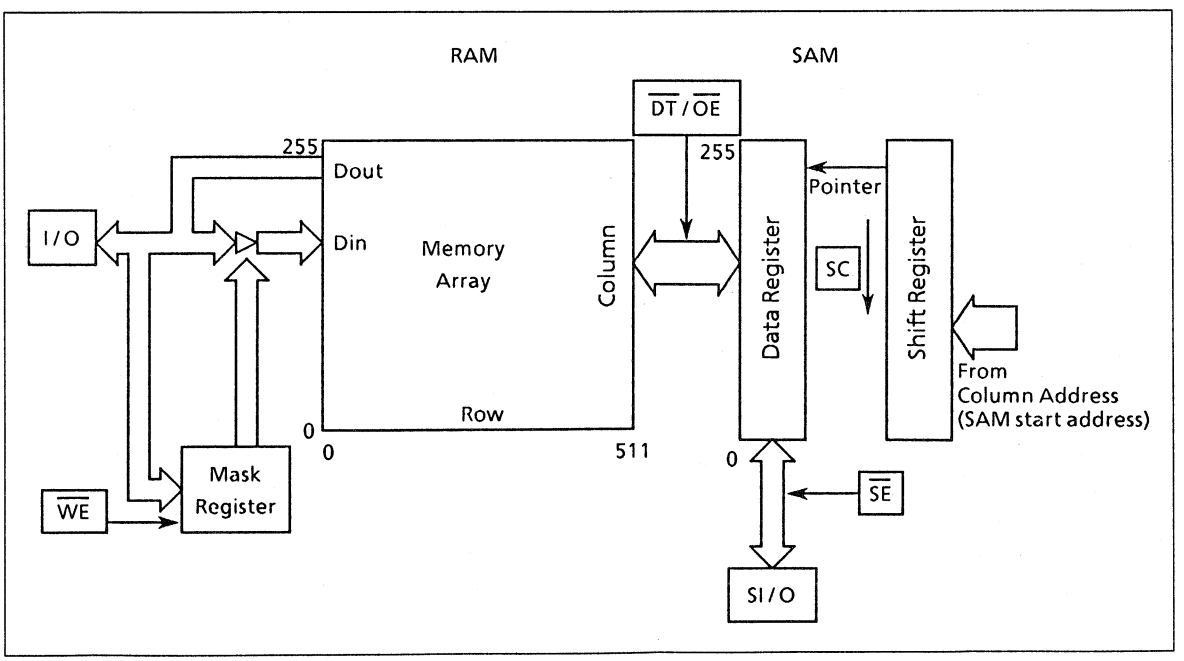
Type No.	Access time RAM	Access time SAM	Package
HM538121JP-10	100 ns	30 ns	400-mil
HM538121JP-11	100 ns	35 ns	40-pin
HM538121JP-12	120 ns	40 ns	plastic SOJ
HM538121JP-15	150 ns	50 ns	(CP-40D)
HM538122JP-10	100 ns	30 ns	
HM538122JP-11	100 ns	35 ns	
HM538122JP-12	120 ns	40 ns	
HM538122JP-15	150 ns	50 ns	

Pin Description

Pin name	Function
A0 – A8	Address inputs
I/O0 – I/O7	RAM port data inputs/outputs
SI/O0 – SI/O7	SAM port data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{DT/OE}$	Data transfer/output enable
SC	Serial clock
$\overline{SE}$	SAM port enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

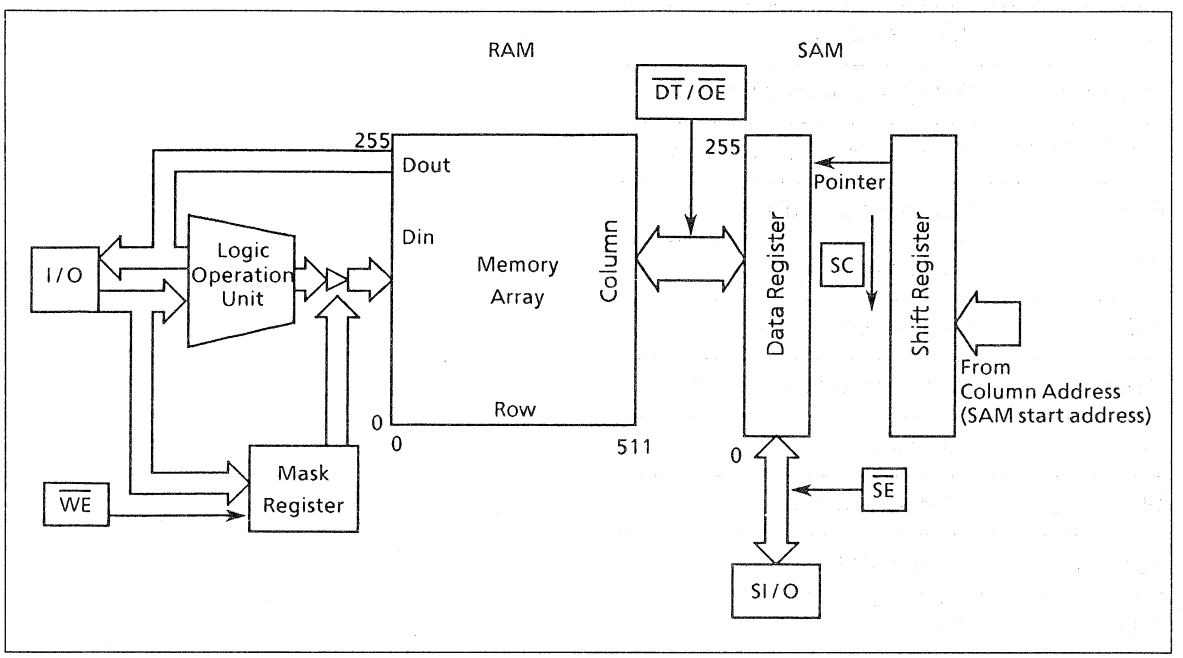
Block Diagram

HM538121 Series



Block Diagram (cont)

HM538122 Series



Pin Function

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of those signals determine the operation cycle of the HM538121 / HM538122.

Table 1 Operation Cycles of the HM538121/HM538122

Input level at the falling edge of $\overline{RAS}$				
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WE}$	$\overline{SE}$	Operation cycle
H	H	H	X	RAM read/write
H	H	L	X	Mask write
H	L	H	X	Read transfer
H	L	L	H	Pseudo transfer
H	L	L	L	Write transfer
L	X	X	X	CBR refresh (HM538121 series)
L	X	H	X	CBR refresh (HM538122 series)
L	X	L	X	Logic operation set/reset (HM538122 series)

Note: X: don't care.

$\overline{CAS}$ (input pin): Column address is put into chip at the falling edge of $\overline{CAS}$. $\overline{CAS}$ controls output impedance of I/O in RAM.

A0 – A8 (input pins): Row address is determined by A0 – A8 level at the falling edge of $\overline{RAS}$. Column address is determined by A0 – A7 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM538121/HM538122 turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O0 – I/O7 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only on high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT}$/$\overline{OE}$ (input pin): $\overline{DT}$/$\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data is output from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is put into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not put into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O0 – SI/O7 (input/output pins): SI/Os are input/output pins in SAM.

Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

Operation of HM538121/HM538122

Operation of RAM Port

RAM Read Cycle ($\overline{DT}$/$\overline{OE}$ high, $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}$/$\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data is output through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}$/$\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle (Early Write, Delayed Write, Read-Modify-Write)
($\overline{DT}$/$\overline{OE}$ high, $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

- Normal Mode Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after $\overline{RAS}$ is set low, a write cycle is executed and I/O data is written at the selected addresses. When all 8 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes high impedance. Data is entered at the $\overline{CAS}$ falling edge.

If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling edge. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables write after read to execute in the same address cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and setting $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is preserved. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode cycle, the mask data is preserved during the page access.

High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle and is higher than the standard page mode cycle by 70 – 80%. This product is based on static column mode, therefore, address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 256-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 µs) and t_{RFSP} max (100 µs) (HM538122 series).

Transfer Operation

HM538121/HM538122 provides the read transfer cycle, pseudo transfer cycle, and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$.

They have following functions:

(1) Transfer data between row address and SAM data register
(except for pseudo transfer cycle)

(2) Determine direction of data transfer
  (a) Read transfer cycle: RAM → SAM
  (b) Write transfer cycle: RAM ← SAM

(3) Determine input or output of SAM I/O pin (SI/O)
Read transfer cycle: SI/O output
Pseudo transfer cycle,
write transfer cycle: SI/O input

(4) Determine first SAM address to access (SAM start address) after transferring at column address.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by setting $\overline{DT}/\overline{OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address data (256 × 8 bit) determined by this cycle is transferred synchronously at the rising of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address decided by column address.

This cycle can execute SAM access serially even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) is specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge, and t_{SDH} (min) between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge (See figure 1).

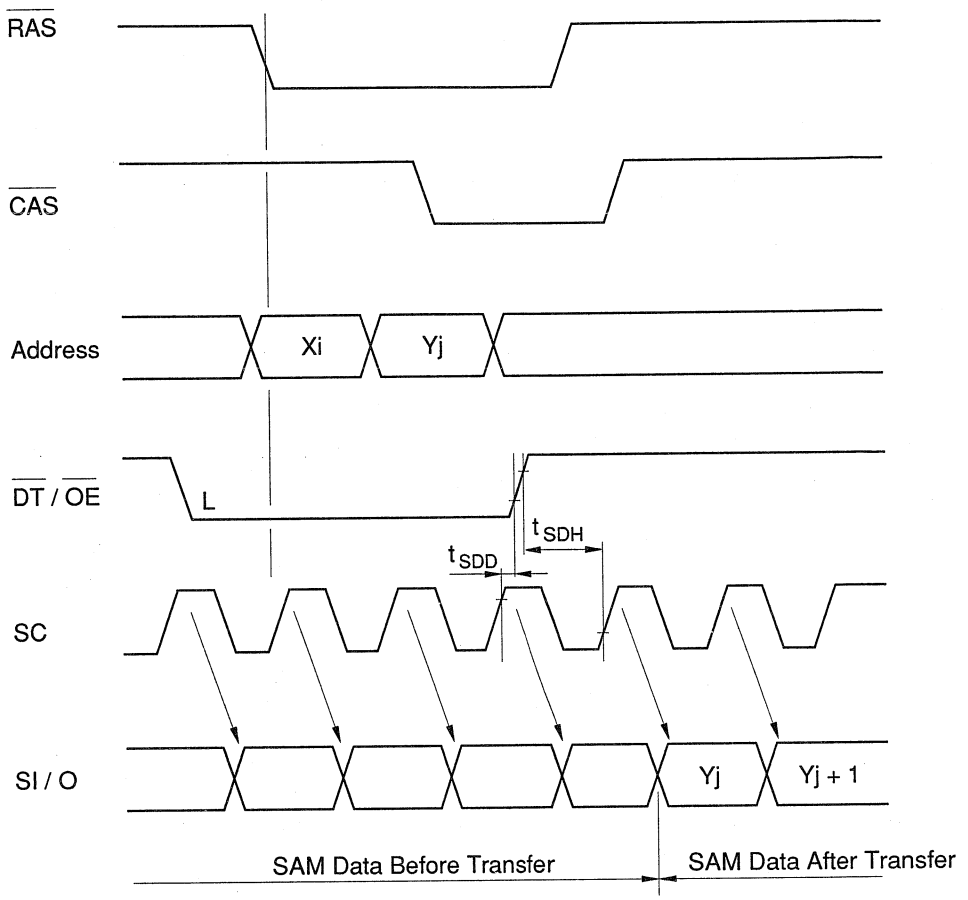


Figure 1 Real Time Read Transfer

If read transfer cycle is executed, SI/O becomes output state. When the previous transfer cycle is either pseudo transfer cycle or write transfer cycle and SI/O is in input state, uncertain data is output after t_{RLZ} (min) after the $\overline{RAS}$ falling edge. Before that, input should be set high impedance to avoid data contention.

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle is available for switching SI/O from output state to input state because data in RAM isn't rewritten. This cycle starts when $\overline{CAS}$ is high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high, at the falling edge of $\overline{RAS}$. The output buffer in SI/O becomes high impedance within t_{SRZ} (max) from the $\overline{RAS}$ falling edge. Data should be input to SI/O later than t_{SID} (min) to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC should not be raised.

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address to serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC should not be raised.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. If $\overline{SE}$ is set high, SI/O becomes high impedance and internal pointer is incremented at the SC rising edge.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is programmed into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't input into data resister. Internal pointer is incremented according to the SC rising edge, so $\overline{SE}$ high can mask data for SAM.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is performed by accessing all 512 row addresses every 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required for accessing all row addresses every 8 ms.

$\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is performed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high by inputting the row address (= refresh address) from external circuits.
To distinguish this cycle from data transfer cycle, $\overline{DT/OE}$ should be high at the falling edge of $\overline{RAS}$.

CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate. (HM538121 series)

CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate.

To distinguish this cycle from logic operation set/reset cycle, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$. (HM538122 series)
Hidden Refresh Cycle: Hidden refresh cycle performs refresh by reactivating $\overline{RAS}$ when $\overline{DT/OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register, selector), organized as fully static circuitry, don't require refresh.

Logic Operation Mode
(HM538122 series)

The HM538122 supports logic operation capability on RAM port. It performs logic operations between the memory cell data and input data in logic operation mode cycle, and writes the result into the memory cell (read modify write). This function realizes high speed raster operations and simplifies peripheral circuits for raster operations.

Logic Operation Set/Reset Cycle ($\overline{CAS}$ and $\overline{WE}$ Low at the falling edge of $\overline{RAS}$)

In logic operation set/reset cycle, the following operations are performed at the same time; 1. Selection of logic operations and logic operation mode set/reset, 2. Mask data programming, 3. $\overline{CAS}$-before-$\overline{RAS}$ refresh.
Figure 2 shows the timing for logic operation set/reset cycle. This cycle starts when $\overline{CAS}$ and $\overline{WE}$ are low at the falling edge of $\overline{RAS}$. In this cycle, logic operation codes and mask data are programmed by row address and I/O pin at the falling edge of $\overline{RAS}$ respectively. When write cycle is performed after this cycle, the logic operation write cycle starts. In the logic operation mode, the specification of cycle time is longer than that of normal mode because read-modify-write cycle is performed internally. In this cycle, logic operation codes and mask data programmed are available until reprogrammed. In normal mode, mask data is available only for one $\overline{RAS}$ cycle. Here, the mask data programmed in normal mode is named as "temporary mask data" and the one programmed in logic operation set/reset cycle is named as "mask data".

(1) Selection of logic operations and logic operation mode set/reset

Table 2 shows the logic operations. One operation is selected among sixteen ones by combinations of A0 – A3 levels at the falling edge of $\overline{RAS}$. (A4 – A8 are Don't care.) Logic operation codes (A3, A2, A1, A0) = (0, 1, 0, 1) resets the logic operation mode. When write cycle is performed after that, normal write cycle starts. However, even in this case, mask data is still available. I/O should be at high level at the falling edge of $\overline{RAS}$ in logic operation set/reset cycle when mask data is not used.

(2) Mask data programming

High/low level of I/O at the falling edge of $\overline{RAS}$ functions as mask data. When I/O is high, the data is written in write cycle. When I/O is low, the input data is masked and the same memory cell data remains. Mask data, programmed in this cycle, is available until reprogrammed. It is advantageous when the same mask data continues.

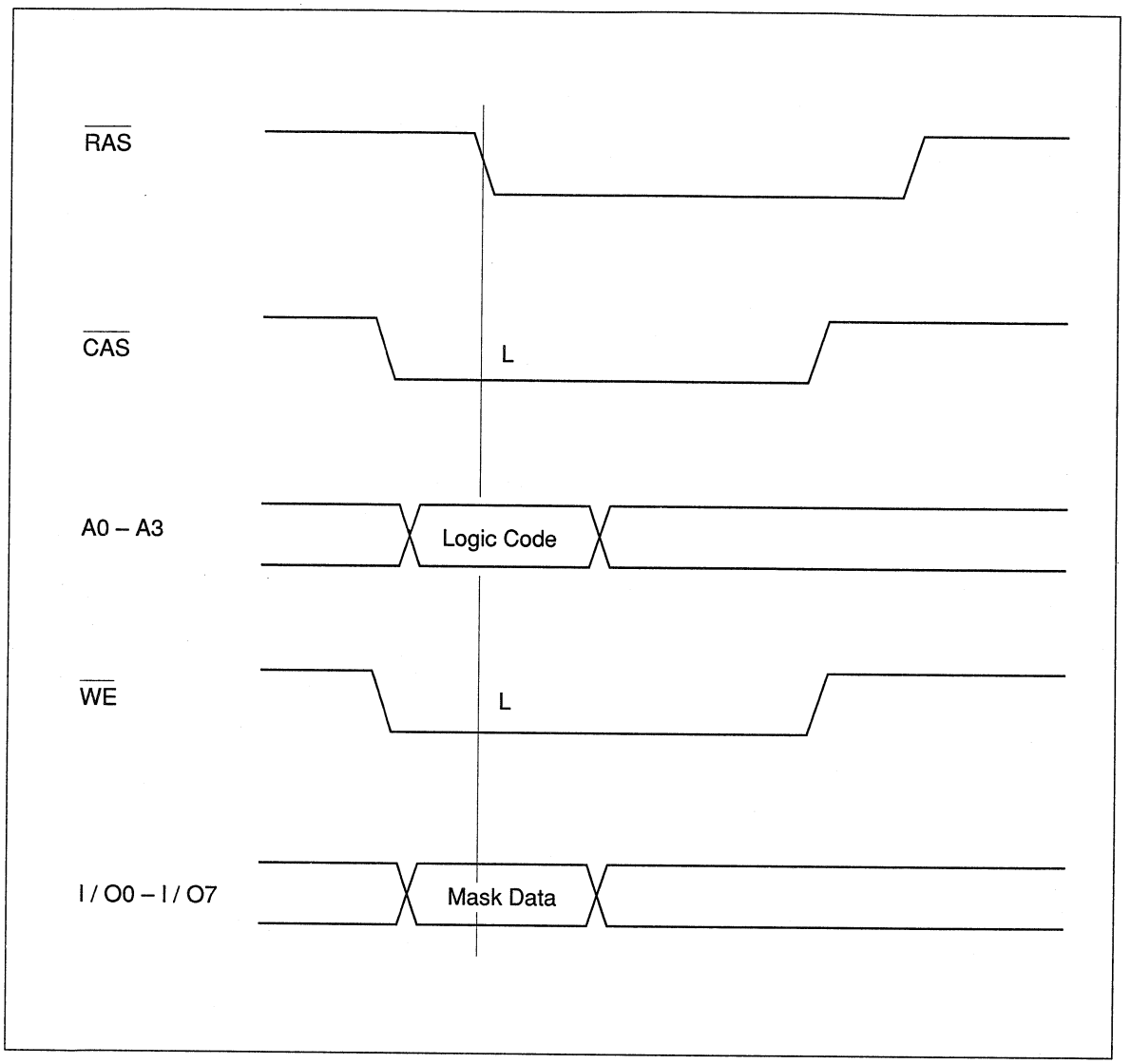


Figure 2 Logic Operation Set/Reset

Table 2 Logic Code

Logic code						
A3	**A2**	**A1**	**A0**	**Symbol**	**Write data**	**Notes**
0	0	0	0	Zero	0	Logic operation mode set
0	0	0	1	AND1	Di • Mi	
0	0	1	0	AND2	$\overline{Di}$ • Mi	
0	0	1	1	—	Mi	
0	1	0	0	AND3	Di • $\overline{Mi}$	
0	1	0	1	THROUGH	Di	Logic operation mode reset
0	1	1	0	EOR	$\overline{Di}$ • Mi + Di • $\overline{Mi}$	Logic operation mode set
0	1	1	1	OR1	Di + Mi	
1	0	0	0	NOR	$\overline{Di}$ + $\overline{Mi}$	
1	0	0	1	ENOR	Di • Mi + $\overline{Di}$ • $\overline{Mi}$	
1	0	1	0	INV1	$\overline{Di}$	
1	0	1	1	OR2	$\overline{Di}$ + Mi	
1	1	0	0	INV2	$\overline{Mi}$	
1	1	0	1	OR3	Di + $\overline{Mi}$	
1	1	1	0	NAND	$\overline{Di}$ + $\overline{Mi}$	
1	1	1	1	One	1	

Notes: Di: External data-in
Mi: The data of the memory cell

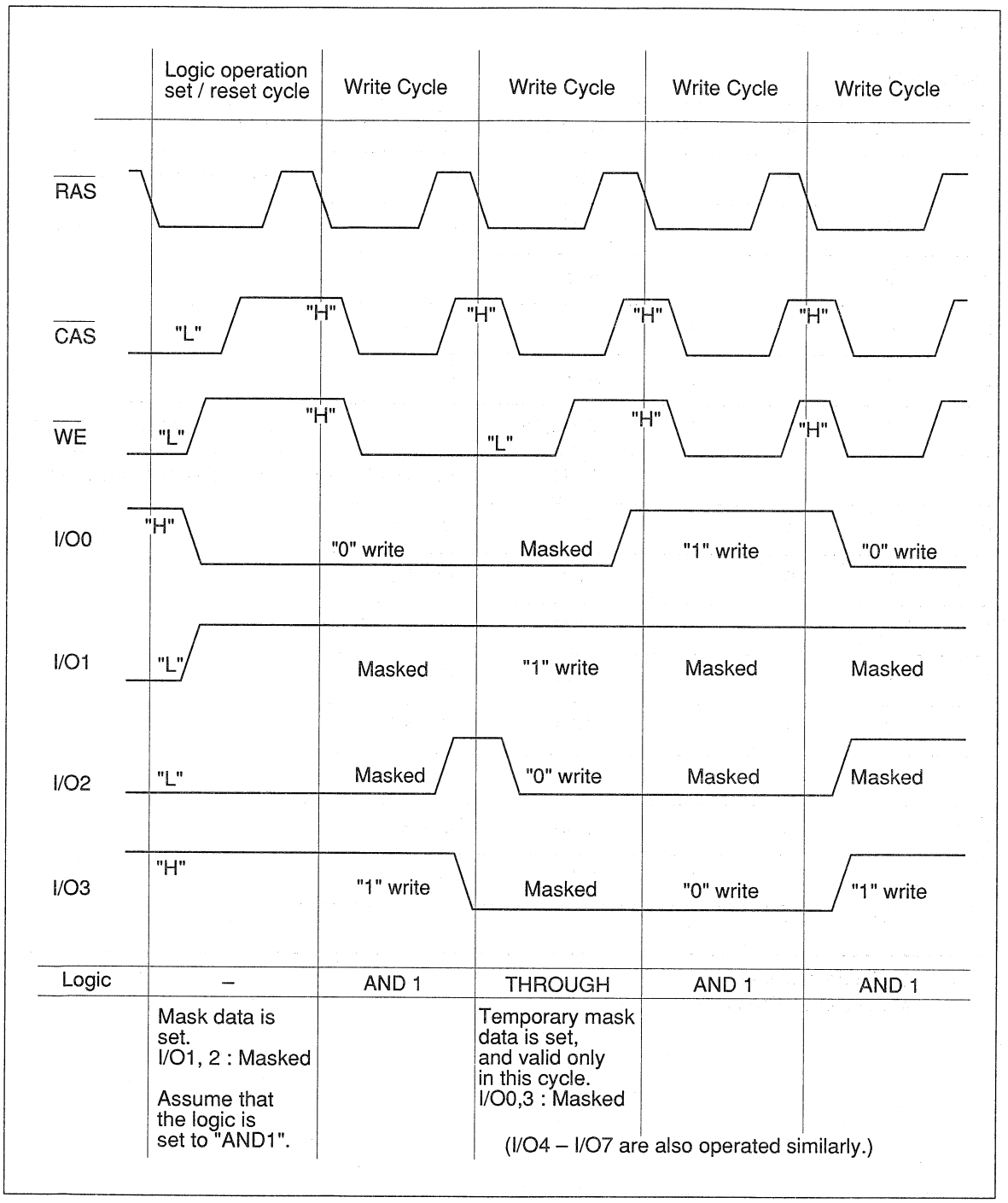


Figure 3 2 types of Mask Write Function and Logic Operation Function

Also, temporary mask data is programmed by falling $\overline{WE}$ at the falling edge of $\overline{RAS}$ in logic operation mode cycle after mask data is programmed in logic operation set/reset cycle. In this case, temporary mask data is available only for one cycle.

Logic operation is reset during temporary mask write cycle. It means that external input data is written into I/O when temporary mask data is set. Figure 4 shows write mask and logic operations. These functions are useful when RAM port is devided into frame buffer area and data area, as they save the need to reprogram logic operation codes and mask data.

Write Cycle in Logic Operation Mode (Early Write, Delayed write, Page Mode)

Write cycle after logic operation set cycle is logic operation mode cycle. In this cycle, the following read-modify-write operation is performed Internally.

(1) Reading memory data in given address into internal bus.
(2) Performing operation between input data and memory data.
(3) Writing the result of (2) into address given by (1).

Figure 4 shows sequence of raster operation. Raster operation which needs 3 cycles (destination read, operation, destination write) in normal mode can be executed in one write cycle of logic operation mode. It makes raster operation faster and simplifies peripheral hardware for raster operation.

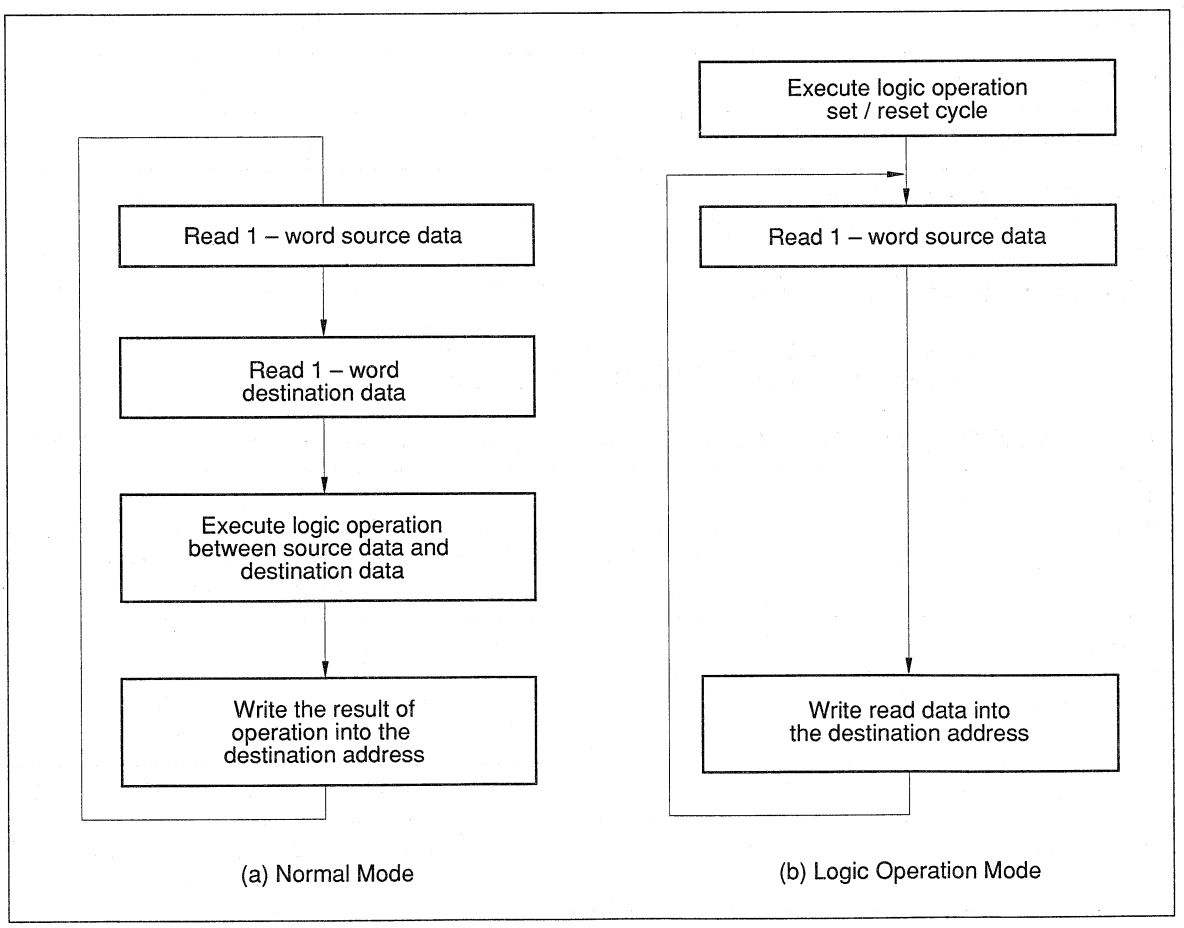


Figure 4 Sequence of Raster Operation

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage*1	V_T	–1.0 to + 7.0	V
Power supply voltage*1	V_{CC}	–0.5 to + 7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Short circuit output current	Iout	50	mA

Note : 1. Relative to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage*1	V_{CC}	4.5	5.0	5.5	V
Input high voltage*1	V_{IH}	2.4	—	6.5	V
Input low voltage*1	V_{IL}	–0.5*2	—	0.8	V

Notes: 1. All voltages referenced to V_{SS}.
2. –3.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	HM538121-10 HM538122-10 Min	Max	HM538121-11 HM538122-11 Min	Max	HM538121-12 HM538122-12 Min	Max	HM538121-15 HM538122-15 Min	Max	Unit	Test conditions RAM port	SAM port	Notes
Operating current	I_{CC1}	—	90	—	90	—	80	—	70	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min	$\overline{SE}$ = V_{IH}, SC = V_{IL}	1, 2
	I_{CC7}	—	160	—	160	—	140	—	120	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min	
Standby current	I_{CC2}	—	7	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	$\overline{SE}$ = V_{IH}, SC = V_{IL}	1, 4
	I_{CC8}	—	85	—	70	—	70	—	55	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min	
$\overline{RAS}$-only refresh current	I_{CC3}	—	90	—	90	—	80	—	70	mA	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH} t_{RC} = min	$\overline{SE}$ = V_{IH}, SC = V_{IL}	1, 2
	I_{CC9}	—	150	—	150	—	130	—	110	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min	

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (cont)

		HM538121-10 HM538122-10		HM538121-11 HM538122-11		HM538121-12 HM538122-12		HM538121-15 HM538122-15			Test conditions		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**RAM port**	**SAM port**	**Notes**
Page mode current	I_{CC4}	—	115	—	115	—	105	—	95	mA	$\overline{CAS}$ cycling	$\overline{SE}$ = V_{IH}, SC = V_{IL}	1, 3
	I_{CC10}	—	185	—	185	—	160	—	140	mA	$\overline{RAS}$ = V_{IL} t_{PC} = min	$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min	
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	—	80	—	80	—	70	—	60	mA	$\overline{RAS}$ cycling	$\overline{SE}$ = V_{IH}, SC = V_{IL}	1
	I_{CC11}	—	130	—	130	—	110	—	90	mA	t_{RC} = min	$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min	
Data transfer current	I_{CC6}	—	115	—	115	—	110	—	100	mA	$\overline{RAS}$, $\overline{CAS}$ cycling	$\overline{SE}$ = V_{IH}, SC = V_{IL}	1, 2
	I_{CC12}	—	185	—	185	—	160	—	140	mA	t_{RC} = min	$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min	
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	–10	10	µA			
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	–10	10	µA			
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V	I_{OH} = –2 mA		
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V	I_{OL} = 4.2 mA		

Notes:
1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition ($I_{I/O}$ = $I_{SI/O}$ = 0 mA).
2. Address can be changed less than three times in one $\overline{RAS}$ cycle.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. Address must be fixed.

Capacitance (Ta = 25°C, V_{CC} = 5 V, f = 1 MHz, Bias: Clock, I/O = V_{CC}, address = V_{SS})

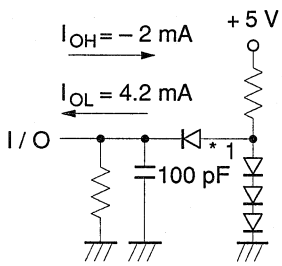
Parameter	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clocks	C_{I2}	—	—	5	pF
I/O, SI/O	$C_{I/O}$	—	—	7	pF

Note: This parameter is sampled and not 100% tested.

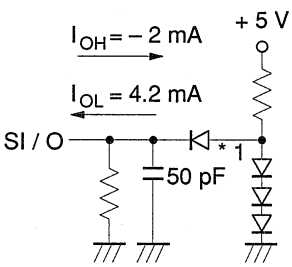
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) *1, *11

Test Conditions

- Input rise and fall time: 5 ns
- Output load: See figures
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.4 V, 2.4 V



Output Load (A)



Output Load (B)

Note: 1. Including scope and jig.

Common Parameter

Parameter	Symbol	HM538121-10 HM538122-10		HM538121-11 HM538122-11		HM538121-12 HM538122-12		HM538121-15 HM538122-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	190	—	190	—	220	—	260	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	80	—	80	—	90	—	100	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	30	10000	30	10000	35	10000	40	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	15	—	15	—	15	—	20	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	20	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	70	25	70	25	85	30	110	ns	5, 6
$\overline{RAS}$ hold time	t_{RSH}	30	—	30	—	35	—	40	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	—	100	—	120	—	150	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Transition time (rise to fall)	t_T	3	50	3	50	3	50	3	50	ns	8
Refresh period	t_{REF}	—	8	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ setup time	t_{DTS}	0	—	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ hold time	t_{DTH}	15	—	15	—	15	—	20	—	ns	
Data-in to $\overline{OE}$ delay time	t_{DZO}	0	—	0	—	0	—	0	—	ns	
Data-in to $\overline{CAS}$ delay time	t_{DZC}	0	—	0	—	0	—	0	—	ns	

Read Cycle (RAM), Page Mode Read Cycle

Parameter	Symbol	HM538121-10 HM538122-10		HM538121-11 HM538122-11		HM538121-12 HM538122-12		HM538121-15 HM538122-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	—	100	—	100	—	120	—	150	ns	2, 3
Access time from $\overline{CAS}$	t_{CAC}	—	30	—	30	—	35	—	40	ns	3, 5
Access time from $\overline{OE}$	t_{OAC}	—	30	—	30	—	35	—	40	ns	3
Address access time	t_{AA}	—	45	—	45	—	55	—	70	ns	3, 6
Output buffer turn off delay referenced to $\overline{CAS}$	t_{OFF1}	—	25	—	25	—	30	—	40	ns	7
Output buffer turn off delay referenced to $\overline{OE}$	t_{OFF2}	—	25	—	25	—	30	—	40	ns	7
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	0	—	ns	12
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	12
$\overline{RAS}$ to column address delay time	t_{RAD}	20	55	20	55	20	65	25	80	ns	5, 6
Page mode cycle time	t_{PC}	55	—	55	—	65	—	80	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	15	—	20	—	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	50	—	50	—	60	—	75	ns	
$\overline{RAS}$ pulse width in page mode	t_{RASP}	0.1	100	0.1	100	0.12	100	0.15	100	µs	

Write Cycle (RAM), Page Mode Write Cycle

		HM538121-10 HM538122-10		HM538121-11 HM538122-11		HM538121-12 HM538122-12		HM538121-15 HM538122-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Write command setup time	t_{WCS}	0	—	0	—	0	—	0	—	ns	9
Write command hold time	t_{WCH}	25	—	25	—	25	—	30	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	20	—	25	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	30	—	30	—	35	—	40	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30	—	30	—	35	—	40	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	10
Data-in hold time	t_{DH}	25	—	25	—	25	—	30	—	ns	10
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	15	—	20	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	15	—	15	—	15	—	20	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	10	—	10	—	15	—	20	—	ns	
Page mode cycle time	t_{PC}	55	—	55	—	65	—	80	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	15	—	20	—	ns	
$\overline{RAS}$ pulse width in page mode	t_{RASP}	0.1	100	0.1	100	0.12	100	0.15	100	µs	

Read-Modify-Write Cycle

		HM538121-10 HM538122-10		HM538121-11 HM538122-11		HM538121-12 HM538122-12		HM538121-15 HM538122-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Read modify write cycle time	t_{RWC}	255	—	255	—	295	—	350	—	ns	
$\overline{RAS}$ pulse width	t_{RWS}	165	10000	165	10000	195	10000	240	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	65	—	65	—	75	—	90	—	ns	9
Column address to $\overline{WE}$ delay	t_{AWD}	80	—	80	—	95	—	120	—	ns	9
$\overline{OE}$ to data-in delay time	t_{ODD}	25	—	25	—	30	—	40	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	100	—	100	—	120	—	150	ns	2, 3
Access time from $\overline{CAS}$	t_{CAC}	—	30	—	30	—	35	—	40	ns	3, 5
Access time from $\overline{OE}$	t_{OAC}	—	30	—	30	—	35	—	40	ns	3
Address access time	t_{AA}	—	45	—	45	—	55	—	70	ns	3, 6
$\overline{RAS}$ to column address delay	t_{RAD}	20	55	20	55	20	65	25	80	ns	5, 6
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	—	25	—	25	—	30	—	40	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	30	—	30	—	35	—	40	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30	—	30	—	35	—	40	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	20	—	25	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	10
Data-in hold time	t_{DH}	25	—	25	—	25	—	30	—	ns	10
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	15	—	20	—	ns	

Read-Modify-Write Cycle (cont)

		HM538121-10 HM538122-10		HM538121-11 HM538122-11		HM538121-12 HM538122-12		HM538121-15 HM538122-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	15	—	15	—	15	—	20	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	10	—	10	—	15	—	20	—	ns	

Refresh Cycle

		HM538121-10 HM538122-10		HM538121-11 HM538122-11		HM538121-12 HM538122-12		HM538121-15 HM538122-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20	—	20	—	25	—	30	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

Transfer Cycle

Parameter	Symbol	HM538121-10 HM538122-10 Min	HM538121-10 HM538122-10 Max	HM538121-11 HM538122-11 Min	HM538121-11 HM538122-11 Max	HM538121-12 HM538122-12 Min	HM538121-12 HM538122-12 Max	HM538121-15 HM538122-15 Min	HM538121-15 HM538122-15 Max	Unit	Note
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	15	—	20	—	ns	
$\overline{SE}$ to $\overline{RAS}$ setup time	t_{ES}	0	—	0	—	0	—	0	—	ns	
$\overline{SE}$ to $\overline{RAS}$ hold time	t_{EH}	15	—	15	—	15	—	20	—	ns	
$\overline{RAS}$ to SC delay time	t_{SRD}	25	—	30	—	30	—	35	—	ns	
SC to $\overline{RAS}$ setup time	t_{SRS}	30	—	40	—	40	—	45	—	ns	
$\overline{DT}$ hold time from $\overline{RAS}$	t_{RDH}	80	—	90	—	90	—	110	—	ns	
$\overline{DT}$ hold time from $\overline{CAS}$	t_{CDH}	20	—	30	—	30	—	45	—	ns	
Last SC to $\overline{DT}$ delay time	t_{SDD}	5	—	5	—	5	—	10	—	ns	
First SC to $\overline{DT}$ hold time	t_{SDH}	20	—	25	—	25	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ lead time	t_{DTL}	50	—	50	—	50	—	50	—	ns	
$\overline{DT}$ hold time referenced to $\overline{RAS}$ high	t_{DTHH}	20	—	25	—	25	—	30	—	ns	
$\overline{DT}$ precharge time	t_{DTP}	30	—	35	—	35	—	40	—	ns	
Serial data input delay time from $\overline{RAS}$	t_{SID}	50	—	60	—	60	—	75	—	ns	
Serial data input to $\overline{RAS}$ delay time	t_{SZR}	10	—	10	—	10	—	10	—	ns	
Serial output buffer turn-off delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	60	10	75	ns	7
$\overline{RAS}$ to Sout (Low-Z) delay time	t_{RLZ}	5	—	10	—	10	—	10	—	ns	
Serial clock cycle time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
Serial clock cycle time	t_{SCC2}	40	—	40	—	40	—	60	—	ns	13
Access time from SC	t_{SCA}	—	30	—	35	—	40	—	50	ns	4
Serial data out hold time	t_{SOH}	7	—	7	—	7	—	7	—	ns	4

Transfer Cycle (cont)

		HM538121-10 HM538122-10		HM538121-11 HM538122-11		HM538121-12 HM538122-12		HM538121-15 HM538122-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
SC pulse width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	20	—	20	—	25	—	ns	

Serial Read Cycle

		HM538121-10 HM538122-10		HM538121-11 HM538122-11		HM538121-12 HM538122-12		HM538121-15 HM538122-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Serial clock cycle time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
Access time from SC	t_{SCA}	—	30	—	35	—	40	—	50	ns	4
Access time from $\overline{SE}$	t_{SEA}	—	25	—	30	—	30	—	40	ns	4
Serial data-out hold time	t_{SOH}	7	—	7	—	7	—	7	—	ns	4
SC pulse width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial output buffer turn-off delay from $\overline{SE}$	t_{SEZ}	—	25	—	25	—	25	—	30	ns	7

Serial Write Cycle

Parameter	Symbol	HM538121-10 HM538122-10 Min	Max	HM538121-11 HM538122-11 Min	Max	HM538121-12 HM538122-12 Min	Max	HM538121-15 HM538122-15 Min	Max	Unit	Note
Serial clock cycle time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
SC pulse width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	20	—	20	—	25	—	ns	
Serial write enable setup time	t_{SWS}	0	—	0	—	0	—	0	—	ns	
Serial write enable hold time	t_{SWH}	30	—	35	—	35	—	50	—	ns	
Serial write disable setup time	t_{SWIS}	0	—	0	—	0	—	0	—	ns	
Serial write disable hold time	t_{SWIH}	30	—	35	—	35	—	50	—	ns	

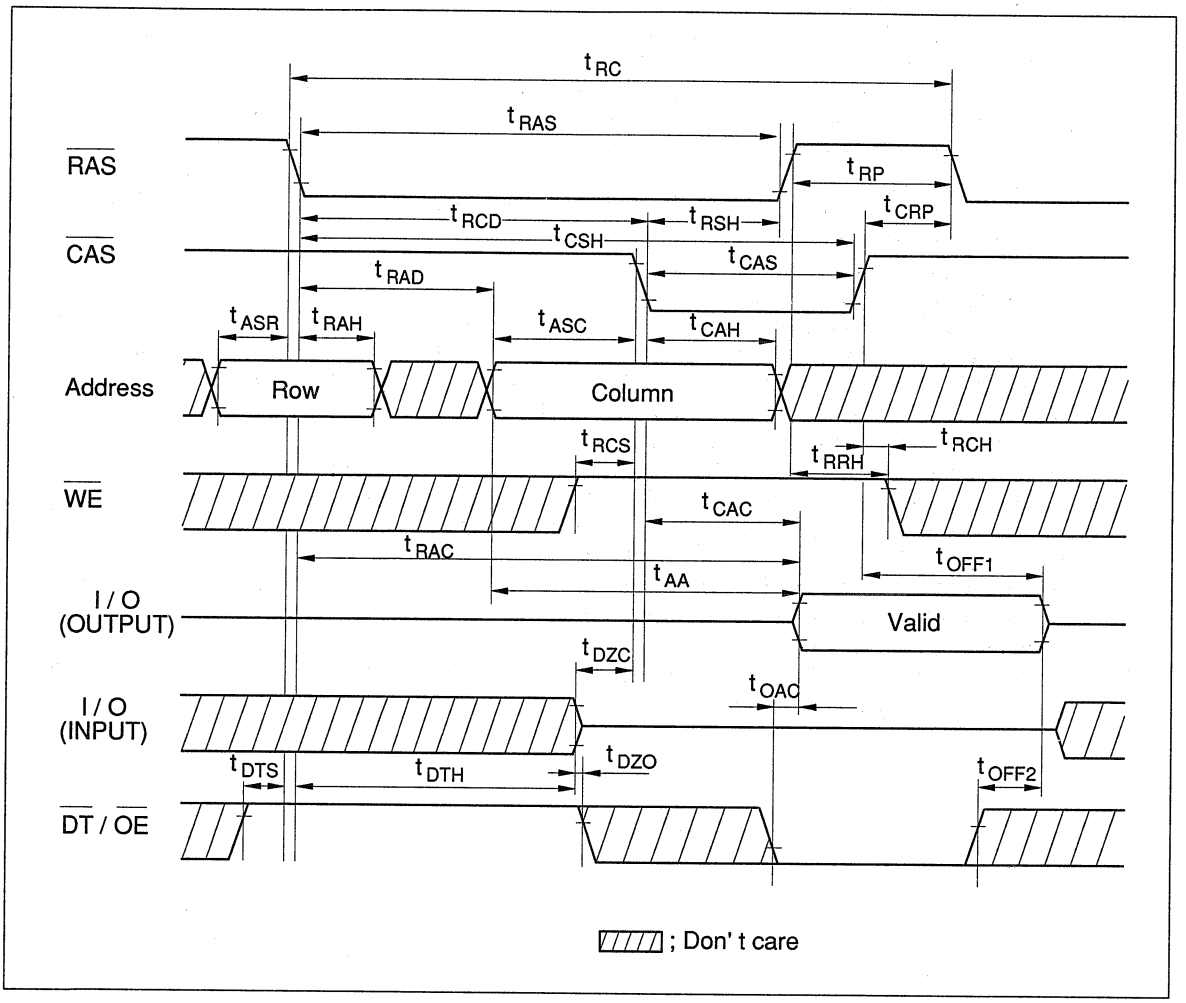
Logic Operation Mode

Parameter	Symbol	HM538122-10 Min	Max	HM538122-11 Min	Max	HM538122-12 Min	Max	HM538122-15 Min	Max	Unit	Note
$\overline{CAS}$ hold time (logic operation set/reset cycle)	t_{FCHR}	90	—	90	—	100	—	120	—	ns	
$\overline{RAS}$ pulse width in write cycle	t_{RFS}	140	10000	140	10000	165	10000	200	10000	ns	
$\overline{CAS}$ pulse width in write cycle	t_{CFS}	60	—	60	—	70	—	80	—	ns	
$\overline{CAS}$ hold time in write cycle	t_{FCSH}	140	—	140	—	165	—	200	—	ns	
$\overline{RAS}$ hold time in write cycle	t_{FRSH}	60	—	60	—	70	—	80	—	ns	
Write cycle time	t_{FRC}	230	—	230	—	265	—	310	—	ns	
Page mode cycle time (write cycle)	t_{FPC}	85	—	85	—	100	—	120	—	ns	
Pulse width in page mode	t_{RFSP}	0.14	100	0.14	100	0.165	100	0.2	100	µs	

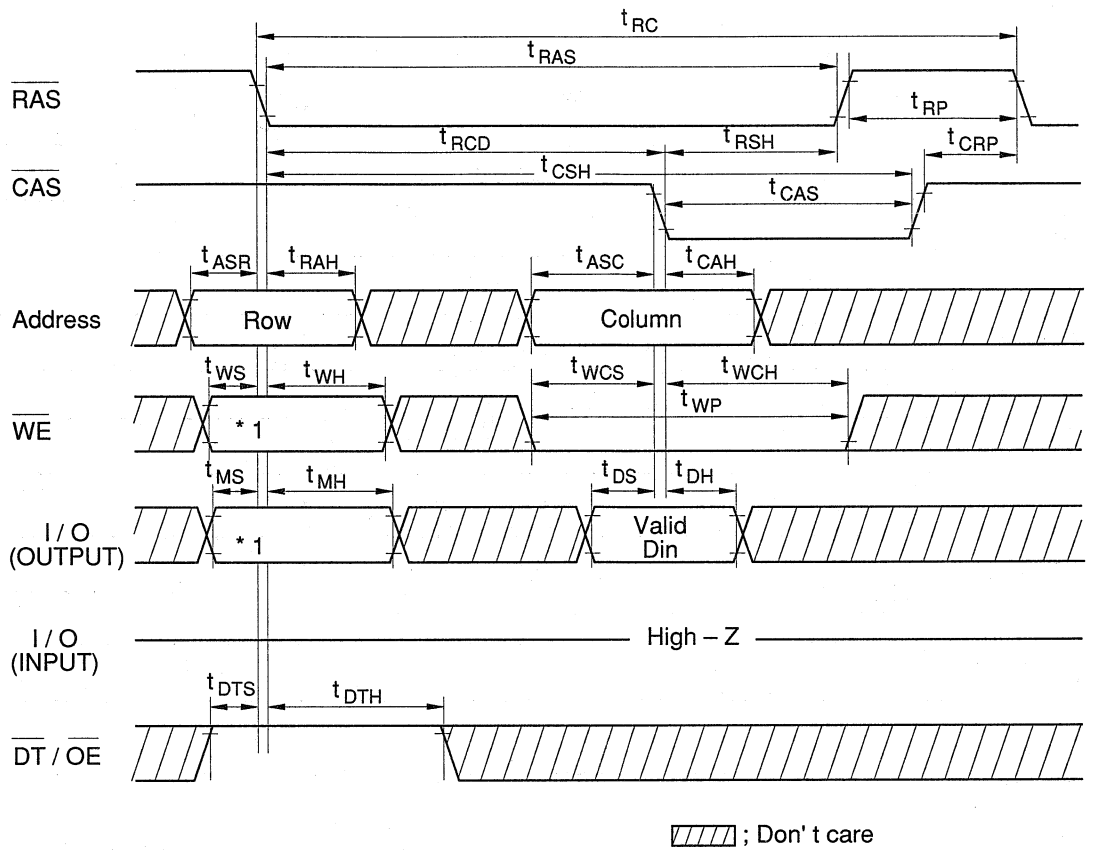
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
   If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
5. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
6. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
7. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition (V_{OH} –200 mV, V_{OL} +200 mV).
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
9. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
   When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read-modify-write cycle; the data of the selected address is read out from a data output pin and input data is written into the selected address. In this case, impedance on I/O pins is controlled by $\overline{OE}$.
10. These parameters are referenced to $\overline{CAS}$ falling edge in early write cycles or to $\overline{WE}$ falling edge in delayed write or read-modify-write cycles.
11. After power-up, pause for 100 µs or more and execute at least 8 initialization cycles (normal memory cycles or refresh cycles), then start operation.
12. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.
13. t_{SCC2} is defined as the last SAM cycle time before read transfer in read transfer cycle (1).
14. When I/O or SI/O is in the output state, data input signals must not be applied to I/O or SI/O.
15. When $\overline{SE}$ is low after power on, SI/O is in the output state. Data input signals must not be applied to SI/O in this time.
16. When $\overline{CAS}$ and $\overline{DT/OE}$ are both low after power on, it is possible that I/O is in the output state. Data input signals must not be applied to I/O in this time.

Timing Waveforms

Read Cycle

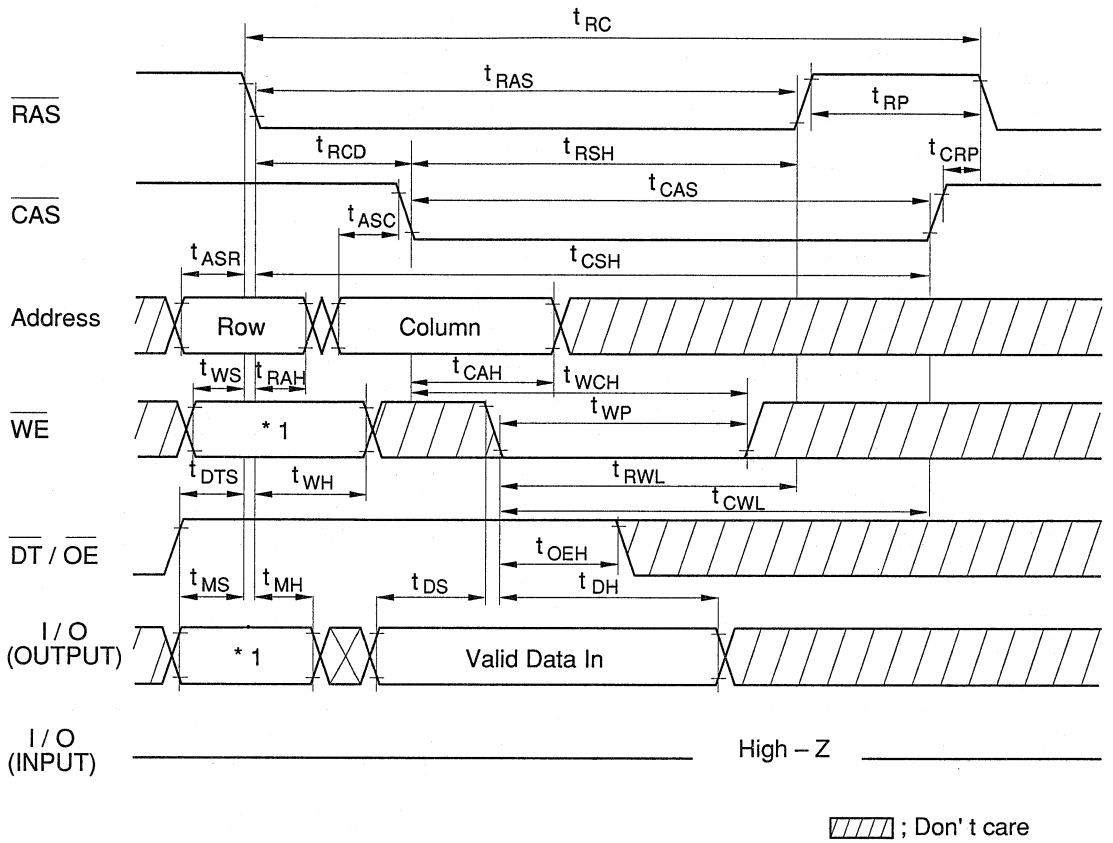


Early Write Cycle



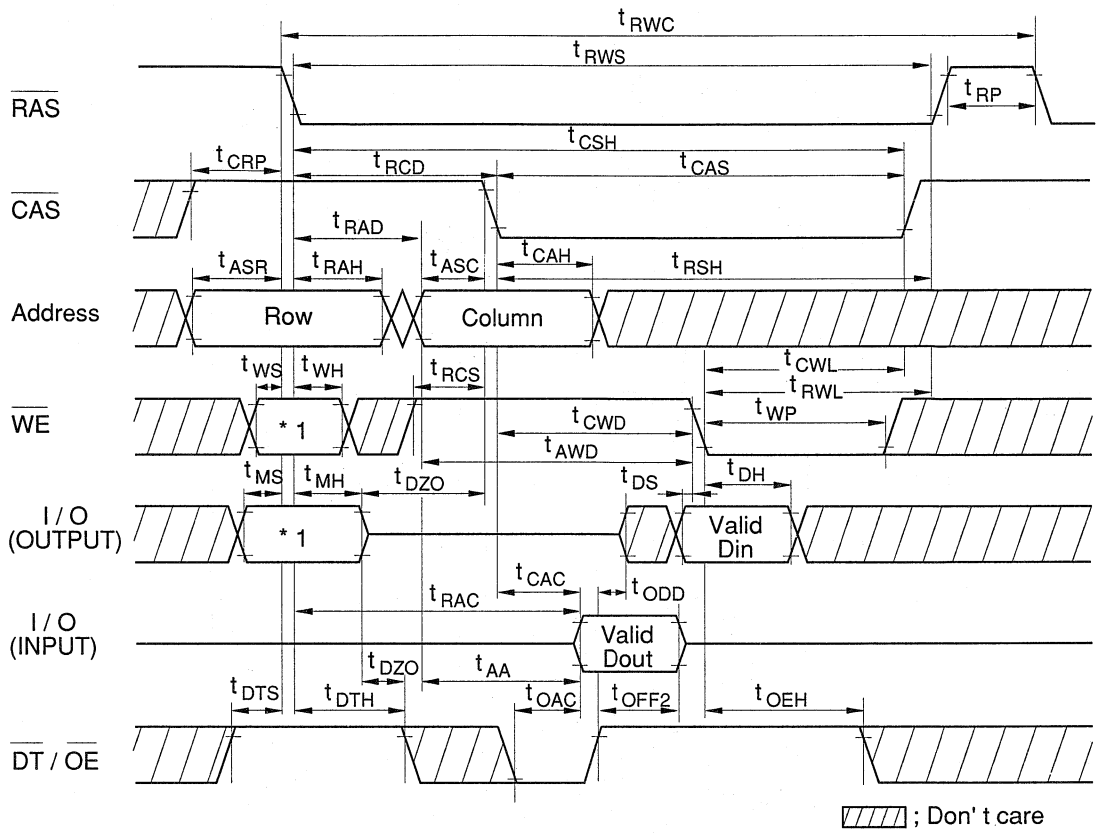
Note: 1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Delayed Write Cycle



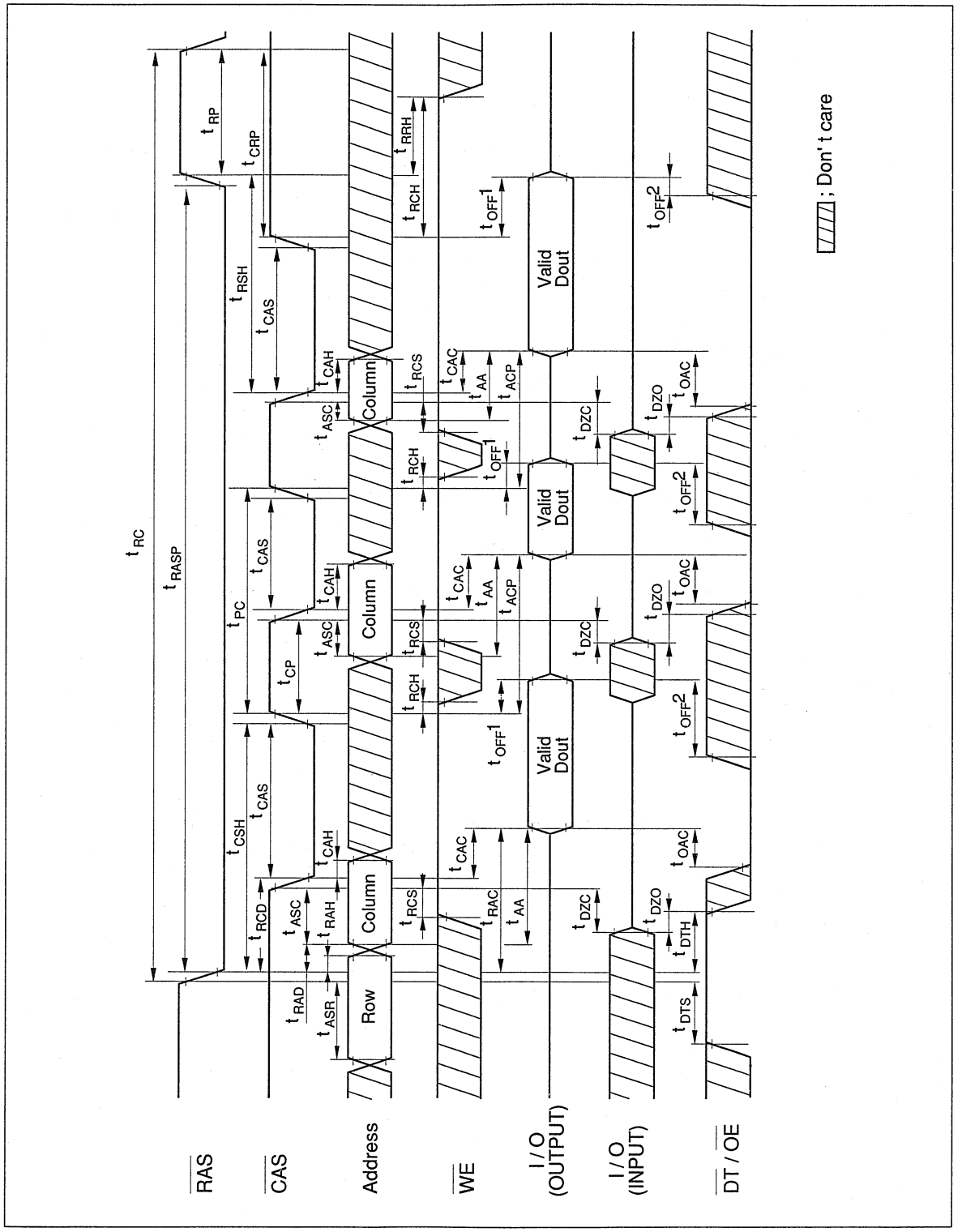
Note: 1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Read-Modify-Write Cycle

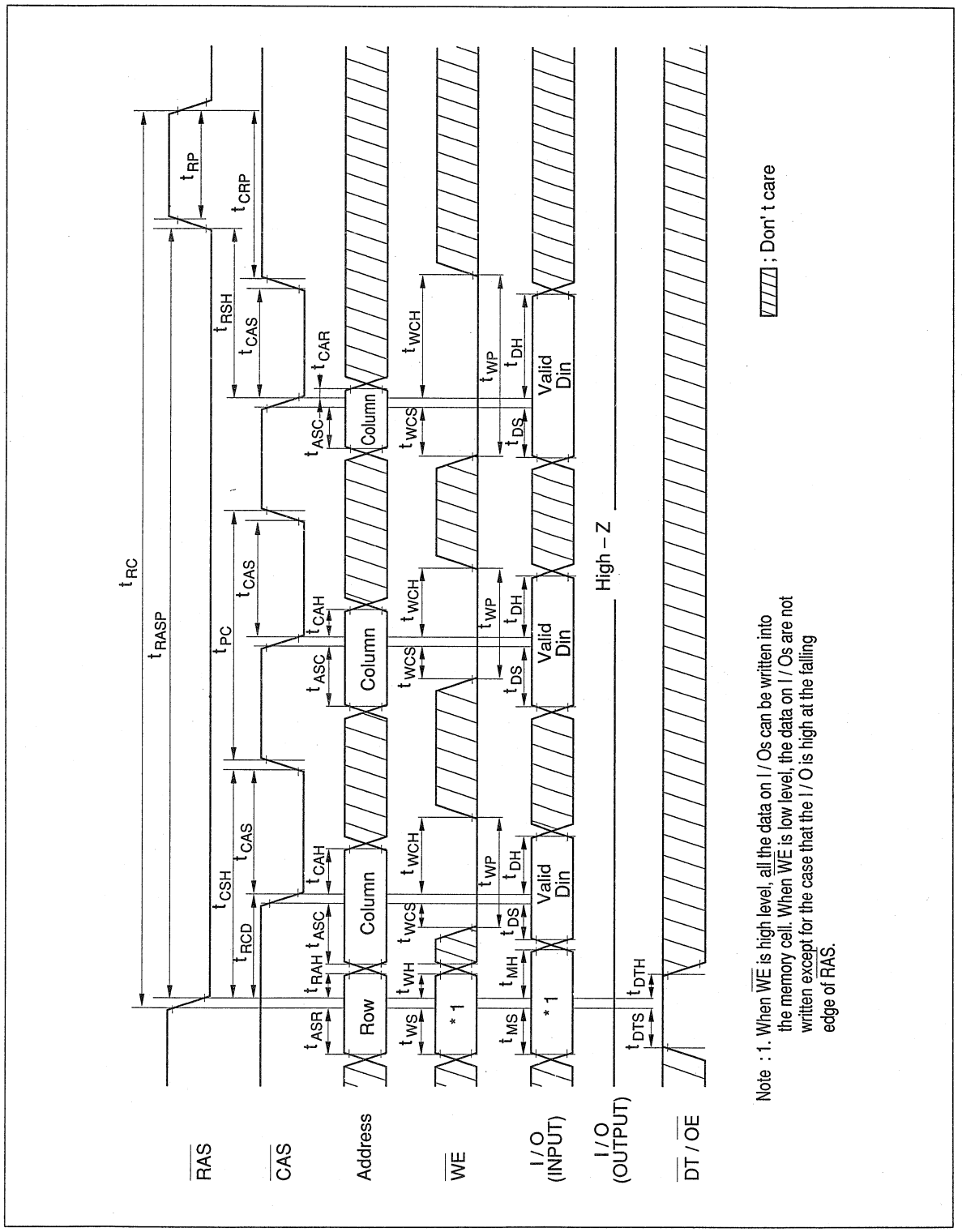


Note: 1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Read Cycle

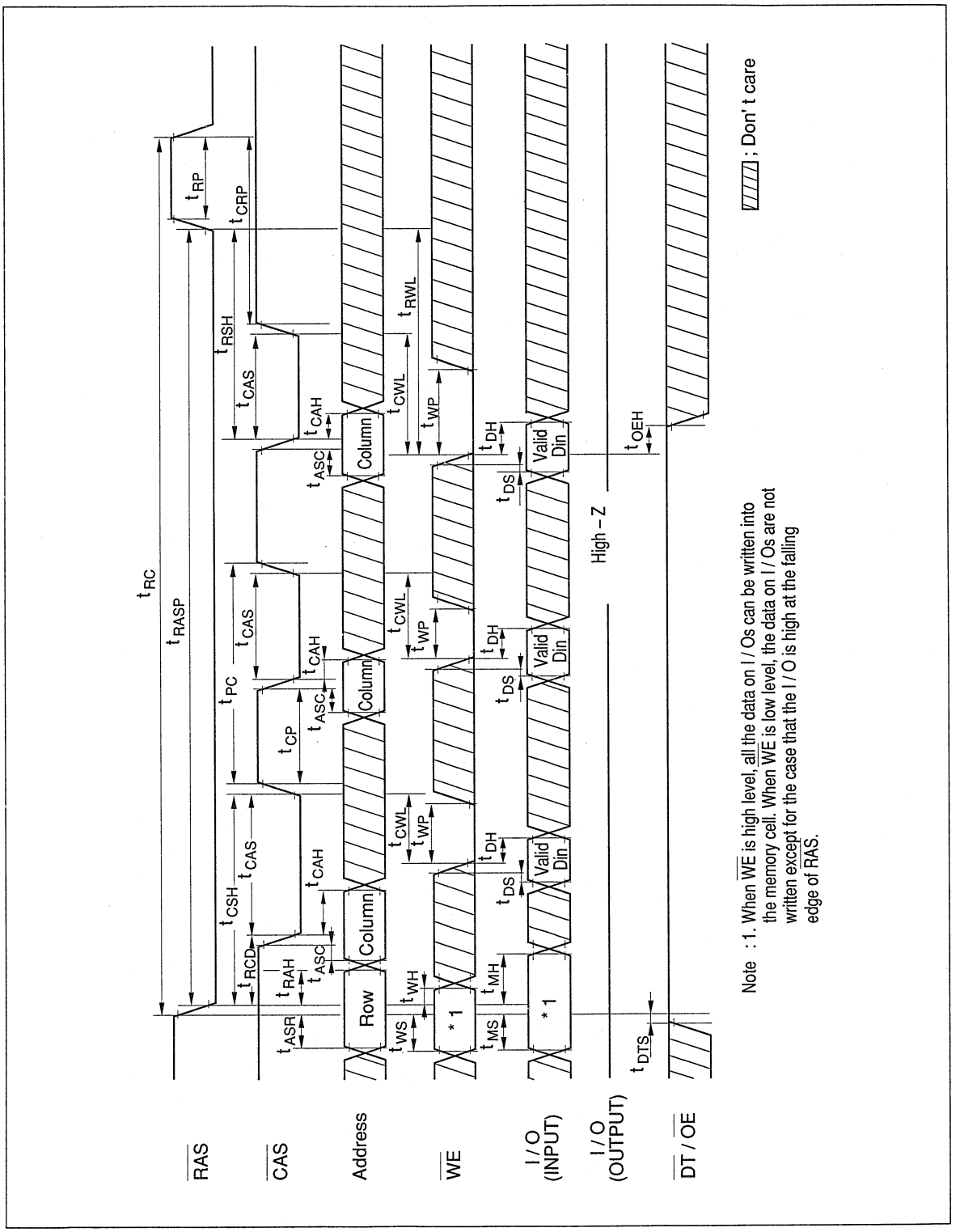


Page Mode Write Cycle (Early Write)



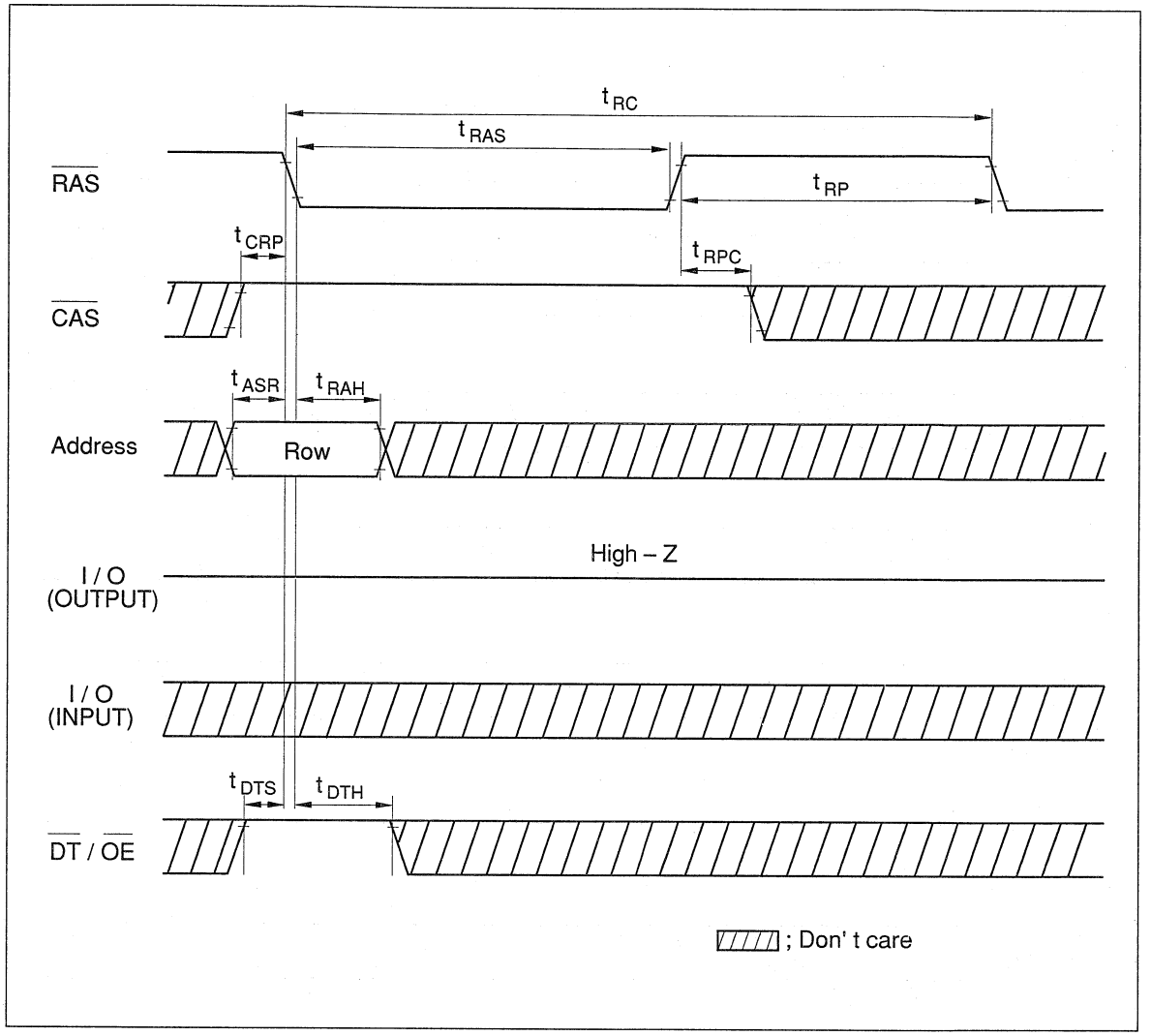
Note : 1. When $\overline{WE}$ is high level, all the data on I / Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I / Os are not written except for the case that the I / O is high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Delayed Write)

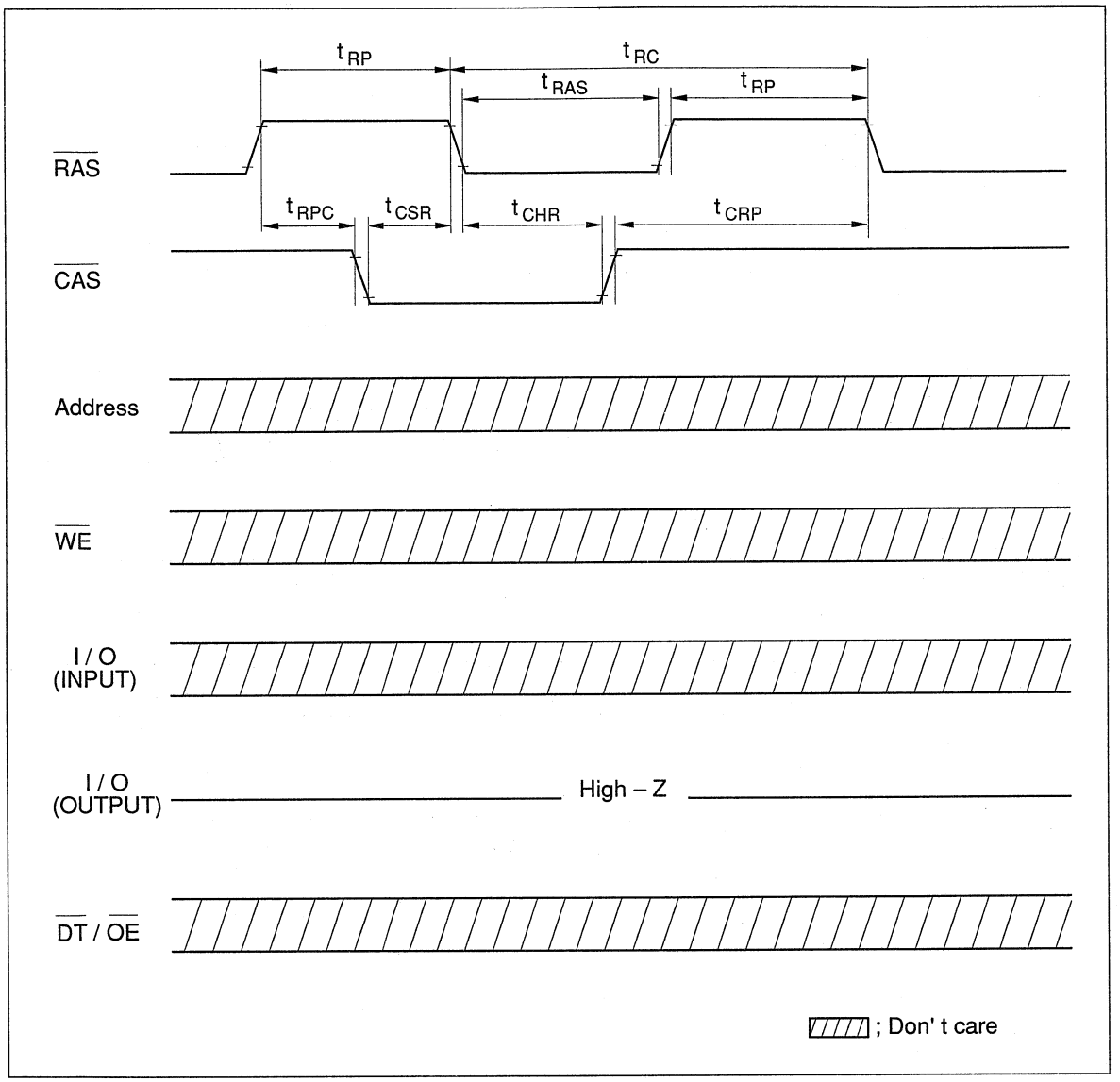


Note : 1. When $\overline{WE}$ is high level, all the data on I / Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I / Os are not written except for the case that the I / O is high at the falling edge of $\overline{RAS}$.

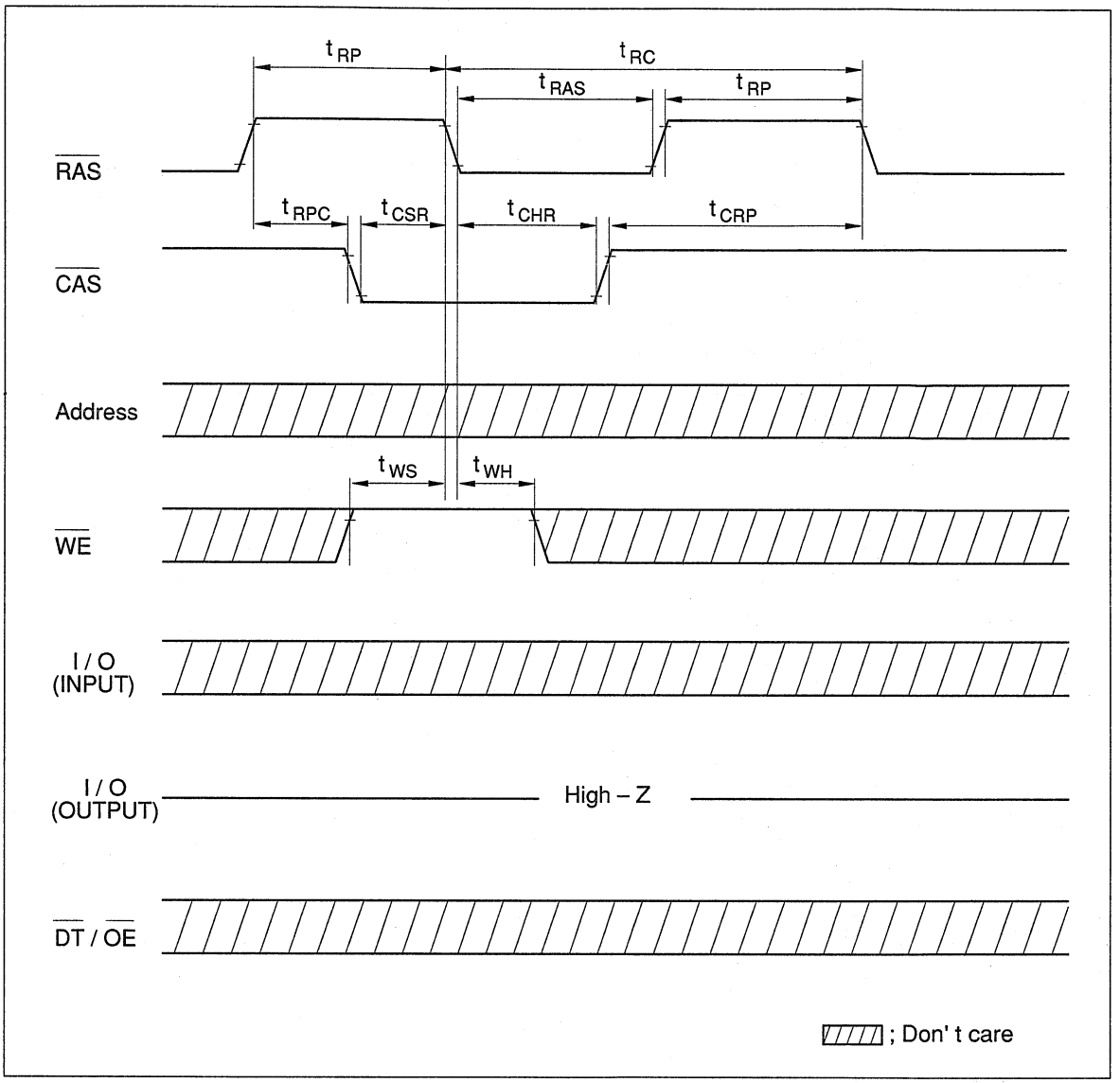
$\overline{RAS}$-Only Refresh Cycle



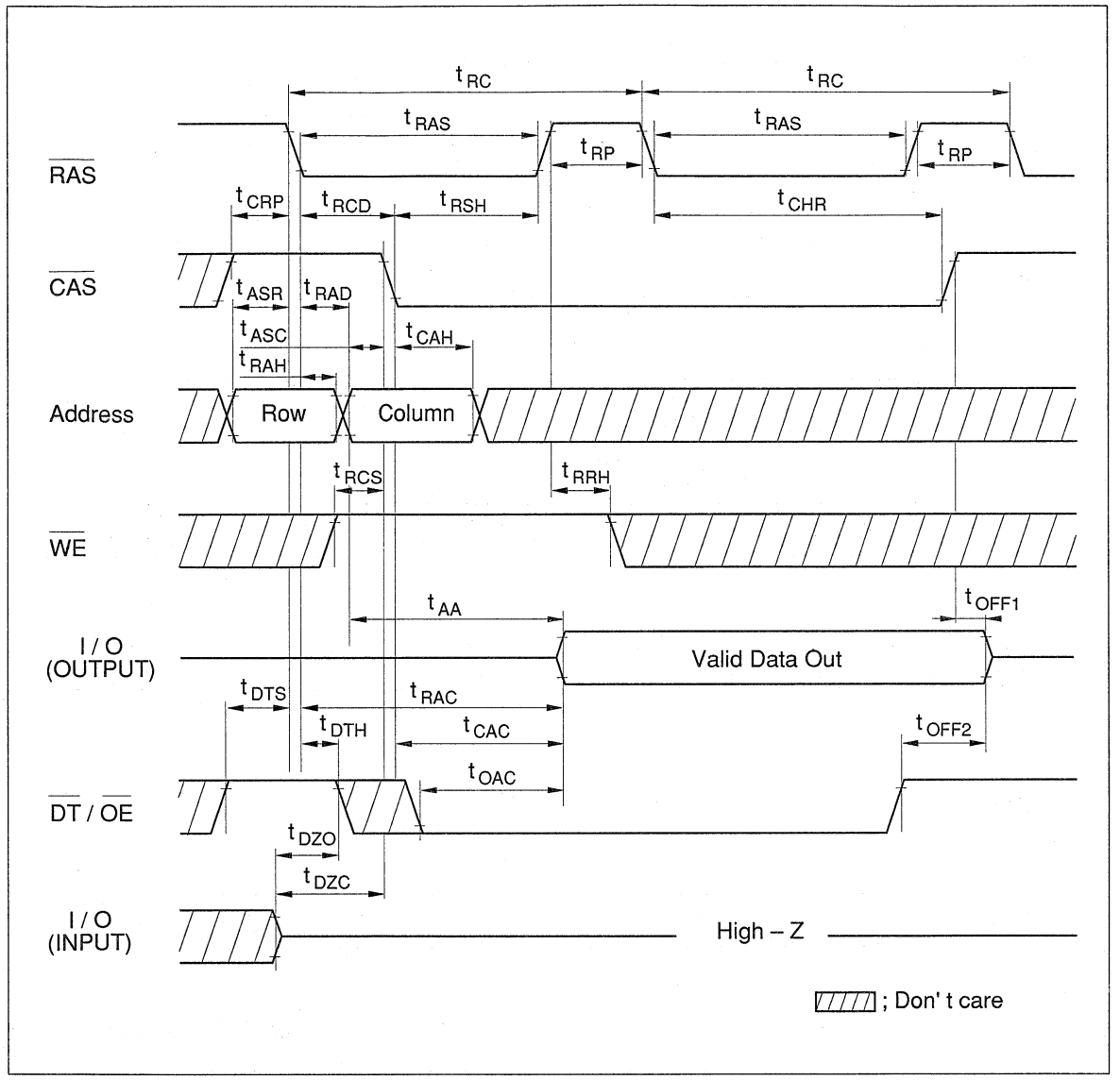
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle (HM538121 Series)



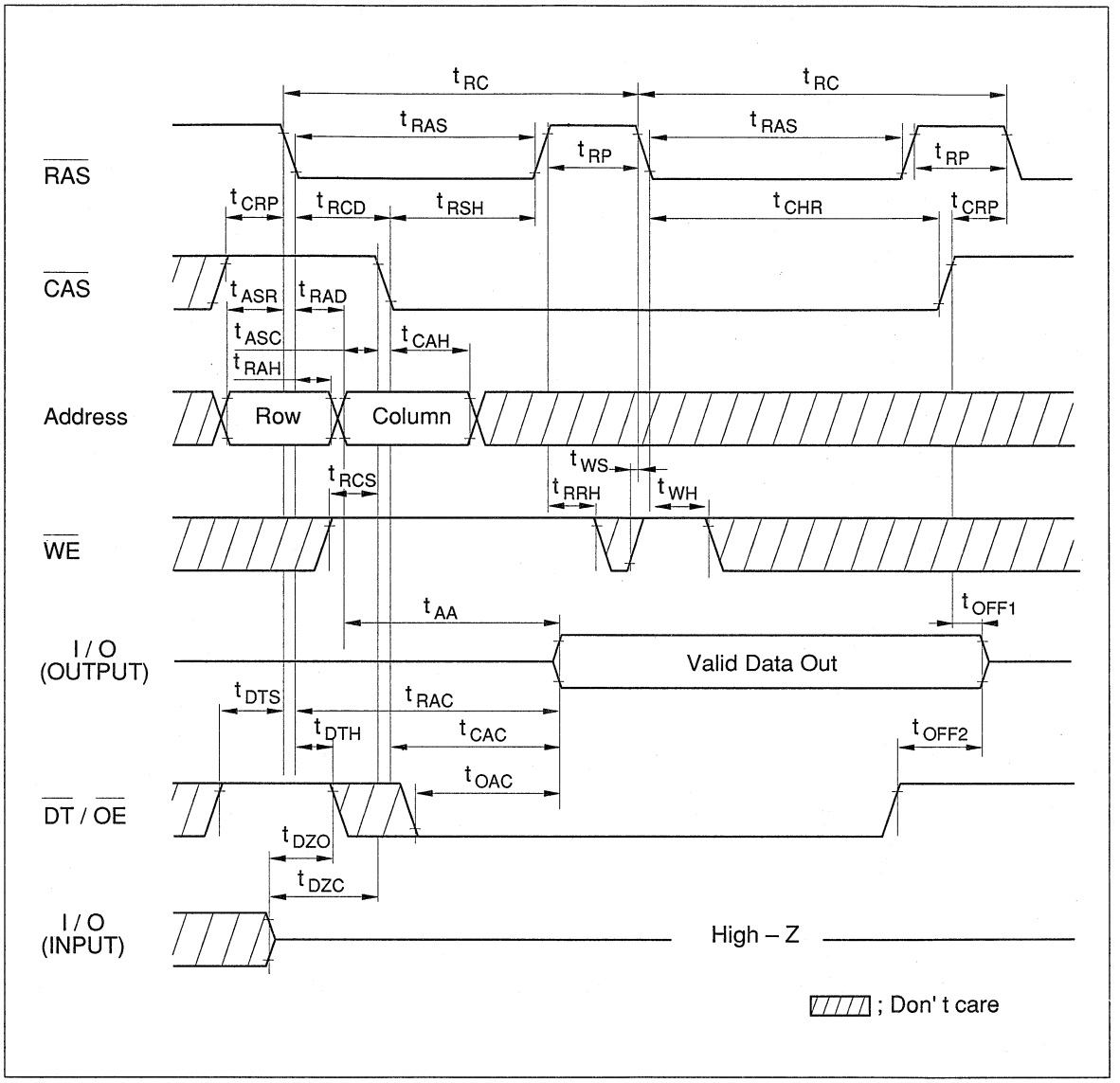
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle (HM538122 Series)



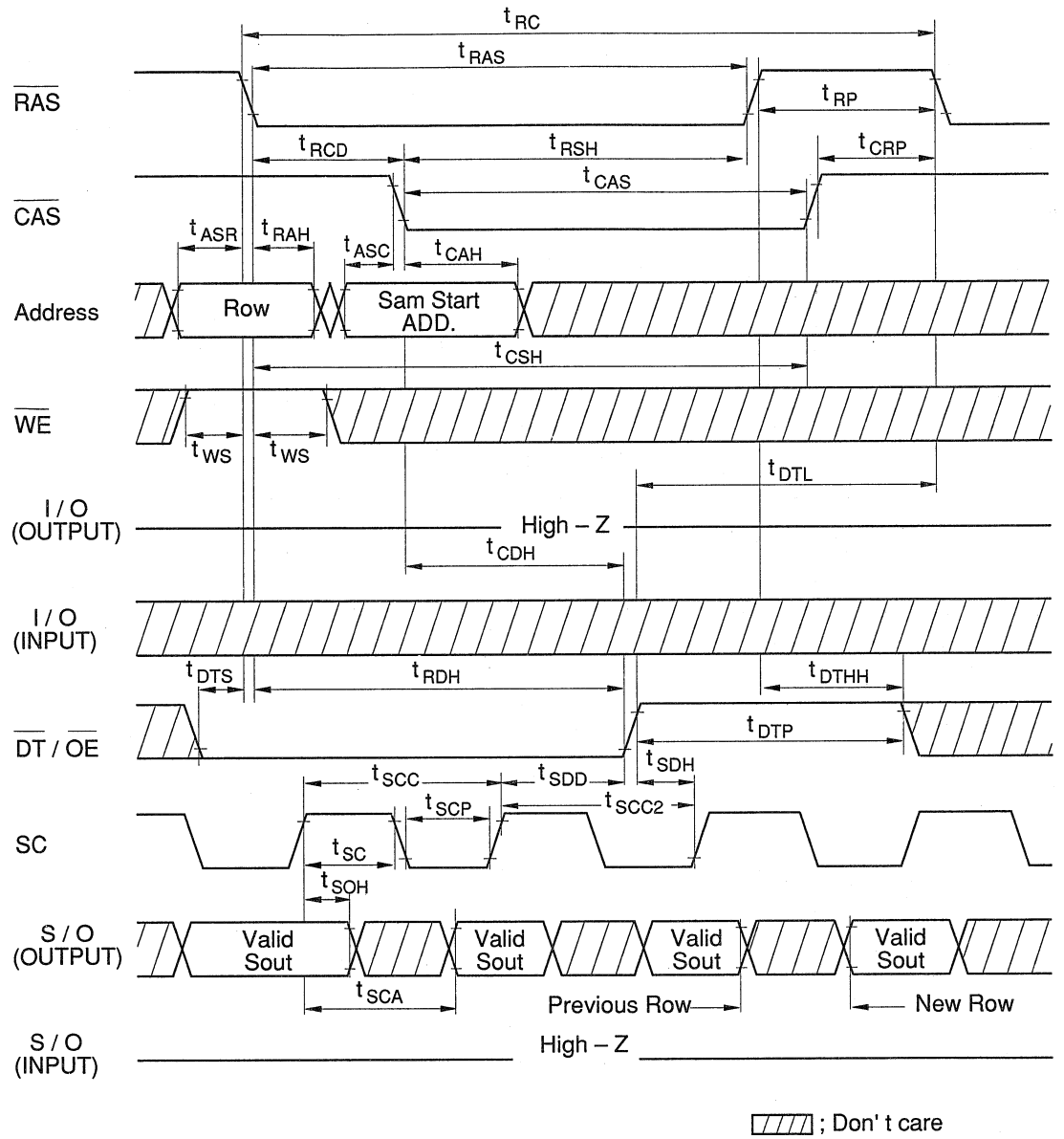
Hidden Refresh Cycle (HM538121 Series)



Hidden Refresh Cycle (HM538122 Series)

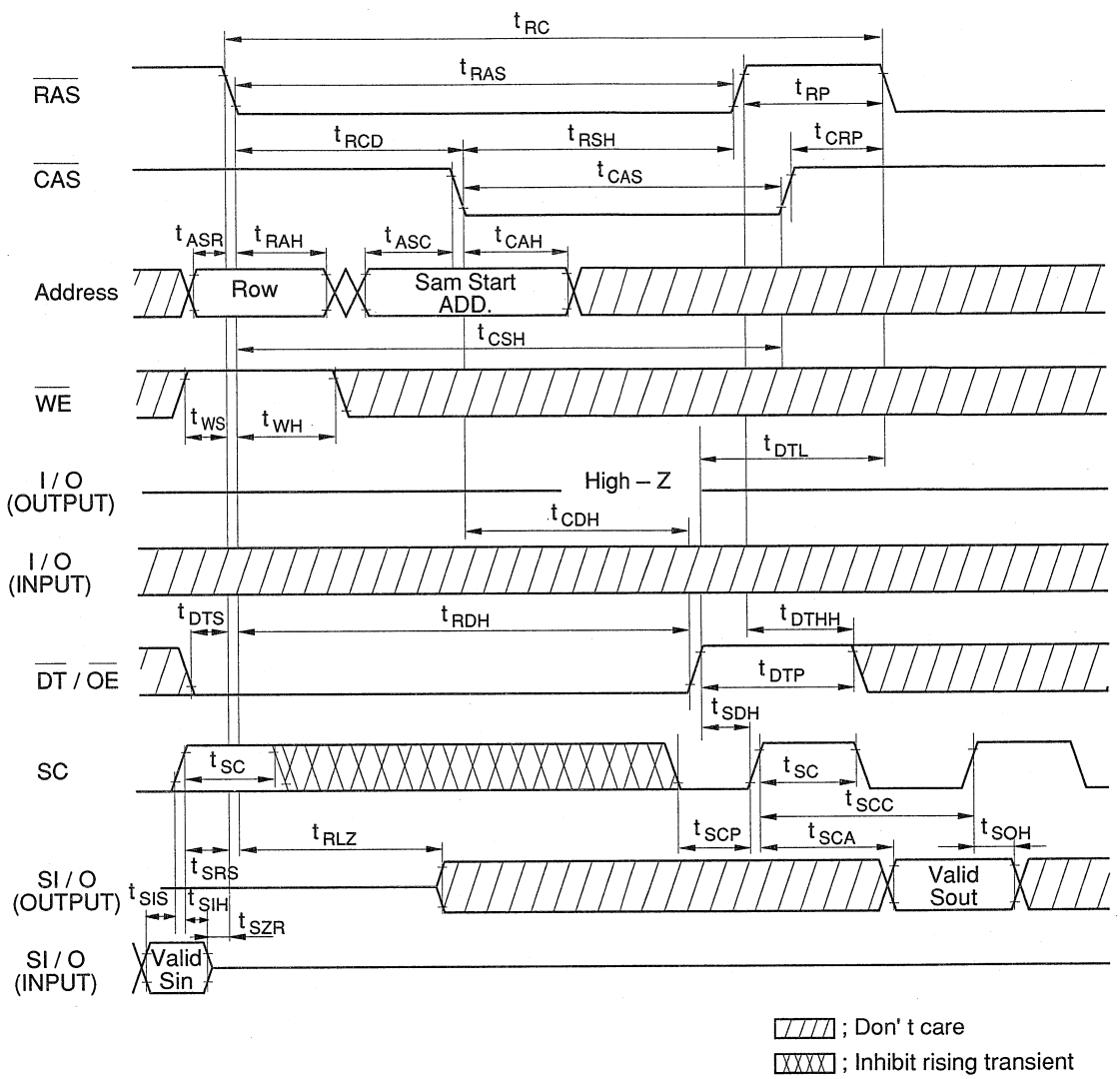


Read Transfer Cycle (1) *1, *2



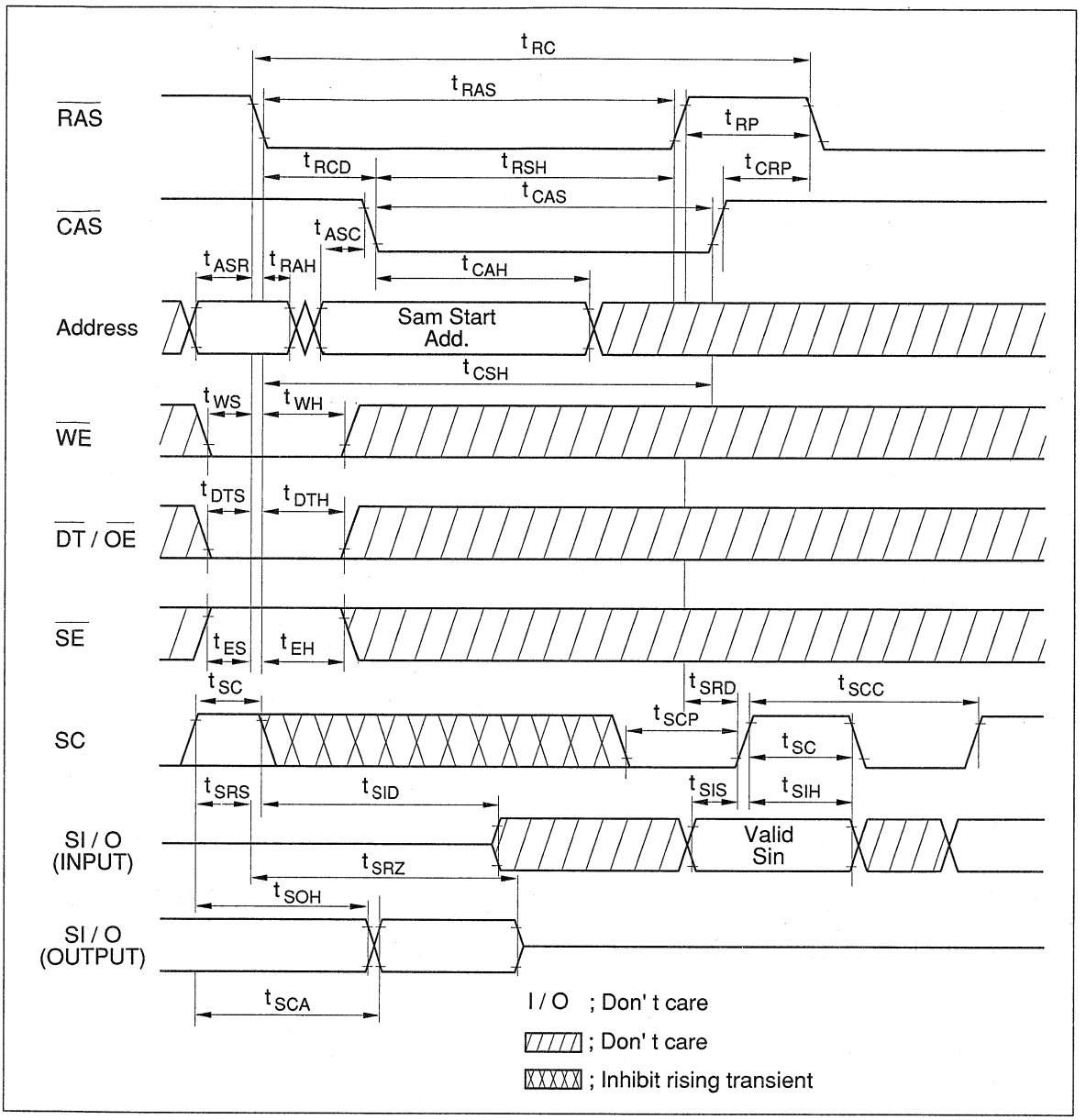
Notes: 1. When the previous data transfer cycle is a read transfer cycle, it is defined as read transfer cycle (1).
2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)

Read Transfer Cycle (2) *1, *2

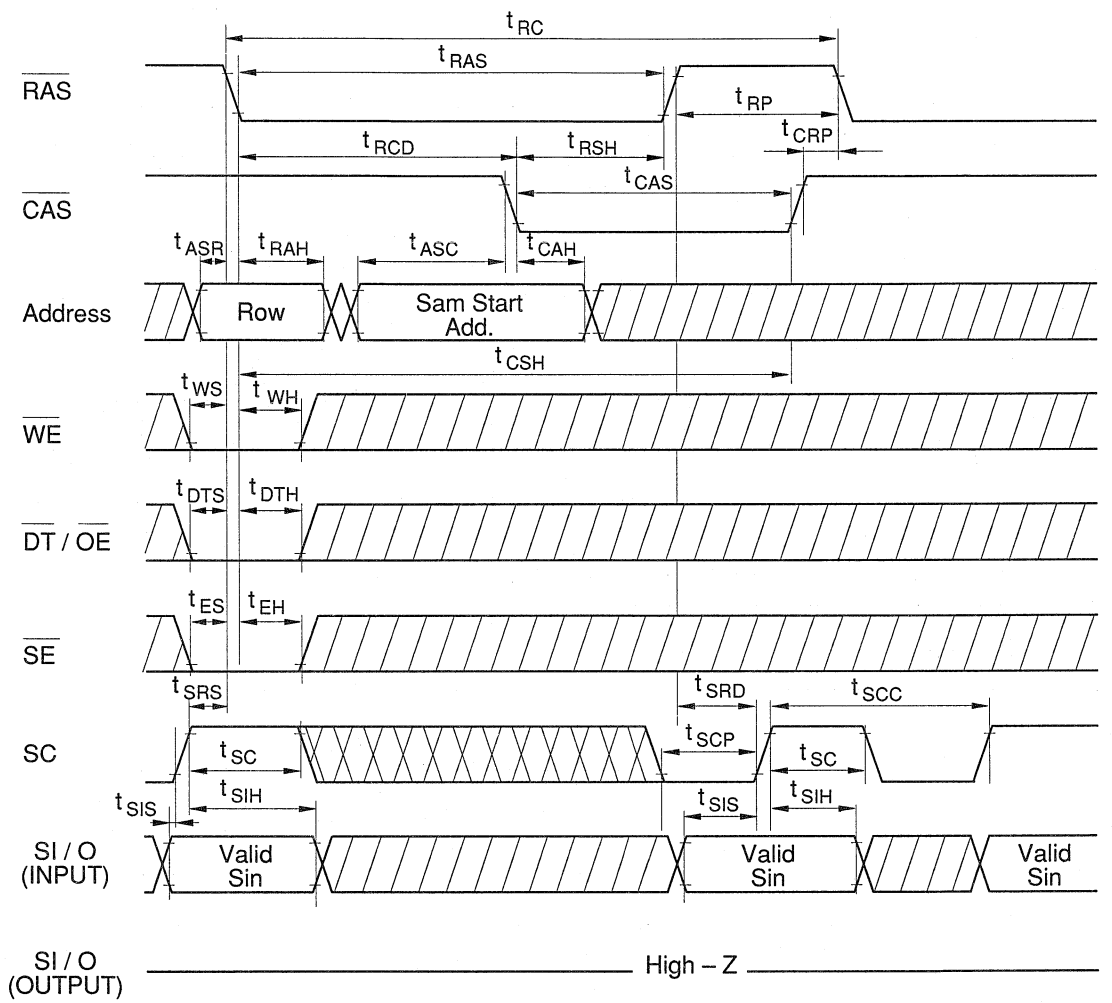


Notes: 1. When the previous data transfer cycle is a write or pseudo transfer cycle, it is defined as read transfer cycle (2).
2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)

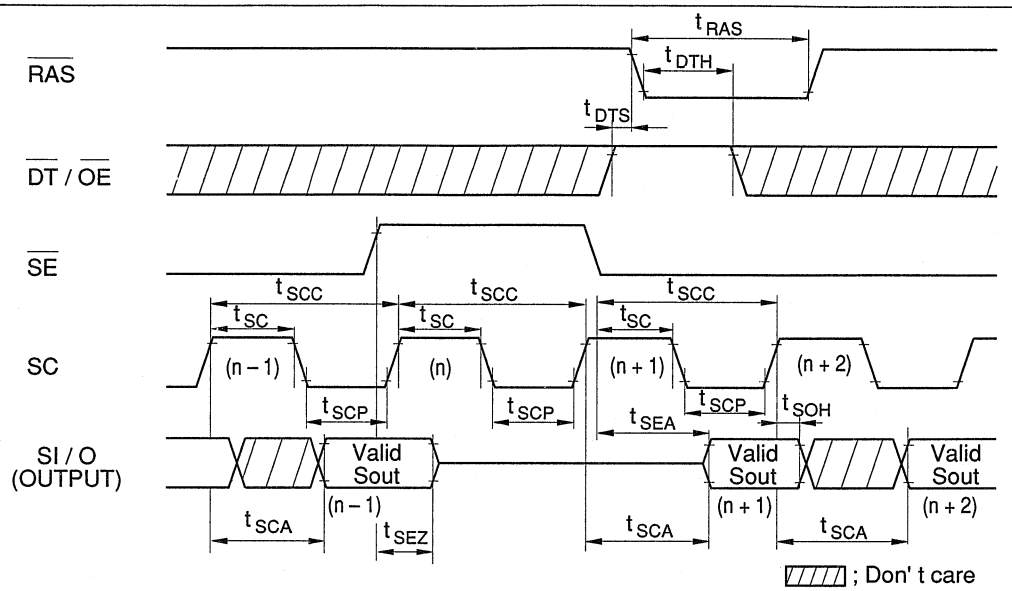
Pseudo Transfer Cycle



Write Transfer Cycle

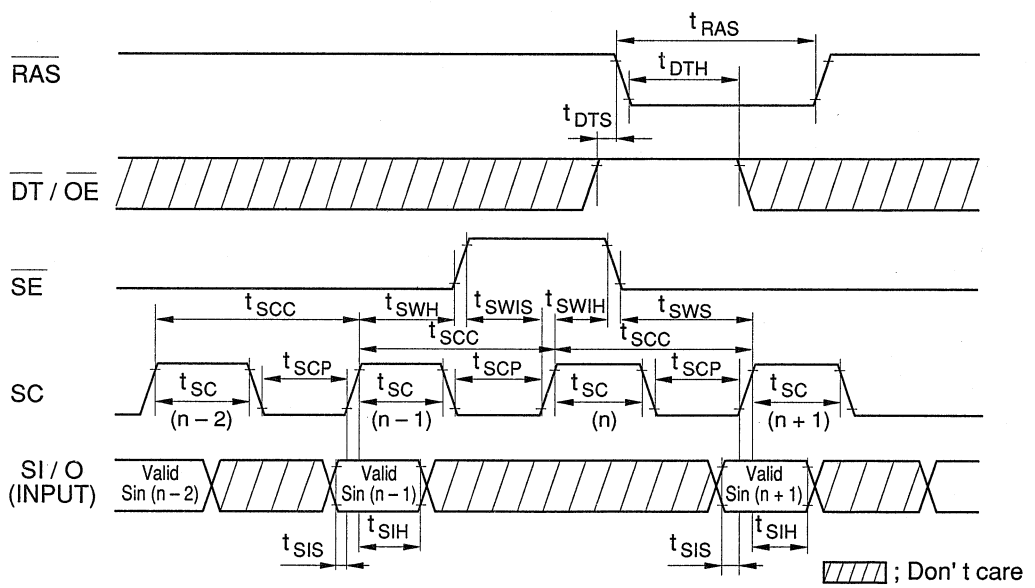


Serial Read Cycle



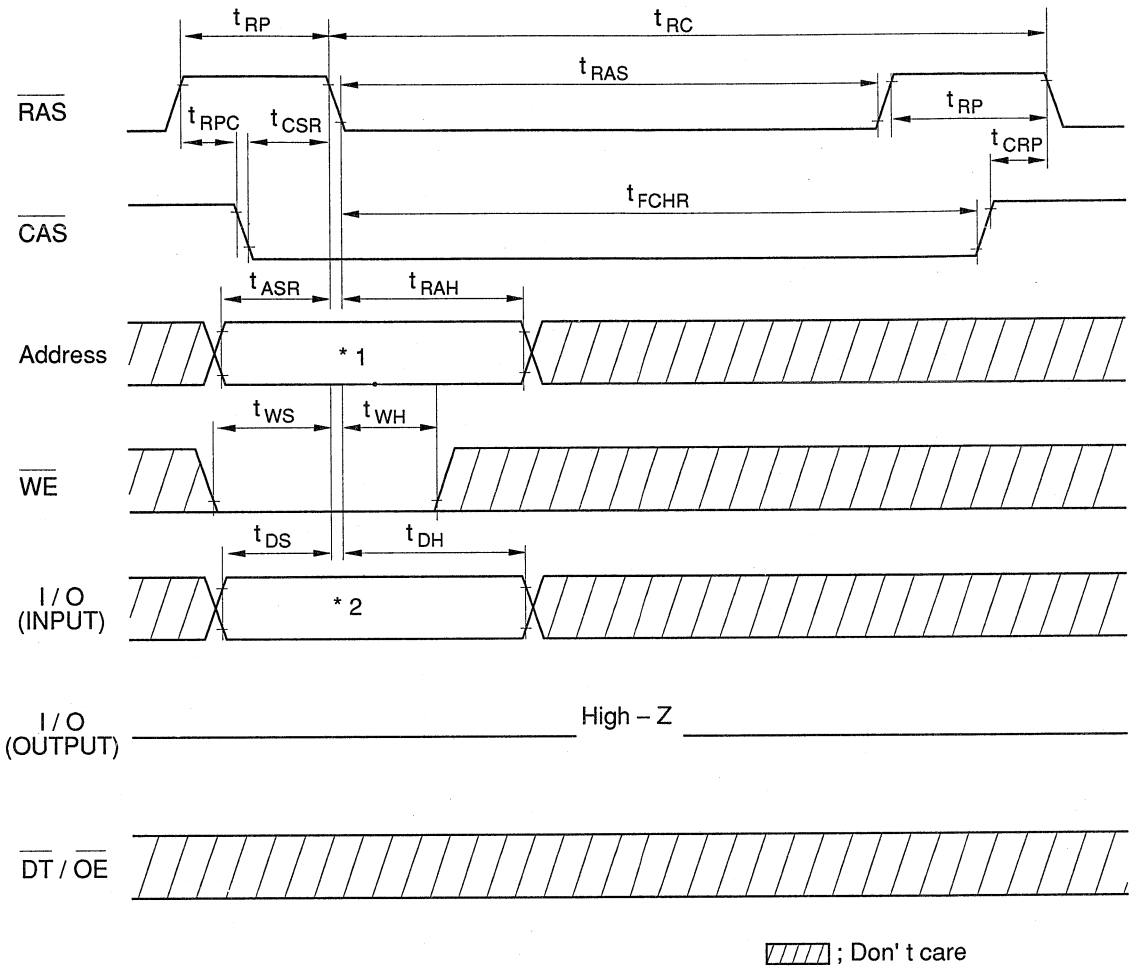
Note: 1. Address 0 is accessed next to address 255.

Serial Write Cycle



Notes : 1. When $\overline{SE}$ is high level in a serial write cycle, data is not written into SAM, however, the pointer is incremented.
2. Address 0 is accessed next to address 255.

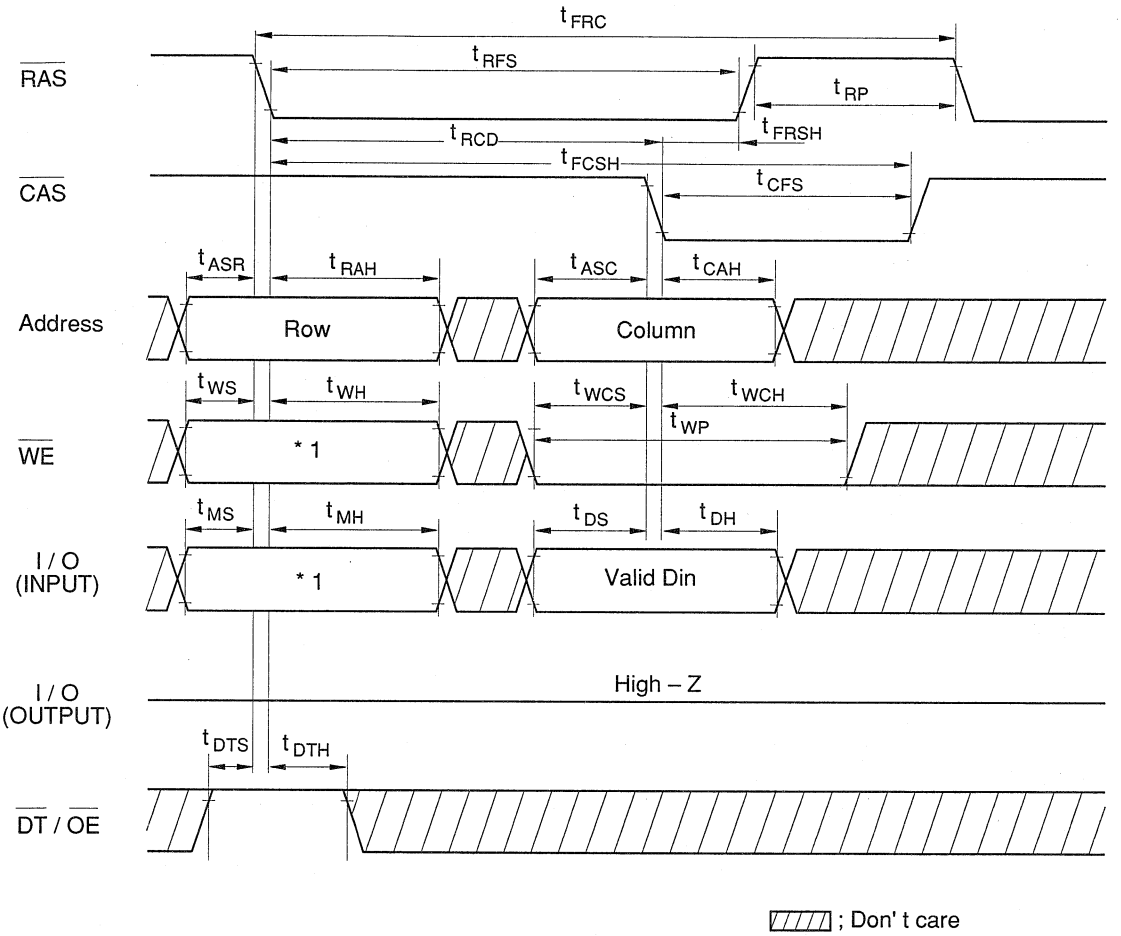
Logic Operation Set/Reset Cycle (HM538122 Series)



Notes: 1. Logic code A0 – A3
2. Write mask data

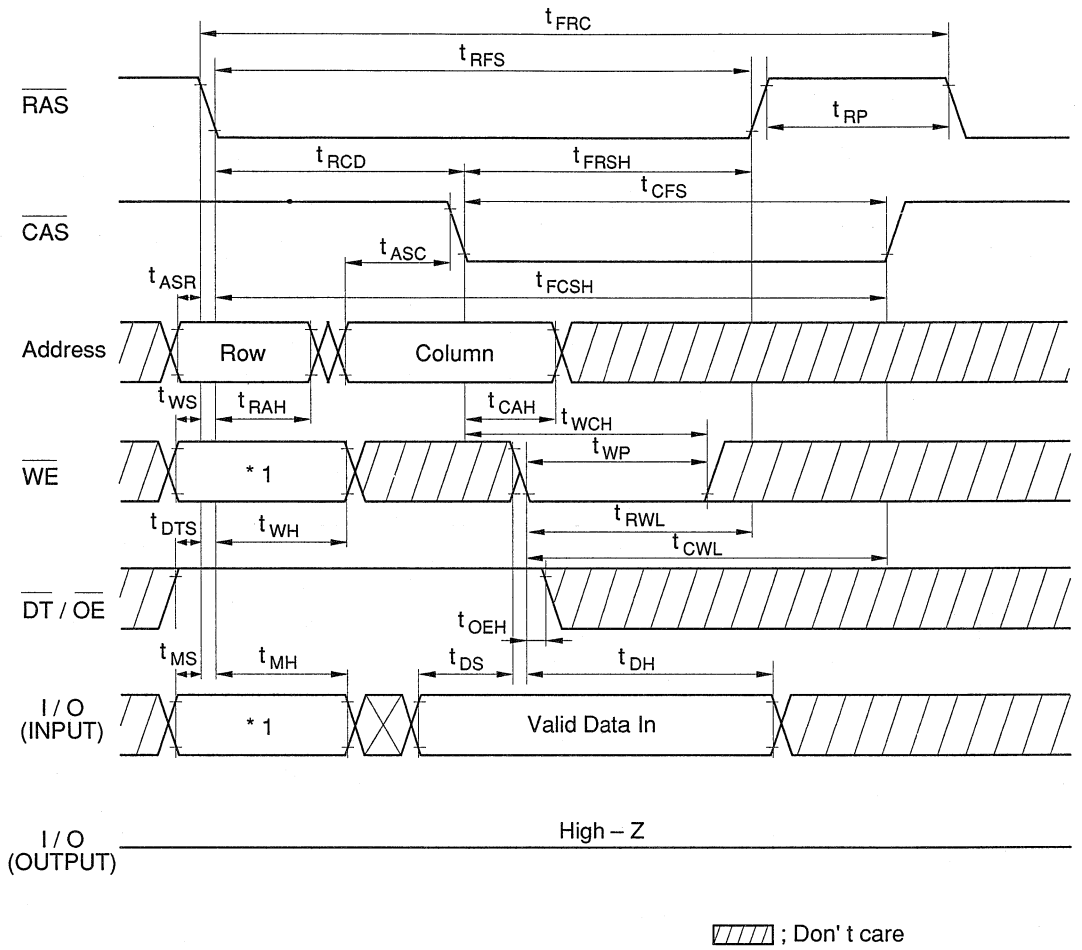
Logic Operation Mode Timing Waveforms

Early Write Cycle (HM538122 Series)



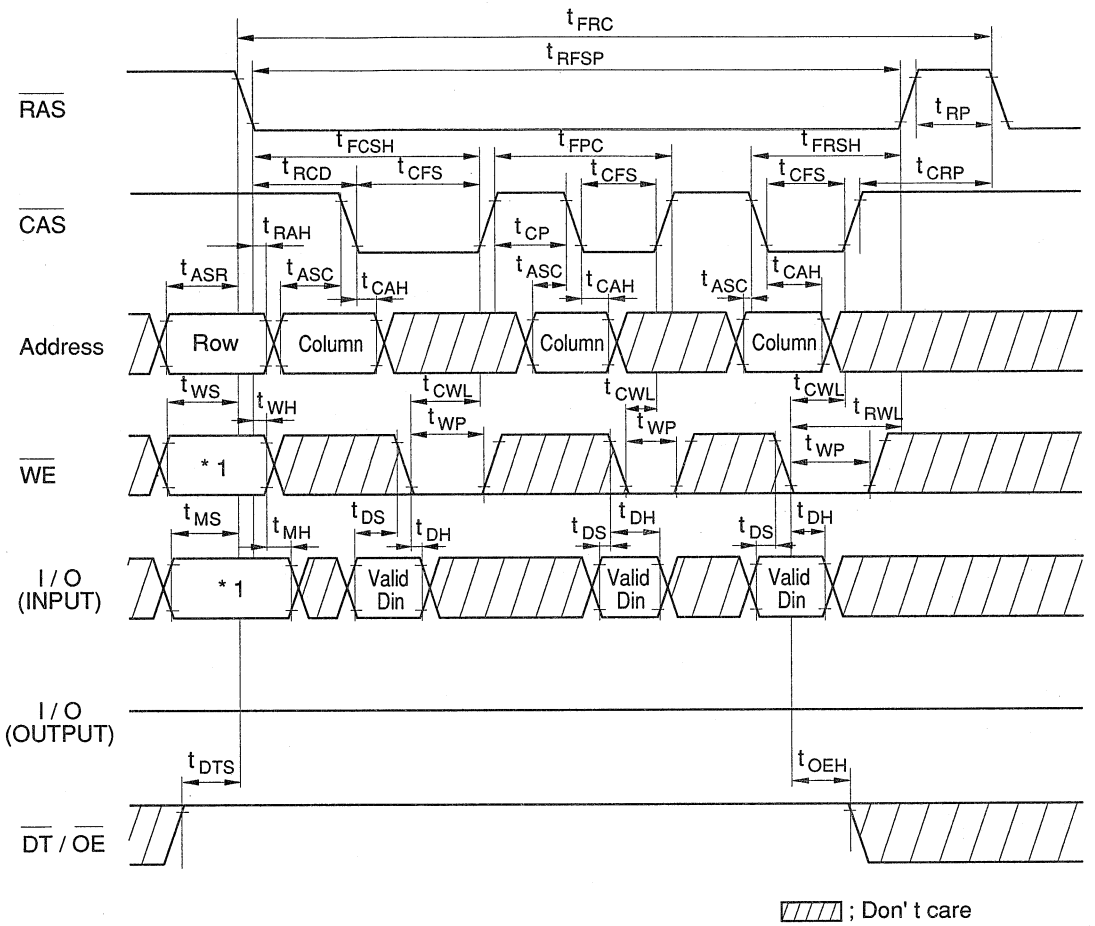
Note: 1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Delayed Write Cycle (HM538122 Series)



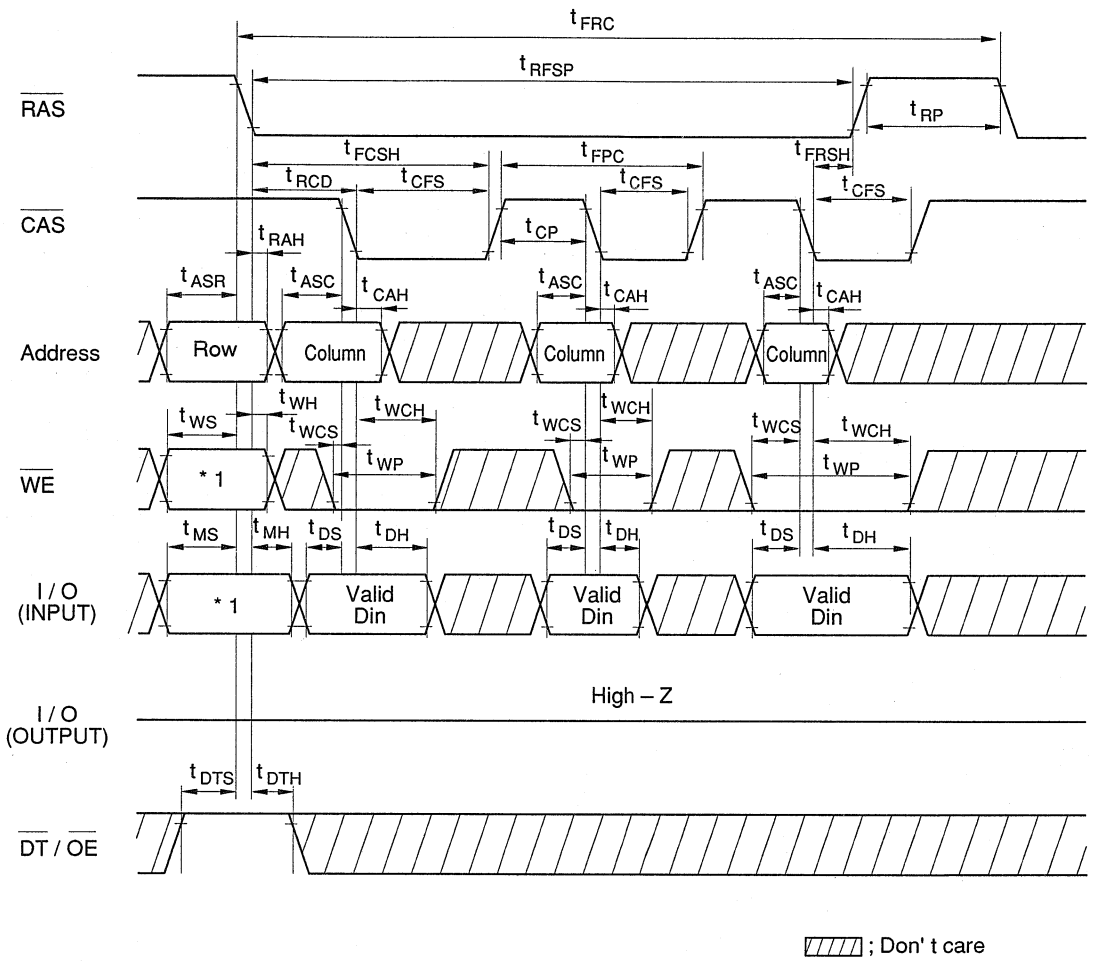
Note: 1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Delayed Write) (HM538122 Series)



Note: 1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Early Write) (HM538122 Series)



Note: 1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

HM534251A Series

262144-word × 4-bit Multiport CMOS Video RAM

The HM534251A is a 1-Mbit multiport video RAM equipped with a 256-kword × 4-bit dynamic RAM and a 512-word × 4-bit SAM (serial access memory). Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has write mask function.

Features

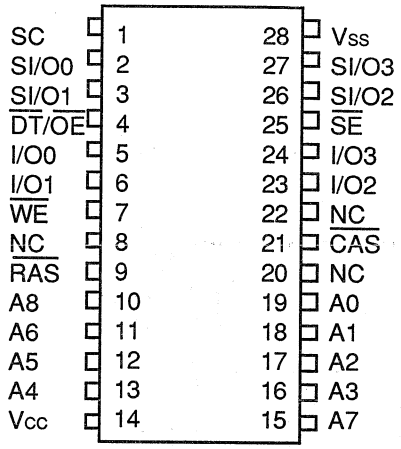
- Multiport organization
  - Asynchronous and simultaneous operation of RAM and SAM capability
    - RAM: 256 kword × 4 bit
    - SAM: 512 word × 4 bit
- Access time
  - RAM: 60 ns/70 ns/80 ns/100 ns max
  - SAM: 20 ns/22 ns/25 ns/25 ns max
- Cycle time
  - RAM: 125 ns/135 ns/150 ns/180 ns min
  - SAM: 25 ns/25 ns/30 ns/30 ns min
- Low power
  - Active RAM: 413 mW max
  - SAM: 275 mW max
  - Standby 38.5 mW max
- High-speed page mode capability
- Mask write mode capability
- Bidirectional data transfer cycle between RAM and SAM capability
- Real time read transfer cycle capability
- 3 variations of refresh (8 ms/512 cycles)
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package
HM534251AJ-6	60 ns	400-mil 28-pin plastic SOJ (CP-28D)
HM534251AJ-7	70 ns	
HM534251AJ-8	80 ns	
HM534251AJ-10	100 ns	
HM534251AZ-6	60 ns	400-mil 28-pin plastic ZIP (ZP-28)
HM534251AZ-7	70 ns	
HM534251AZ-8	80 ns	
HM534251AZ-10	100 ns	
HM534251AT-6	60 ns	8 mm × 14 mm 32-pin TSOP type I (TFP-32DA)
HM534251AT-7	70 ns	
HM534251AT-8	80 ns	
HM534251AT-10	100 ns	
HM534251AR-6	60 ns	8 mm × 14 mm 32-pin TSOP type I reverse (TFP-32DAR)
HM534251AR-7	70 ns	
HM534251AR-8	80 ns	
HM534251AR-10	100 ns	

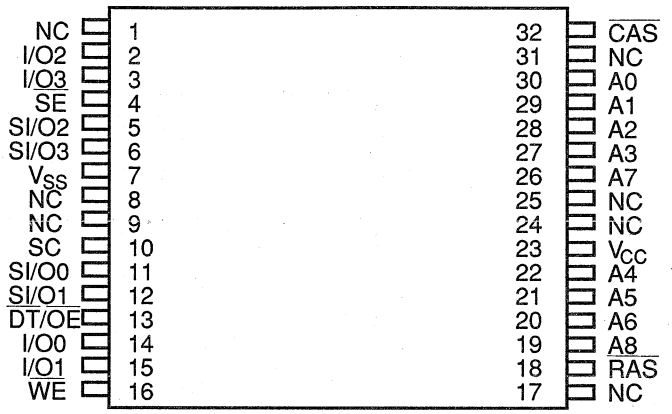
Pin Arrangement

HM534251AJ Series



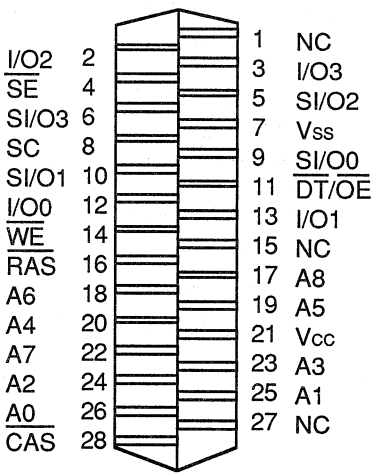
(Top View)

HM534251AT Series



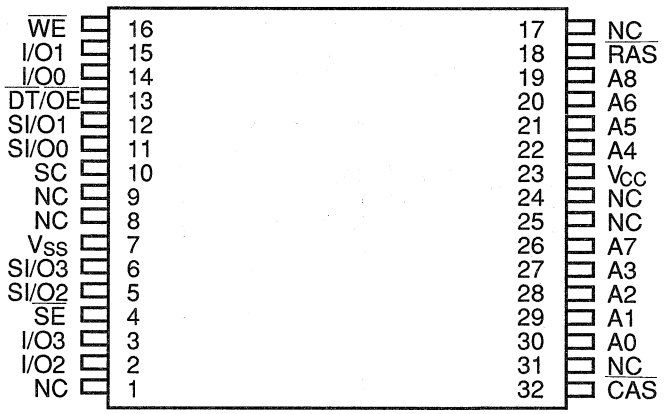
(Top View)

HM534251AZ Series



(Bottom View)

HM534251AR Series



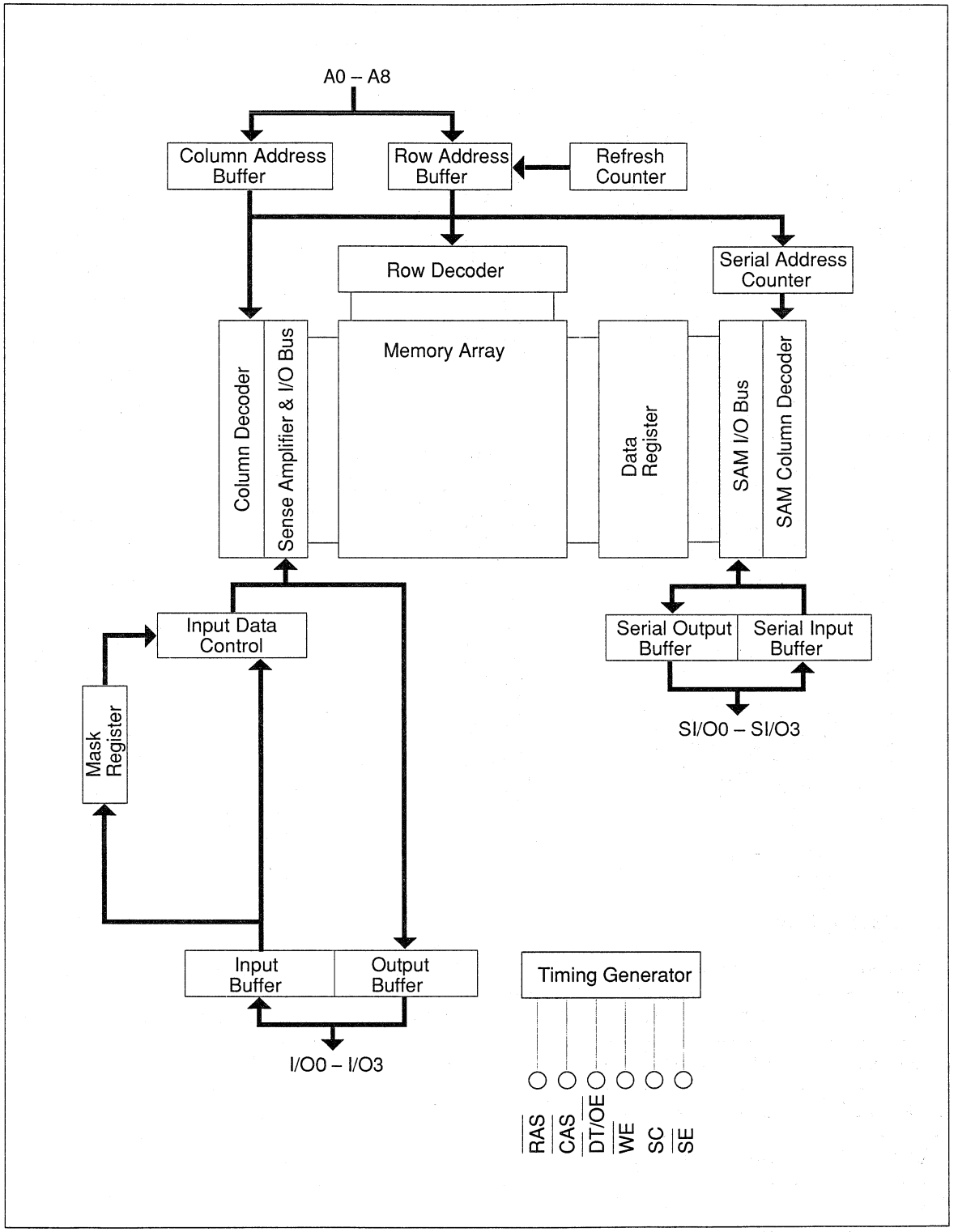
(Top View)

Pin Description

Pin name	Function
A0 – A8	Address inputs
I/O0 – I/O3	RAM port data inputs/outputs
SI/O0 – SI/O3	SAM port data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable

Pin name	Function
$\overline{DT/OE}$	Data transfer/Output enable
SC	Serial clock
$\overline{SE}$	SAM port enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



Pin Functions

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of these signals determine the operation cycle of the HM534251A.

Table 1. Operation Cycles of the HM534251A

Input level at the falling edge of $\overline{RAS}$				
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WE}$	$\overline{SE}$	Operation mode
L	X	X	X	CBR refresh
H	L	L	L	Write transfer
H	L	L	H	Pseudo transfer
H	L	H	X	Read transfer
H	H	L	X	Read/mask write
H	H	H	X	Read/write

Note: X : Don't care.

$\overline{CAS}$ (input pin): Column address is fetched into chip at the falling edge of $\overline{CAS}$. $\overline{CAS}$ controls output impedance of I/O in RAM.

A0–A8 (input pins): Row address is determined by A0–A8 level at the falling edge of $\overline{RAS}$. Column address is determined by A0-A8 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM534251A turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O0 – I/O3 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only to high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT/OE}$ (input pin): $\overline{DT/OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data outputs from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is fetched into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not fetched into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O0-SI/O3 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

Operation of HM534251A

RAM Read Cycle ($\overline{DT/OE}$ high and $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT/OE}$ is low while $\overline{CAS}$ is low, the selected address data outputs through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT/OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle (Early Write, Delayed Write, Read-Modify-Write)
($\overline{DT}/\overline{OE}$ high and $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

- Normal Mode Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after driving $\overline{RAS}$ low, a write cycle is executed and I/O data is written in the selected addresses. When all 4 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.
If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes in high impedance. Data is entered at the $\overline{CAS}$ falling edge.
If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delalyed write cycle. Data is input at the $\overline{WE}$ falling. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.
If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables read/write at the same address in one cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and driving $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is retained. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode cycle, the mask data is retained during the page access.

High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high and $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle. Note that address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 512-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 µs).

Transfer Operation

The HM534251A provides the read transfer cycle, pseudo transfer cycle and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{CAS}$ high and $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)
Read transfer cycle: RAM to SAM
Write transfer cycle: SAM to RAM
(2) Determine SI/O state
Read transfer cycle: SI/O output
Pseudo transfer cycle
and write transfer cycle: SI/O input
(3) Determine first SAM address to access after transferring at column address (SAM start address).
SAM start address must be determined by read transfer cycle or pseudo transfer cycle after power on, and determined for each transfer cycle.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by driving $\overline{DT}/\overline{OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address data (512 x 4-bit) determined by this cycle is transferred to SAM data register synchronously at the rising edge of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address determined by column address. In read transfer cycle, $\overline{DT}/\overline{OE}$ must be risen to transfer data from RAM to SAM.
This cycle can access SAM even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge and t_{SDH} (min) specified between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge must be satisfied. (See figure 1.).

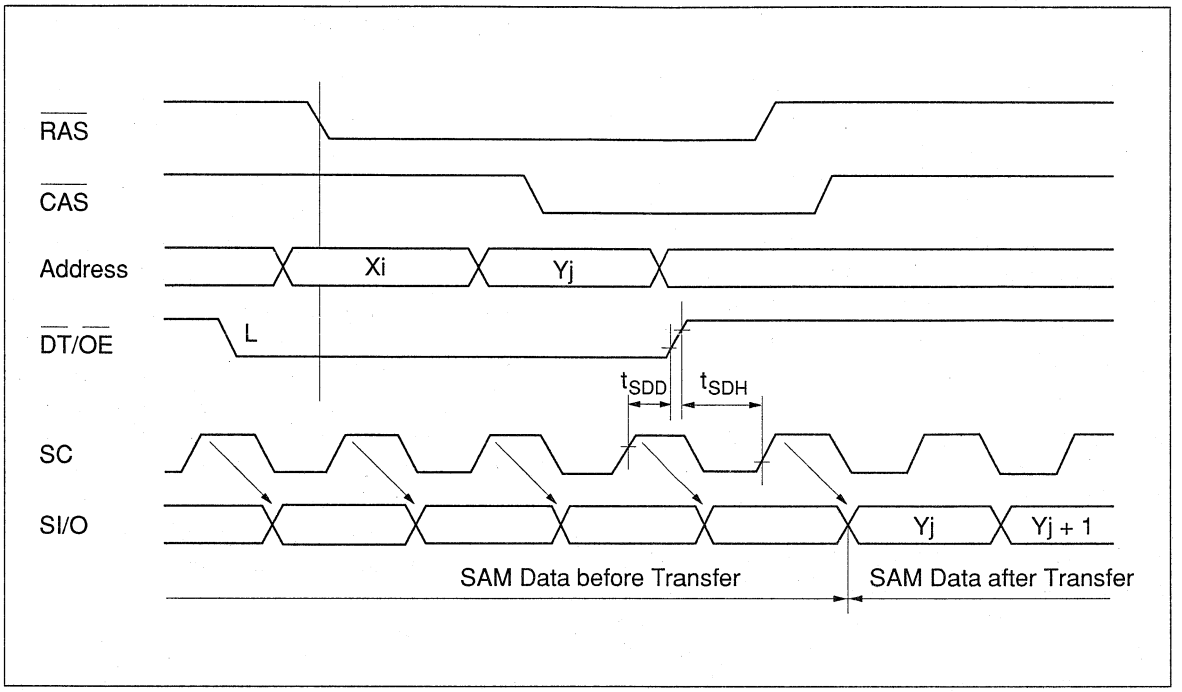


Figure 1. Real Time Read Transfer

When read transfer cycle is executed, SI/O becomes output state by first SAM access. Input must be set high impedance before t_{SZS} (min) of the first SAM access to avoid data contention.

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and $\overline{SE}$ high at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle switches SI/O to input state and set SAM start address without data transfer to RAM.
This cycle starts when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and $\overline{SE}$ high at the falling edge of $\overline{RAS}$. Data should be input to SI/O later than t_{SID} (min) after $\overline{RAS}$ becomes low to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC must not be risen.

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and $\overline{SE}$ low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address for serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC must not be risen.
Data transferred to SAM by read transfer cycle can be written to other address of RAM by write transfer cycle. However, the address to write data must be the same MSB of row address (AX8) as that of the read transfer cycle.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When $\overline{SE}$ is set high, SI/O becomes high impedance, and the internal pointer is incremented by the SC rising. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is fetched into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't fetched into data register. Internal pointer is incremented by the SC rising, so $\overline{SE}$ high can be used as mask data for SAM. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is executed by accessing all 512 row addresses within 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required when all row addresses are accessed within 8 ms.

(1) $\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is executed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high after inputting the row address (= refresh address) from external circuits. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ must be high at the falling edge of $\overline{RAS}$.

(2) CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate.

(3) Hidden Refresh Cycle: Hidden refresh cycle executes CBR refresh with the data output by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register and selector), organized as fully static circuitry, require no refresh.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage*1	V_T	–1.0 to +7.0	V
Power supply voltage*1	V_{CC}	–0.5 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Note: 1. Relative to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage*1	V_{CC}	4.5	5.0	5.5	V
Input high voltage*1	V_{IH}	2.4	—	6.5	V
Input low voltage*1	V_{IL}	–0.5*2	—	0.8	V

Notes: 1. All voltages referenced to V_{SS}.
2. –3.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM534251A										
		-6		-7		-8		-10			Test conditions	
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	RAM port	SAM port
Operating current	I_{CC1}	—	75	—	70	—	60	—	55	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC7}	—	125	—	120	—	100	—	95	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Standby current	I_{CC2}	—	7	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC8}	—	50	—	50	—	40	—	40	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
$\overline{RAS}$-only refresh current	I_{CC3}	—	75	—	70	—	60	—	55	mA	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH} t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC9}	—	125	—	120	—	100	—	95	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Page mode current	I_{CC4}	—	80	—	80	—	70	—	65	mA	$\overline{CAS}$ cycling $\overline{RAS}$ = V_{IL} t_{PC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10}	—	130	—	130	—	110	—	105	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	—	50	—	45	—	40	—	35	mA	$\overline{RAS}$ cycling t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC11}	—	100	—	95	—	80	—	75	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Data transfer current	I_{CC6}	—	80	—	75	—	65	—	60	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC12}	—	130	—	125	—	105	—	100	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (cont)

		HM534251A									
		-6		-7		-8		-10			Test conditions
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	RAM port / SAM port
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	–10	10	µA	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	–10	10	µA	
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V	I_{OH} = –2 mA
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V	I_{OL} = 4.2 mA

Note: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once while $\overline{RAS}$ is low and $\overline{CAS}$ is high.

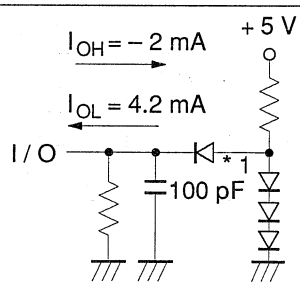
Capacitance (Ta = 25°C, V_{CC} = 5 V, f = 1 MHz, Bias: Clock, I/O = V_{CC}, address = V_{SS})

Item	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clock	C_{I2}	—	—	5	pF
I/O, SI/O	$C_{I/O}$	—	—	7	pF

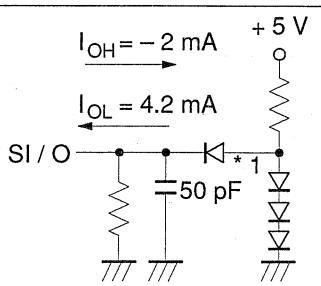
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V) *1, *16

Test Conditions

- Input rise and fall time: 5 ns
- Output load: See figures
- Input pulse levels : V_{SS} to 3.0 V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V



Output Load (A)



Output Load (B)

Note: 1. Including scope & jig.

Common Parameter

		HM534251A									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	125	—	135	—	150	—	180	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	55	—	55	—	60	—	70	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	—	20	—	20	—	25	—	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	20	60	20	75	ns	2
$\overline{RAS}$ hold time referenced to $\overline{CAS}$	t_{RSH}	20	—	20	—	20	—	25	—	ns	
$\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Transition time (rise to fall)	t_T	3	50	3	50	3	50	3	50	ns	3
Refresh period	t_{REF}	—	8	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ setup time	t_{DTS}	0	—	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ hold time	t_{DTH}	10	—	10	—	10	—	10	—	ns	
Data-in to $\overline{CAS}$ delay time	t_{DZC}	0	—	0	—	0	—	0	—	ns	4
Data-in to $\overline{OE}$ delay time	t_{DZO}	0	—	0	—	0	—	0	—	ns	4
Output buffer turn-off delay referenced to $\overline{CAS}$	t_{OFF1}	—	20	—	20	—	20	—	20	ns	5
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	—	20	—	20	—	20	—	20	ns	5

Read Cycle (RAM), Page Mode Read Cycle

Item	Symbol	HM534251A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	35	—	40	—	45	ns	7, 9
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	0	—	ns	10
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	10
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	2
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	35	—	40	—	45	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	35	—	35	—	40	—	45	—	ns	
Page mode cycle time	t_{PC}	45	—	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	10	—	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	—	40	—	45	—	50	ns	
Page mode $\overline{RAS}$ pulse width	t_{RASP}	60	100000	70	100000	80	100000	100	100000	ns	

Write Cycle (RAM), Page Mode Write Cycle

		HM534251A									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	0	—	ns	11
Write command hold time	t_{WCH}	15	—	15	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	15	—	15	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	15	—	15	—	15	—	15	—	ns	12
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	10	—	10	—	10	—	10	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	10	—	10	—	10	—	10	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	20	—	20	—	20	—	20	—	ns	
Page mode cycle time	t_{PC}	45	—	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ to data-in delay time	t_{CDD}	20	—	20	—	20	—	20	—	ns	13
Page mode $\overline{RAS}$ pulse width	t_{RASP}	60	100000	70	100000	80	100000	100	100000	ns	

Read-Modify-Write Cycle

Item	Symbol	HM534251A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	175	—	185	—	200	—	230	—	ns	
$\overline{RAS}$ pulse width (read-modify-write cycle)	t_{RWS}	110	10000	120	10000	130	10000	150	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	45	—	45	—	45	—	50	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	60	—	60	—	65	—	70	—	ns	14
$\overline{OE}$ to data-in delay time	t_{ODD}	20	—	20	—	20	—	20	—	ns	12
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	6, 7
Access time form $\overline{CAS}$	t_{CAC}	—	20	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	35	—	40	—	45	ns	7, 9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	20	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	15	—	15	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	15	—	15	—	15	—	15	—	ns	12
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	20	—	20	—	20	—	20	—	ns	

Refresh Cycle

Item	Symbol	HM534251A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Notes
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

Read Transfer Cycle

Item	Symbol	HM534251A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Notes
$\overline{DT}$ hold time referenced to $\overline{RAS}$	t_{RDH}	50	10000	60	10000	65	10000	80	10000	ns	
$\overline{DT}$ hold time referenced to $\overline{CAS}$	t_{CDH}	20	—	20	—	20	—	25	—	ns	
$\overline{DT}$ hold time referenced to column address	t_{ADH}	25	—	25	—	30	—	30	—	ns	
$\overline{DT}$ precharge time	t_{DTP}	20	—	20	—	20	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ delay time	t_{DRD}	65	—	65	—	70	—	80	—	ns	
SC to $\overline{RAS}$ setup time	t_{SRS}	25	—	25	—	30	—	30	—	ns	
1st SC to $\overline{RAS}$ hold time	t_{SRH}	60	—	70	—	80	—	100	—	ns	
1st SC to $\overline{CAS}$ hold time	t_{SCH}	25	—	25	—	25	—	25	—	ns	
1st SC to column address hold time	t_{SAH}	40	—	40	—	45	—	50	—	ns	
Last SC to $\overline{DT}$ delay time	t_{SDD}	5	—	5	—	5	—	5	—	ns	
1st SC to $\overline{DT}$ hold time	t_{SDH}	10	—	10	—	15	—	15	—	ns	
Serial data-in to 1st SC delay time	t_{SZS}	0	—	0	—	0	—	0	—	ns	
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	10	—	ns	

Read Transfer Cycle (cont)

Item	Symbol	HM534251A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Notes
SC access time	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	35	—	40	—	45	—	ns	
$\overline{DT}$ high hold time from $\overline{RAS}$ precharge	t_{DTHH}	10	—	10	—	10	—	10	—	ns	

Pseudo Transfer Cycle, Write Transfer Cycle

Item	Symbol	HM534251A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Notes
$\overline{SE}$ setup time referenced to $\overline{RAS}$	t_{ES}	0	—	0	—	0	—	0	—	ns	
$\overline{SE}$ hold time referenced to $\overline{RAS}$	t_{EH}	10	—	10	—	10	—	10	—	ns	
SC setup time referenced to $\overline{RAS}$	t_{SRS}	25	—	25	—	30	—	30	—	ns	
$\overline{RAS}$ to SC delay time	t_{SRD}	20	—	20	—	25	—	25	—	ns	
Serial output buffer turn-off time referenced to $\overline{RAS}$	t_{SRZ}	10	40	10	40	10	45	10	50	ns	
$\overline{RAS}$ to serial data-in delay time	t_{SID}	40	—	40	—	45	—	50	—	ns	
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	22	—	25	—	25	ns	15

Pseudo Transfer Cycle, Write Transfer Cycle (cont)

		HM534251A									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{SE}$ access time	t_{SEA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial write enable setup time	t_{SWS}	5	—	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	

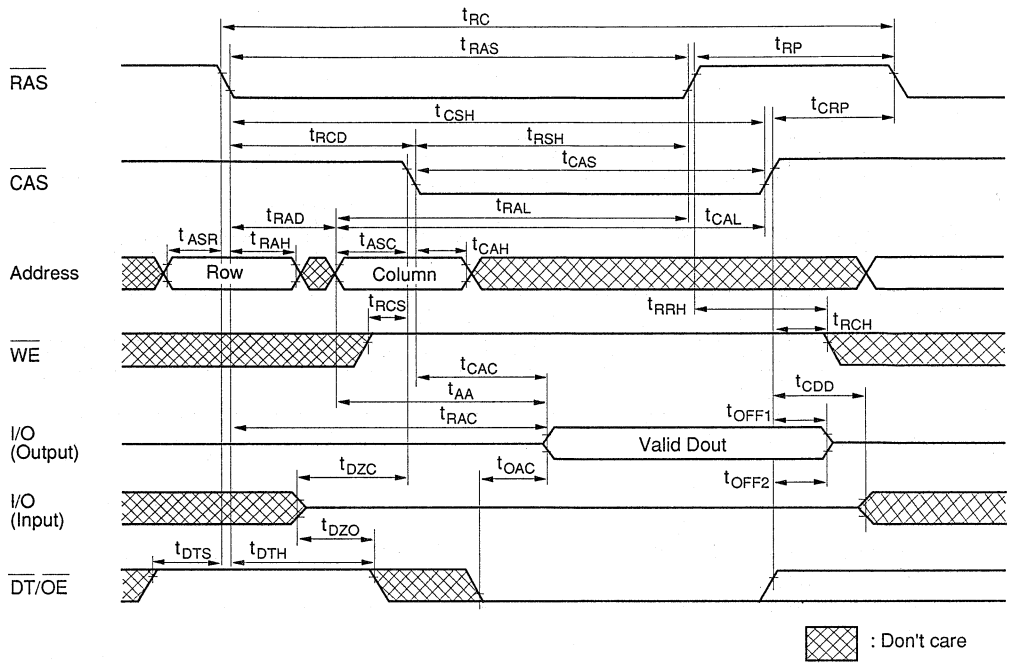
Serial Read Cycle, Serial Write Cycle

		HM534251A									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Access time from SC	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
Access time from $\overline{SE}$	t_{SEA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial output buffer turn-off time referenced to $\overline{SE}$	t_{SEZ}	—	20	—	20	—	20	—	20	ns	5
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	
Serial write enable setup time	t_{SWS}	5	—	5	—	5	—	5	—	ns	
Serial write enable hold time	t_{SWH}	15	—	15	—	15	—	15	—	ns	
Serial write disable setup time	t_{SWIS}	5	—	5	—	5	—	5	—	ns	
Serial write disable hold time	t_{SWIH}	15	—	15	—	15	—	15	—	ns	

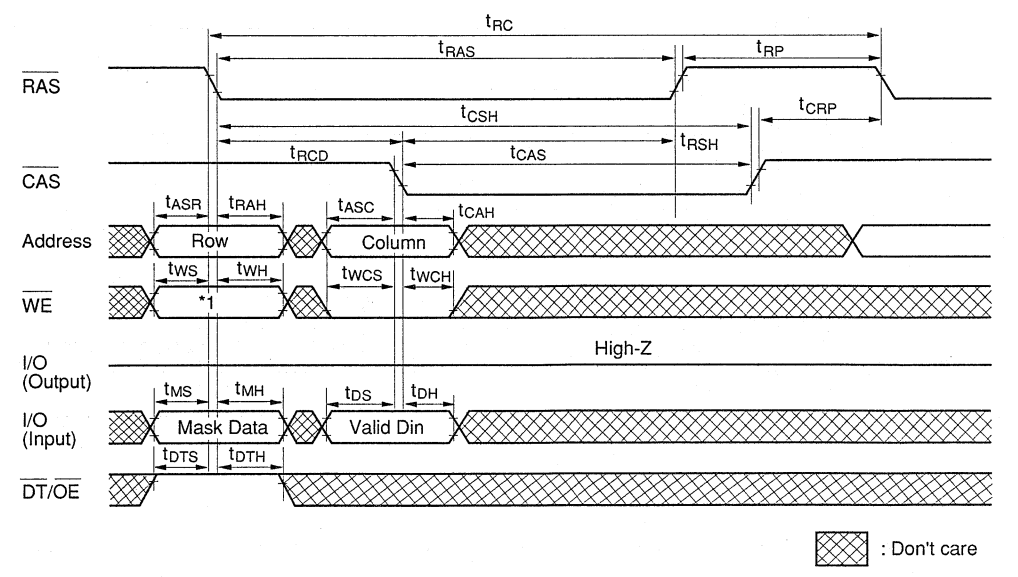
Notes:
1. AC measurements assume t_T = 5 ns.
2. When $t_{RCD} > t_{RCD}$ (max) or $t_{RAD} > t_{RAD}$ (max), access time is specified by t_{CAC} or t_{AA}.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition time t_T is measured between V_{IH} and V_{IL}.
4. Data input must be floating before output buffer is turned on. In read cycle, read-modify-write cycle and delayed write cycle, either t_{DZC} (min) or t_{DZO} (min) must be satisfied.
5. t_{OFF1} (max), t_{OFF2} (max) and t_{SEZ} (max) are defined as the time at which the output acheives the open circuit condition (V_{OH} –100 mV, V_{OL} +100 mV).
6. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
8. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
9. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
10. If either t_{RCH} of t_{RRH} is satisfied, operation is guaranteed.
11. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
12. These parameters are specified by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
13. Either t_{CDD} (min) or t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{CAS}$ or $\overline{OE}$ prior to applying data to the device when output buffer is on.
14. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min) in read-modify-write cycle, the data of the selected address outputs to an I/O pin and input data is written into the selected address. t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{OE}$ prior to applying data to the device.
15. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
16. After power-up, pause for 100 µs or more and execute at least 8 initialization cycle (normal memory cycle or refresh cycle), then start operation.

Timing Waveforms

Read Cycle

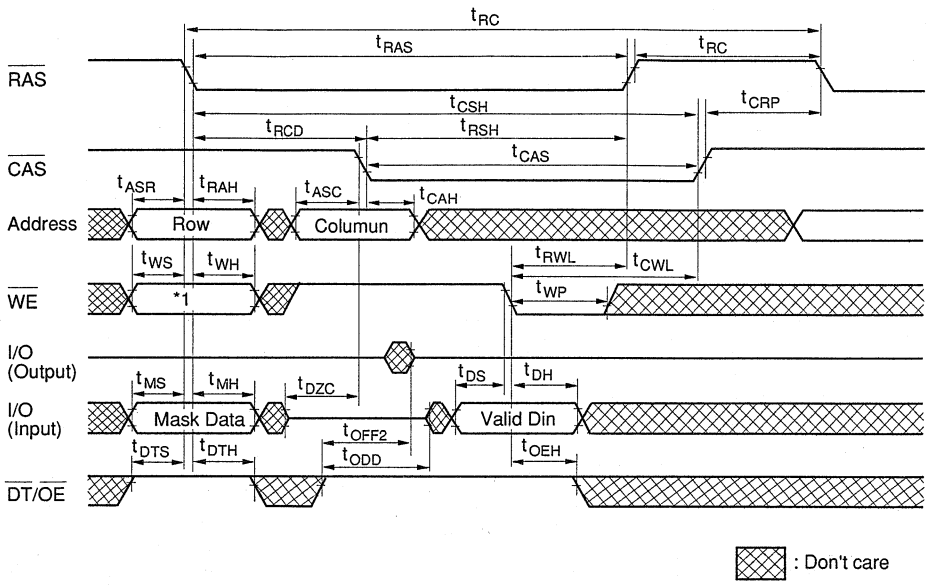


Early Write Cycle



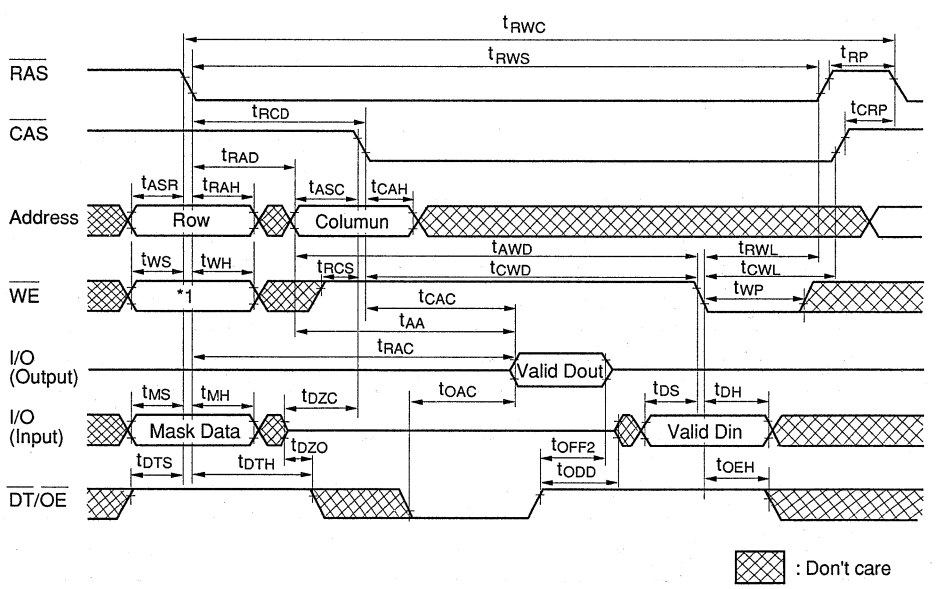
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Delayed Write Cycle



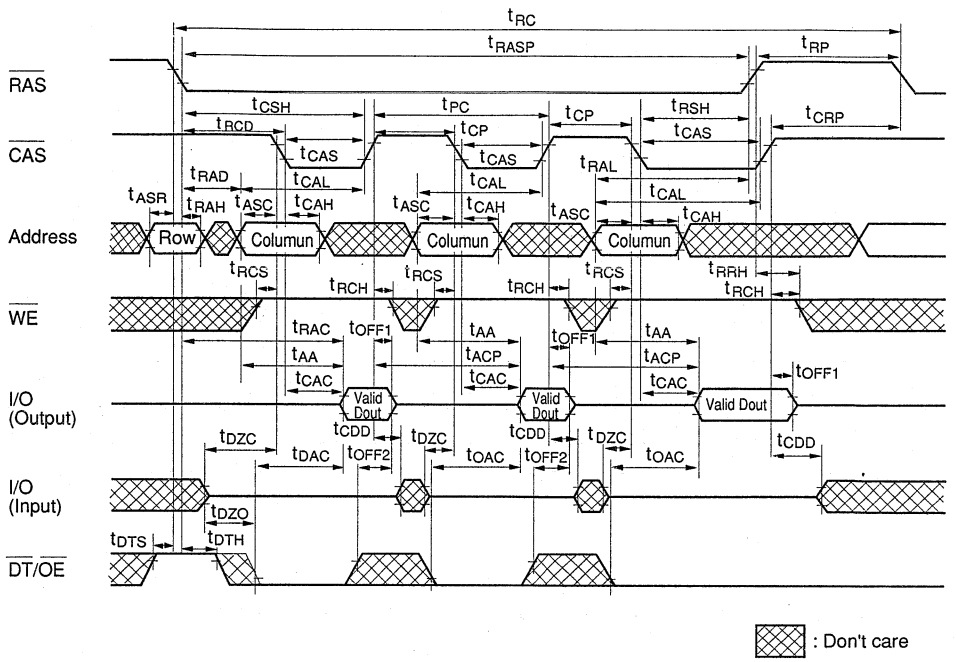
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Read-Modify-Write Cycle

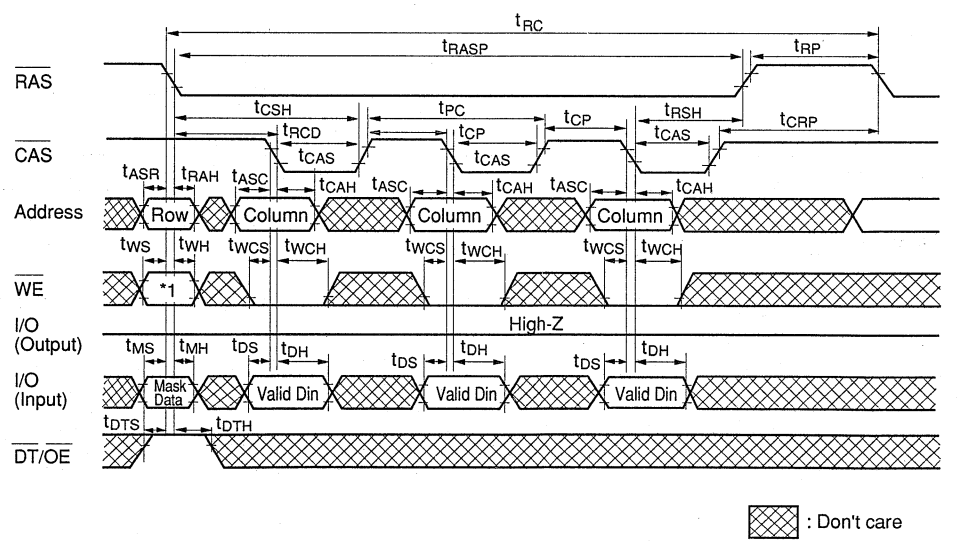


Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Page Mode Read Cycle

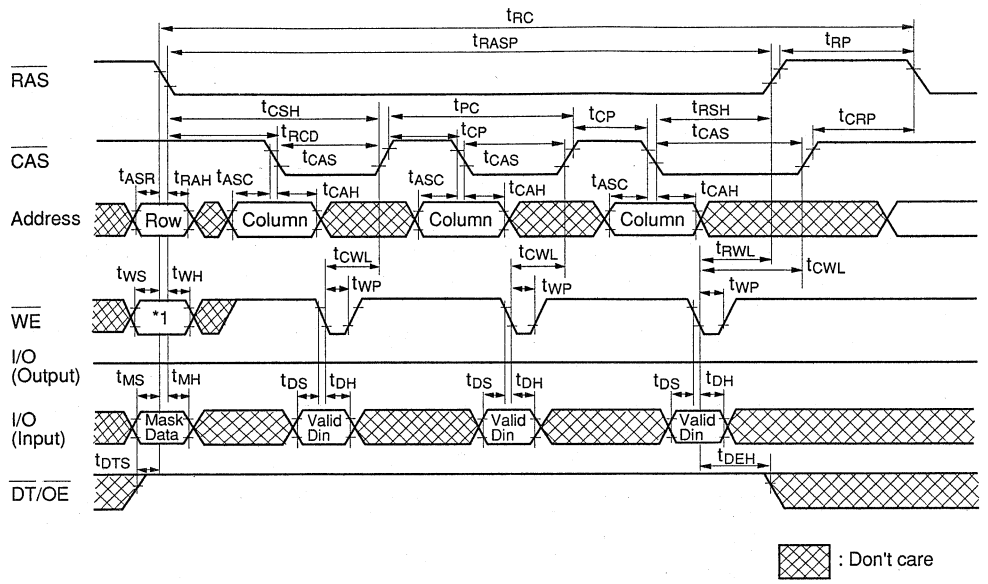


Page Mode Write Cycle (Early Write)



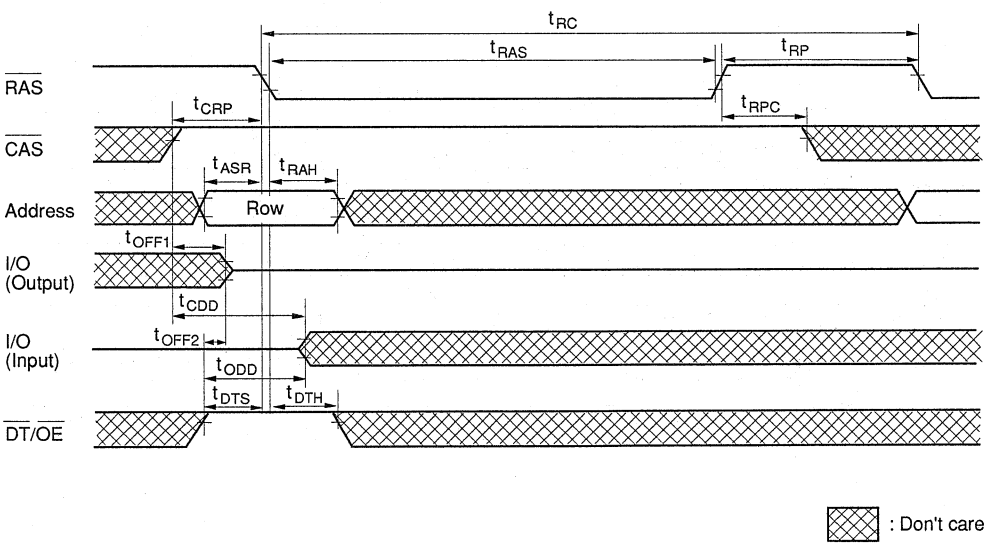
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Page Mode Write Cycle (Delayed Write)

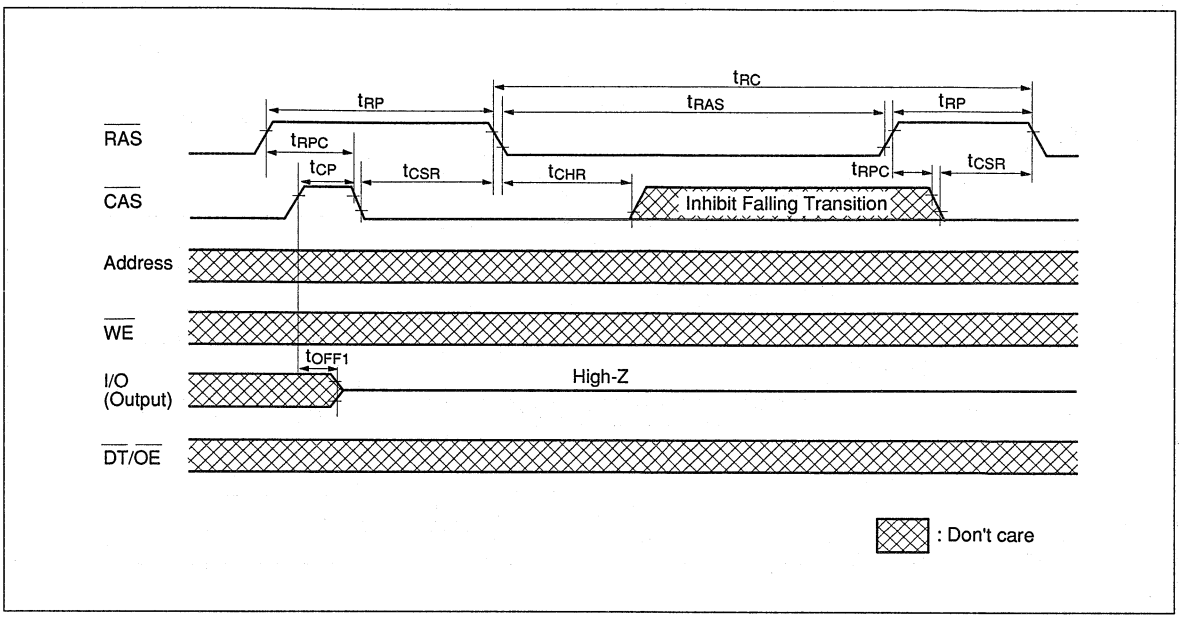


Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

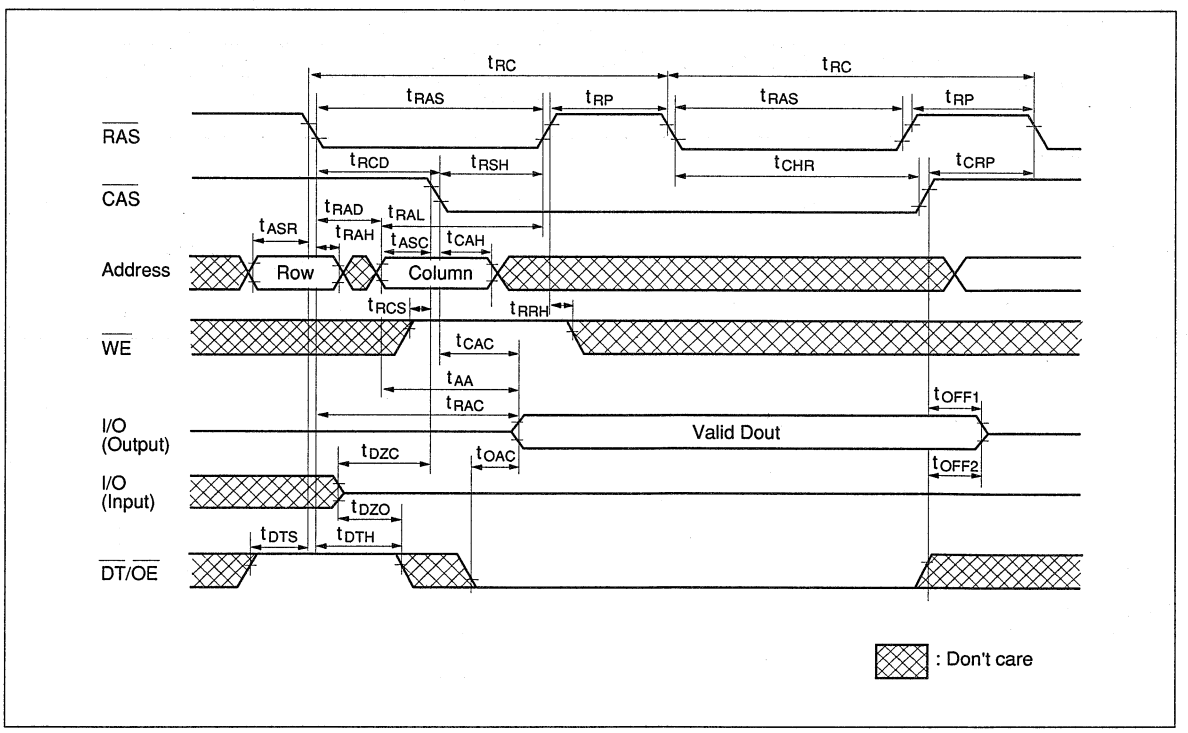
$\overline{RAS}$-Only Refresh Cycle



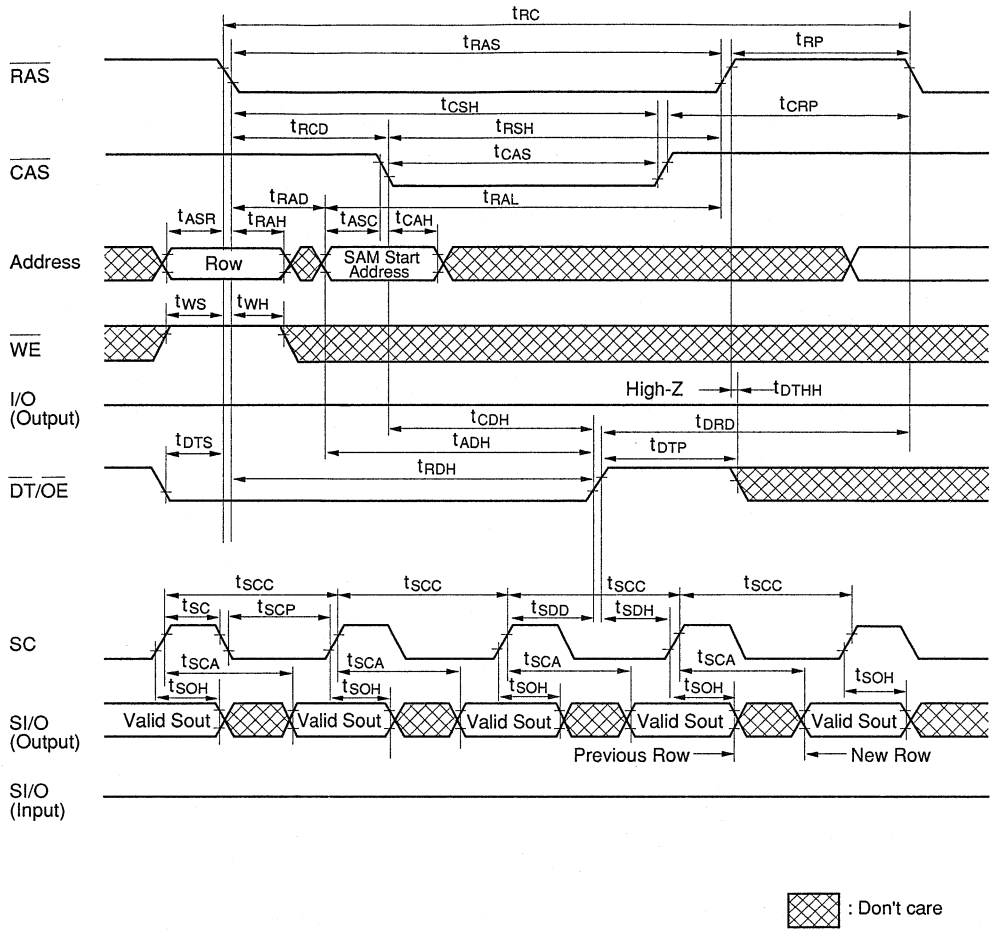
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



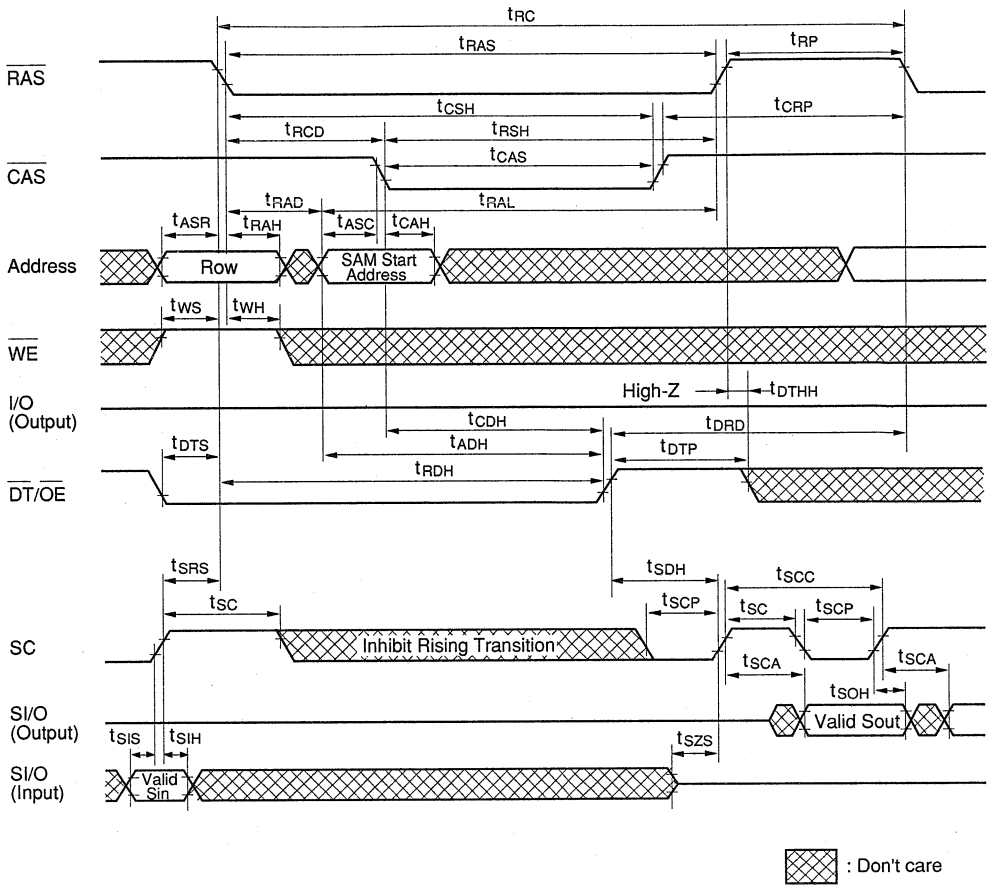
Hidden Refresh Cycle



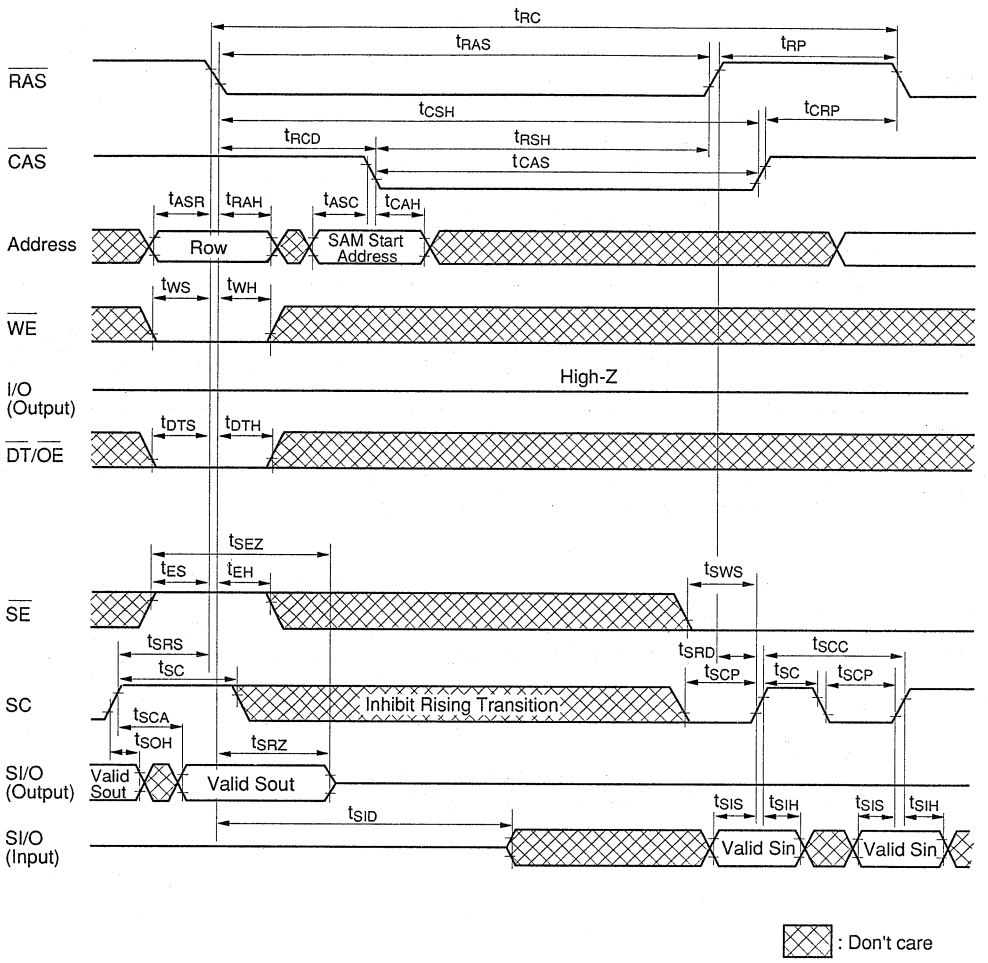
Read Transfer Cycle (1)



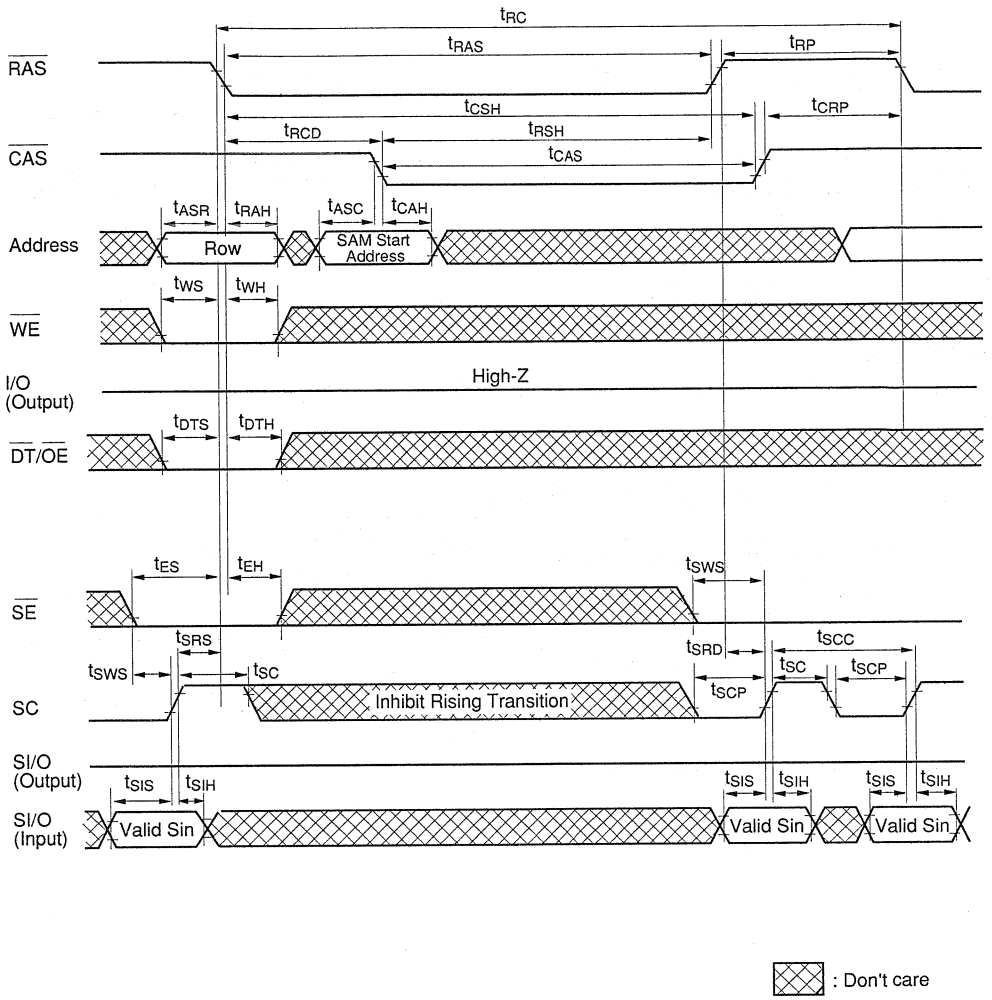
Read Transfer Cycle (2)



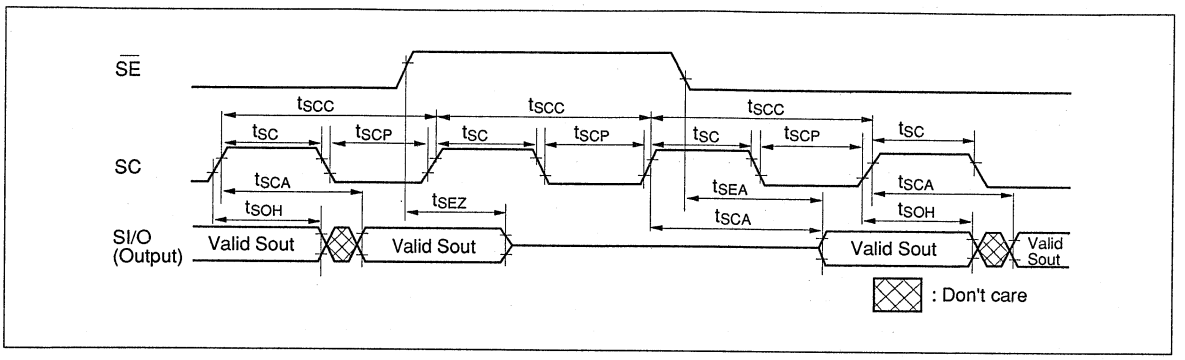
Pseudo Transfer Cycle



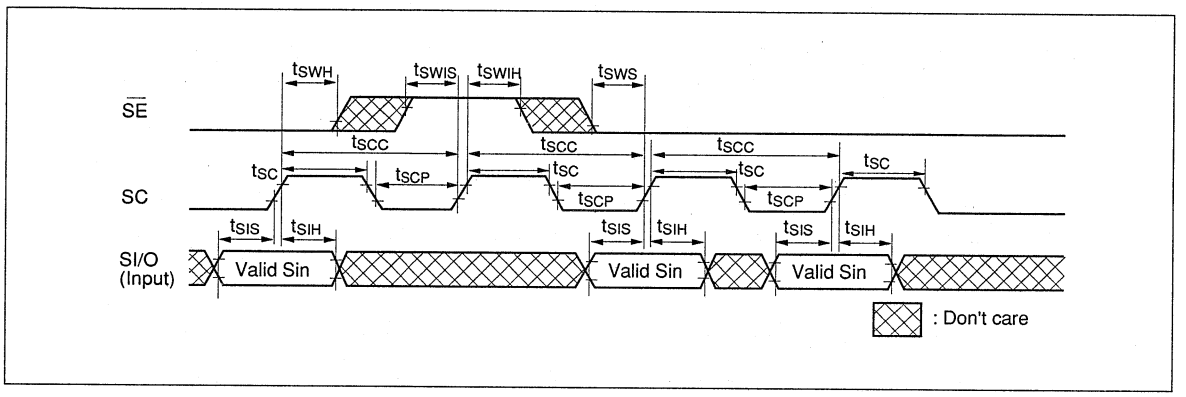
Write Transfer Cycle



Serial Read Cycle



Serial Write Cycle



HM534253A Series

262144-word × 4-bit Multiport CMOS Video RAM

The HM534253A is a 1-Mbit multiport video RAM equipped with a 256-kword × 4-bit dynamic RAM and a 512-word × 4-bit SAM (serial access memory). Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM. In addition, it has two modes to realize fast writing in RAM. Block write and flash write modes clear the data of 4-word × 4-bit and the data of one row (512-word × 4-bit) respectively in one cycle of RAM. And the HM534253A makes split transfer cycle possible by dividing SAM into two split buffers equipped with 256-word × 4-bit each. This cycle can transfer data to SAM which is not active, and enables a continuous serial access.

Features

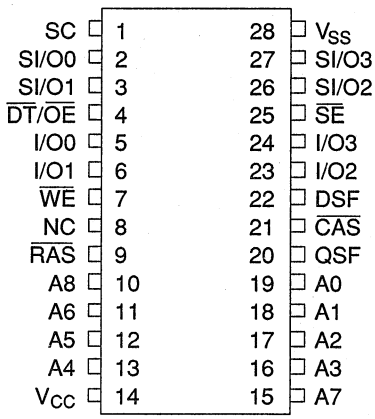
- Multiport organization
  Asynchronous and simultaneous operation of RAM and SAM capability
  RAM: 256-kword × 4-bit and SAM: 512-word × 4-bit
- Access time RAM: 60 ns/70 ns/80 ns/100 ns max
  SAM: 20 ns/22 ns/25 ns/25 ns max
- Cycle time RAM: 125 ns/135 ns/150 ns/180 ns min
  SAM: 25 ns/25 ns/30 ns/30 ns min
- Low power
  Active RAM: 413 mW max
  SAM: 275 mW max
  Standby 38.5 mW max
- High-speed page mode capability
- Mask write mode capability
- Bidirectional data transfer cycle between RAM and SAM capability
- Split transfer cycle capability
- Block write mode capability
- Flash write mode capability
- 3 variations of refresh (8 ms/512 cycles)
  $\overline{\text{RAS}}$-only refresh
  $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package
HM534253AJ-6	60 ns	400-mil 28-pin plastic SOJ (CP-28D)
HM534253AJ-7	70 ns	
HM534253AJ-8	80 ns	
HM534253AJ-10	100 ns	
HM534253AZ-6	60 ns	400-mil 28-pin plastic ZIP (ZP-28)
HM534253AZ-7	70 ns	
HM534253AZ-8	80 ns	
HM534253AZ-10	100 ns	
HM534253AT-6	60 ns	8 mm × 14 mm 32-pin TSOP type I (TFP-32DA)
HM534253AT-7	70 ns	
HM534253AT-8	80 ns	
HM534253AT-10	100 ns	
HM534253AR-6	60 ns	8 mm × 14 mm 32-pin TSOP type I reverse (TFP-32DAR)
HM534253AR-7	70 ns	
HM534253AR-8	80 ns	
HM534253AR-10	100 ns	

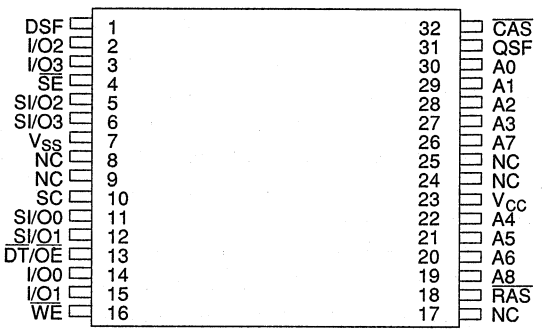
Pin Arrangement

HM534253AJ Series



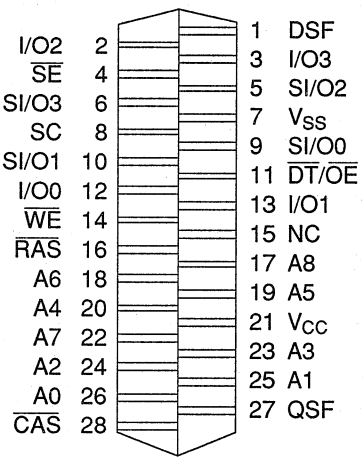
(Top View)

HM534253AT Series



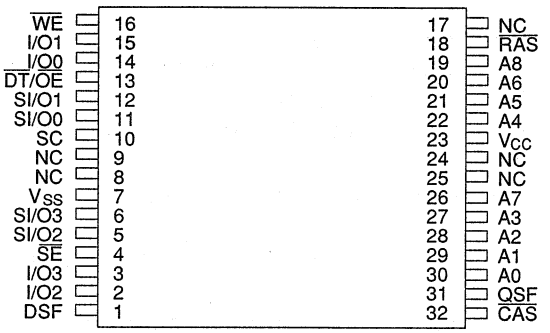
(Top View)

HM534253AZ Series



(Bottom View)

HM534253AR Series



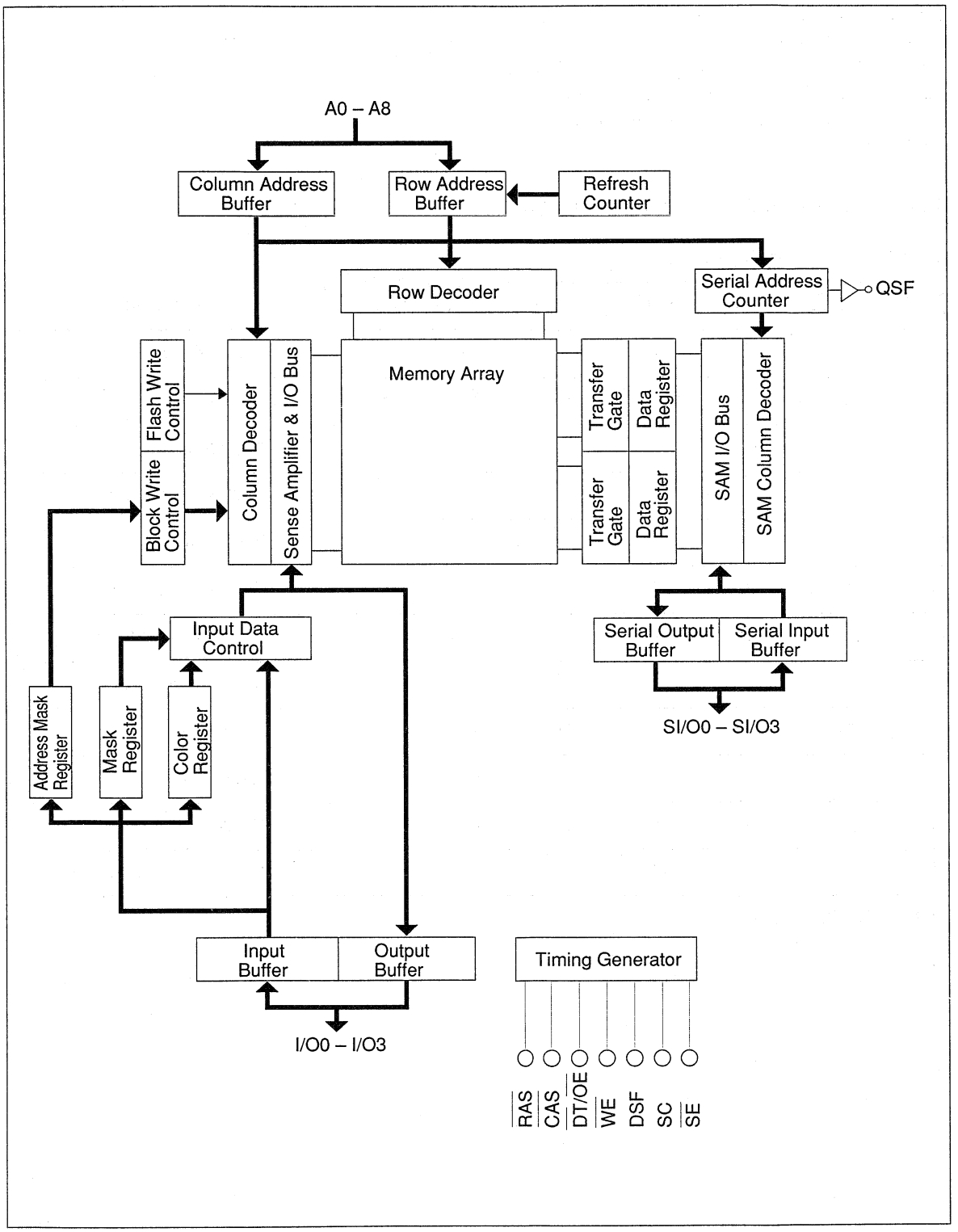
(Top View)

Pin Description

Pin name	Function
A0 – A8	Address inputs
I/O0 – I/O3	RAM port data inputs/outputs
SI/O0 – SI/O3	SAM port data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{DT/OE}$	Data transfer/output enable

Pin name	Function
SC	Serial clock
$\overline{SE}$	SAM port enable
DSF	Special function input flag
QSF	Special function output flag
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



Pin Functions

$\overline{\text{RAS}}$ (input pin): $\overline{\text{RAS}}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{\text{RAS}}$. The input level of these signals determine the operation cycle of the HM534253A.

Table 1 Operation Cycles of the HM534253A

Input level at the falling edge of $\overline{\text{RAS}}$						
$\overline{\text{CAS}}$	$\overline{\text{DT/OE}}$	$\overline{\text{WE}}$	$\overline{\text{SE}}$	DSF	DSF at the falling edge of $\overline{\text{CAS}}$	Operation mode
L	X	X	X	X	—	CBR refresh
H	L	L	L	L	X	Write transfer
H	L	L	H	L	X	Pseudo transfer
H	L	L	X	H	X	Split write transfer
H	L	H	X	L	X	Read transfer
H	L	H	X	H	X	Split read transfer
H	H	L	X	L	L	Read/mask write
H	H	L	X	L	H	Mask block write
H	H	L	X	H	X	Flash write
H	H	H	X	L	L	Read/write
H	H	H	X	L	H	Block write
H	H	H	X	H	X	Color register read/write

Note: X : Don't care.

$\overline{CAS}$ (input pin): Column address and DSF signal are fetched into chip at the falling edge of $\overline{CAS}$, which determines the operation mode of HM534253A. $\overline{CAS}$ controls output impedance of I/O in RAM.

A0–A8 (input pin): Row address is determined by A0–A8 level at the falling edge of $\overline{RAS}$. Column address is determined by A0–A8 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM534253A turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O0–I/O3 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only to high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM. In block write cycle, they function as address mask data at the falling edge of $\overline{CAS}$.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data outputs from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is fetched into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not fetched into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O0-SI/O3 (input/output pins) : SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

DSF (input pin): DSF is a special function data input flag pin. It is set to high at the falling edge of $\overline{RAS}$ when new functions such as color register read/write, split transfer, and flash write, are used. DSF is set to high at the falling edge of $\overline{CAS}$ when block write is executed.

QSF (output pin): QSF outputs data of address A8 in SAM. QSF is switched from low to high by accessing address 255 in SAM and from high to low by accessing 511 address in SAM.

Operation of HM534253A

RAM Read Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF low at the falling edge of $\overline{RAS}$, DSF low at the falling edge of $\overline{CAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data outputs through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle (Early Write, Delayed Write, Read-Modify-Write)
($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF low at the falling edge of $\overline{RAS}$, DSF low at the falling edge of $\overline{CAS}$)

- Normal Mode Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after driving $\overline{RAS}$ low, a write cycle is executed and I/O data is written in the selected addresses. When all 4 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes in high impedance. Data is entered at the $\overline{CAS}$ falling edge.
If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.
If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables read/write at the same address in one cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and driving $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is retained. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode, the mask data is retained during the page access.

High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF low at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle. In this cycle, read, write, and block write cycles can be mixed. Note that address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 512-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 µs).

Color Register Set/Read Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high, $\overline{WE}$ high and DSF high at the falling edge of $\overline{RAS}$)

In color register set cycle, color data is set to the internal color register used in flash write cycle or block write cycle. 4 bits of internal color register are provided at each I/O. This register is composed of static circuits, so once it is set, it retains the data until reset. Color register set cycle is just as same as the usual write cycle except that DSF is set high at the falling edge of $\overline{RAS}$, and read, early write and delayed write cycle can be executed. In this cycle, HM534253A refreshes the row address fetched at the falling edge of $\overline{RAS}$.

Flash Write Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high, $\overline{WE}$ low and DSF high at the falling edge of $\overline{RAS}$)

In a flash write cycle, a row of data (512-word × 4-bit) is cleared to 0 or 1 at each I/O according to the data of color register mentioned before. It is also necessary to mask I/O in this cycle. When $\overline{CAS}$ and $\overline{DT}/\overline{OE}$ is set high, $\overline{WE}$ is low, and DSF is high at the falling edge of $\overline{RAS}$, this cycle starts. Then, the row address to clear is given to row address and mask data is given to I/O. Mask data is as same as that of a RAM write cycle. High I/O is cleared, low I/O is not cleared and the internal data is retained. Cycle time is the same as those of RAM read/write cycles, so all bits can be cleared in 1/512 of the usual cycle time. (See figure 1.)

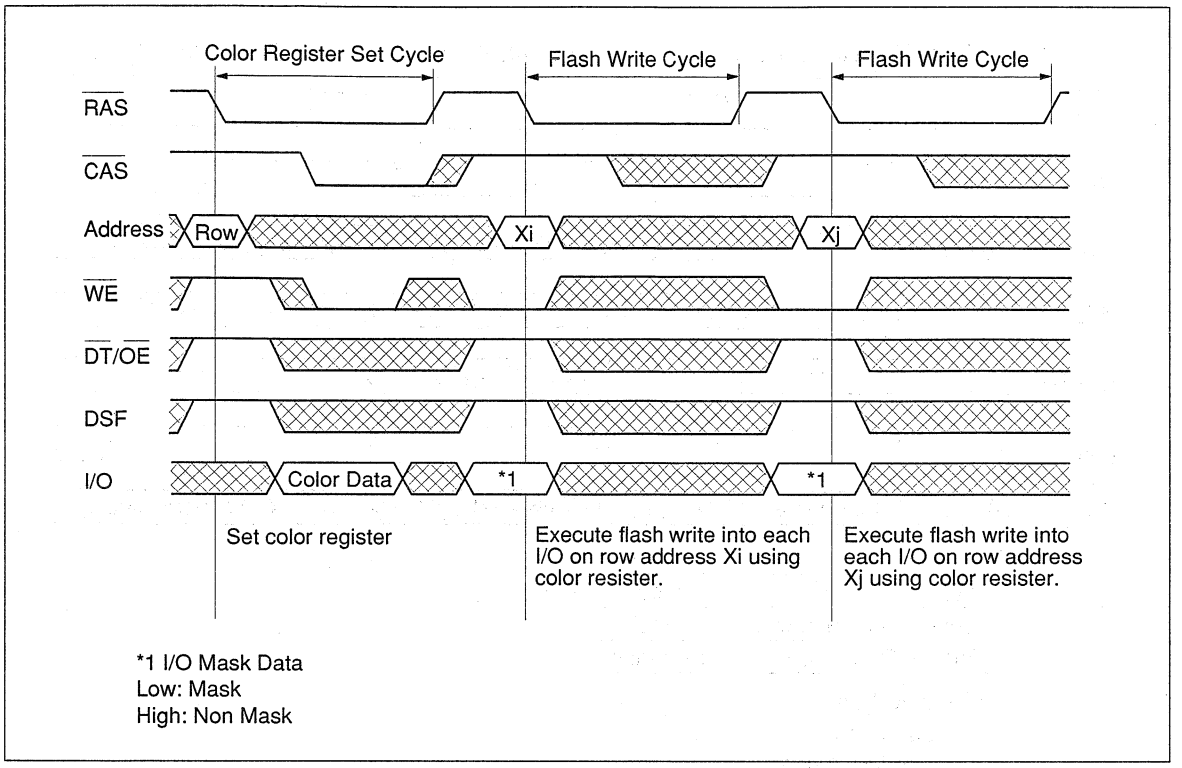


Figure 1 Use of Flash Write

Block Write Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high and DSF low at the falling edge of $\overline{RAS}$, DSF high at the falling edge of $\overline{CAS}$)

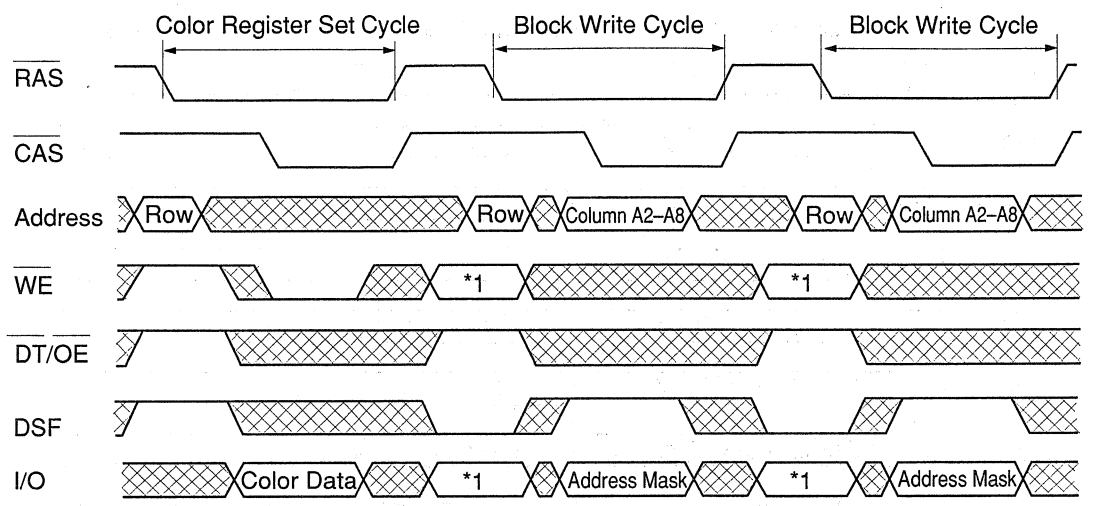
In a block write cycle, 4 columns of data (4-word × 4-bit) is cleared to 0 or 1 at each I/O according to the data of color register. Column addresses A0 and A1 are disregarded. The data on I/Os and addresses can be masked. I/O level at the falling edge of $\overline{CAS}$ determines the address to be cleared. (See figure 2.)

- Normal Mode Block Write cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

The data on 4 I/Os are all cleared when $\overline{WE}$ is high at the falling edge of $\overline{RAS}$.

- Mask Block Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, HM534253A starts mask block write mode to clear the data on an optional I/O. The mask data is the same as that of a RAM write cycle. High I/O is cleared, low I/O is not cleared and the internal data is retained. The mask data is available in the $\overline{RAS}$ cycle. In page mode block write cycle, the mask data is retained during the page access.



*1

WE	I/O	Mode
Low	I/O Mask Data	Mask
High	Don't care	Non mask

I/O Mask Data
Low: Mask
High: Non Mask

Address Mask Data

I/O0	Column0 (A0 = 0, A1 = 0) Mask Data	
I/O1	Column1 (A0 = 1, A1 = 0) Mask Data	Low: Mask
I/O2	Column2 (A0 = 0, A1 = 1) Mask Data	
I/O3	Column3 (A0 = 1, A1 = 1) Mask Data	High: Non Mask

Figure 2 Use of Block Write

Transfer Operation

The HM534253A provides the read transfer cycle, split read transfer cycle, pseudo transfer cycle, write transfer cycle and split write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{CAS}$ high and $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)
Read transfer cycle and
split read transfer cycle: RAM to SAM
Write transfer cycle and
split write transfer cycle: SAM to RAM

(2) Determine SI/O state (except for split read transfer cycle and split write transfer cycle)
Read transfer cycle: SI/O output
Pseudo transfer cycle
and write transfer cycle: SI/O input

(3) Determine first SAM address to access after transferring at column address (SAM start address).
SAM start address must be determined by read transfer cycle or pseudo transfer cycle (split transfer cycle isn't available) before SAM access, after power on, and determined for each transfer cycle.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high and DSF low at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by driving $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high and DSF low at the falling edge of $\overline{RAS}$. The row address data (512 × 4-bit)

determined by this cycle is transferred to SAM data register synchronously at the rising edge of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address determined by column address. In read transfer cycle, $\overline{DT}/\overline{OE}$ must be risen to transfer data from RAM to SAM.

This cycle can access SAM even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge and t_{SDH} (min) specified between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge must be satisfied. (See figure 3.)

When read transfer cycle is executed, SI/O becomes output state by first SAM access. Input must be set high impedance before t_{SZS} (min) of the first SAM access to avoid data contention.

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, $\overline{SE}$ high and DSF low at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle switches SI/O to input state and set SAM start address without data transfer to RAM.

This cycle starts when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, $\overline{SE}$ high and DSF low at the falling edge of $\overline{RAS}$. Data should be input to SI/O later than t_{SID} (min) after $\overline{RAS}$ becomes low to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC must not be risen.

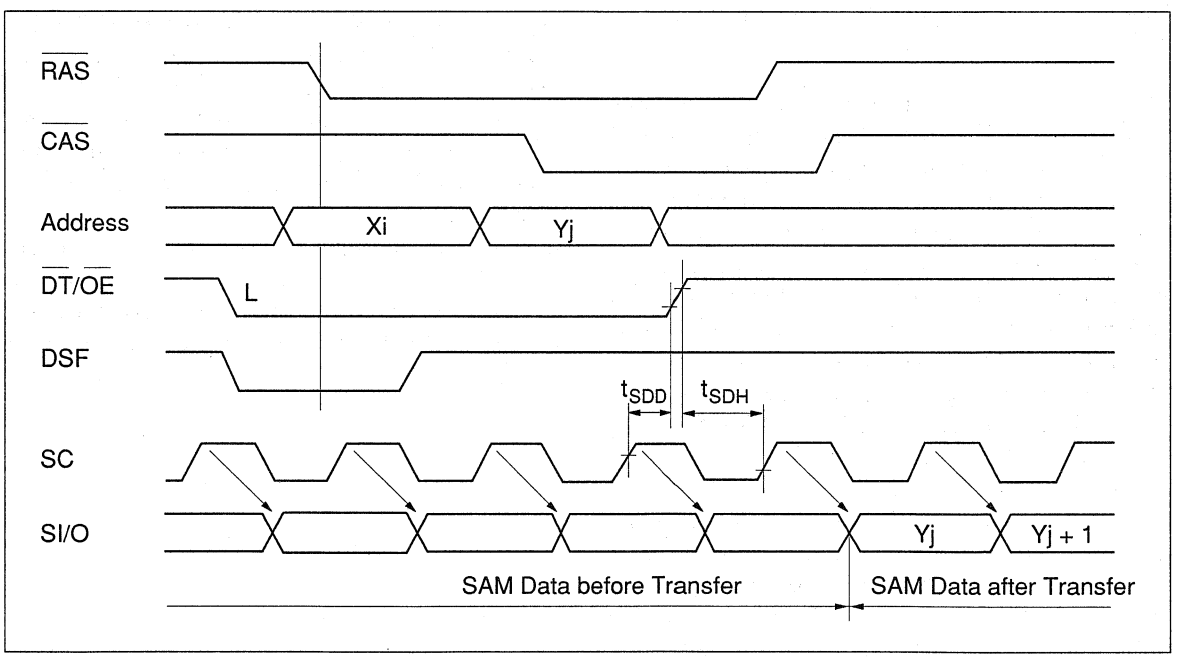


Figure 3 Real Time Read Transfer

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, $\overline{SE}$ low and DSF low at the falling end of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address for serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC must not be risen. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addresses of RAM by write transfer cycle. However, the address to write data must be the same as that of the read transfer cycle or the split read transfer cycle (row address AX8).

Split Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high and DSF high at the falling edge of $\overline{RAS}$)

To execute a continuous serial read by real time read transfer, HM534253A must satisfy SC and $\overline{DT}/\overline{OE}$ timings and requires an external circuit to detect SAM last address. Split read transfer cycle makes it possible to execute a continuous serial read without the above timing limitation. Figure 4 shows the block diagram for a split transfer. SAM data register (DR) consists of 2 split buffers, whose organizations are 256-word × 4-bit each. Let us suppose that data is read from upper data register DR1 (The row address AX8 is 0 and SAM address A8 is 1.). When split read transfer is executed setting row address AX8 0 and SAM start addresses A0 to A7, 256-word × 4-bit data are transferred from RAM to the lower data register DR0 (SAM address A8 is 0) automatically. After data are read from data register DR1, data start to be read from SAM start addresses of data register DR0. If the next split read transfer isn't executed while data are read from data register DR0, data start to be read from SAM start address 0 of DR1 after data are read from data register DR0. If split read transfer is executed setting row address AX8 1 and SAM start addresses A0 to A7 while data are read from data register DR1, 256-word × 4-bit data are transferred to data register DR2. After data are read from data register DR1, data start to be read from SAM start addresses of data register DR2. If the next split read transfer isn't executed while data is read from data register DR2, data start to be read from SAM start address 0 of data register DR3 after data are read from data register DR2. In this time, SAM data is the one transferred to data register DR3 finally while row address AX8 is 1. In split read data transfer, the SAM start address A8 is automatically set in the data register which isn't used.

The data on SAM address A8, which will be accessed next, outputs to QSF, QSF is switched from low to high by accessing SAM last address 255 and from high to low by accessing address 511.

Split read transfer cycle is set when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ is low, $\overline{WE}$ is high and DSF is high at the falling edge of $\overline{RAS}$. The cycle can be executed asyncronously with SC. However, HM534253A must be satisfied t_{STS} (min) timing specified between SC rising and $\overline{RAS}$ falling. SAM start address must be accessed, satisfying t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings specified between $\overline{RAS}$ or $\overline{CAS}$ falling and column address. (See figure 5.)

In split read transfer, SI/O isn't switched to output state. Therefore, read transfer must be executed to switch SI/O to output state when the previous transfer cycle is pseudo transfer or write transfer cycle.

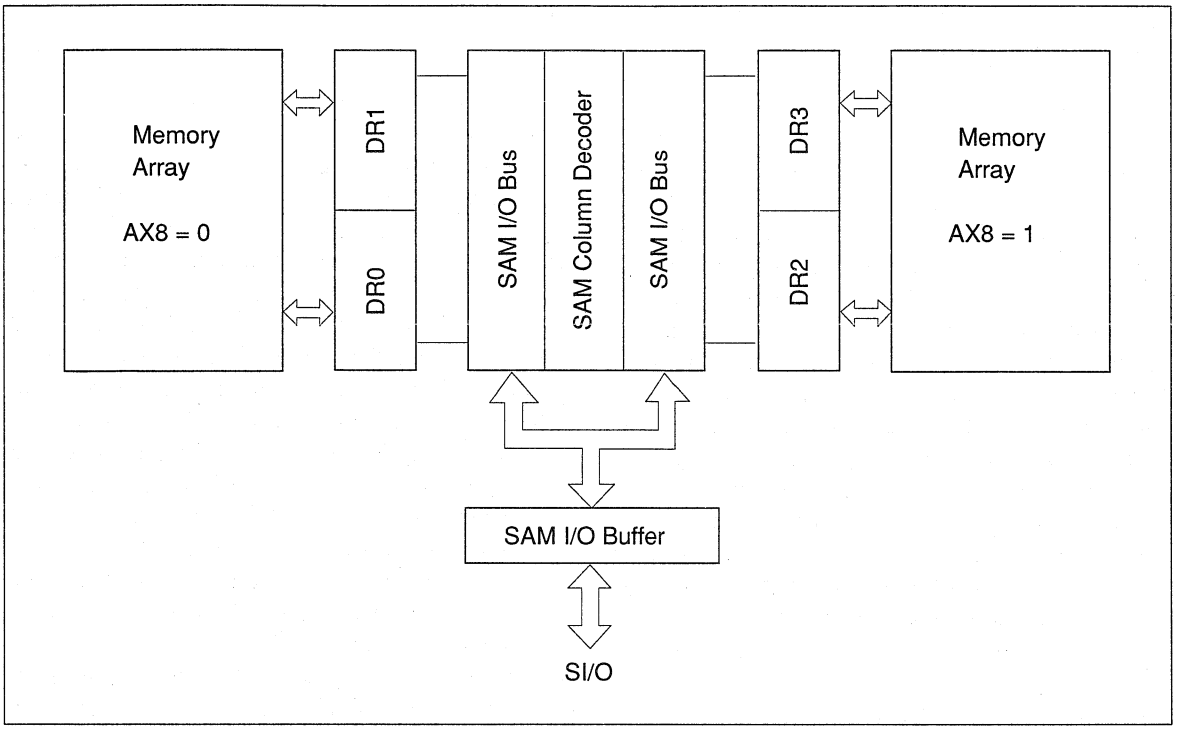


Figure 4 Block Diagram for Split Transfer

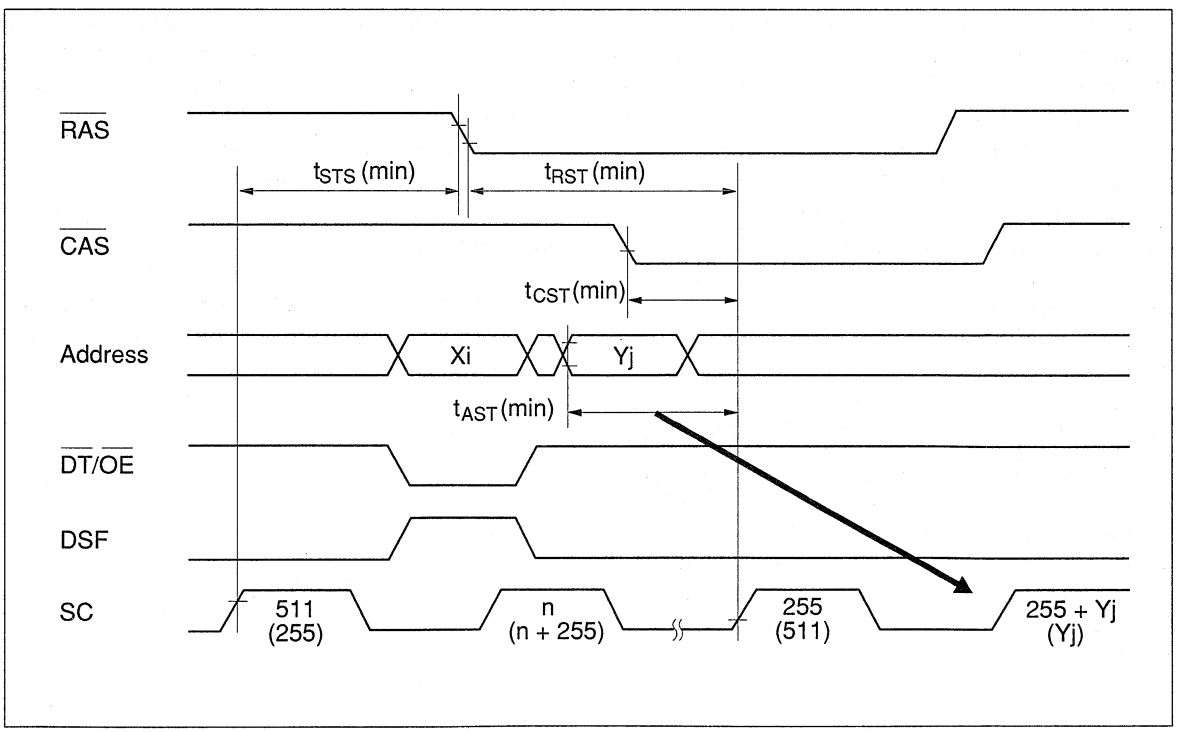


Figure 5 Limitation in Split Transfer

Split Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and DSF high at the falling edge of $\overline{RAS}$)

A continuous serial write cannot be executed because accessing SAM is inhibited during $\overline{RAS}$ low in write transfer. Split write transfer cycle makes it possible. In this cycle, t_{STS} (min), t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings must be satisfied like split read transfer cycle. And it is impossible to switch SI/O to input state in this cycle. If SI/O is in output state, pseudo transfer cycle should be executed to switch SI/O into input state. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addresses of RAM by split write transfer cycle. However, pseudo transfer cycle must be executed before split write transfer cycle. And the MSB of row address (AX8) to write data must be the same as that of the read transfer cycle or the split read transfer cycle.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When $\overline{SE}$ is set high, SI/O becomes high impedance, and the internal pointer is incremented by the SC rising. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is fetched into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't fetched into data register. Internal pointer is incremented by the SC rising, so $\overline{SE}$ high can be used as mask data for SAM. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is executed by accessing all 512 row addresses within 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required when all row addresses are accessed within 8 ms.

(1) $\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is executed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high after inputting the row address (= refresh address) from external circuits. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ must be high at the falling edge of $\overline{RAS}$.

(2) CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate.

(3) Hidden Refresh Cycle: Hidden refresh cycle executes CBR refresh with the data output by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register and selector), organized as fully static circuitry, require no refresh.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage*1	V_T	–1.0 to +7.0	V
Power supply voltage*1	V_{CC}	–0.5 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to 70	°C
Storage temperature	Tstg	–55 to +125	°C

Note: 1. Relative to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage*1	V_{CC}	4.5	5.0	5.5	V
Input high voltage*1	V_{IH}	2.4	—	6.5	V
Input low voltage*1	V_{IL}	–0.5*2	—	0.8	V

Notes: 1. All voltages referenced to V_{SS}.
2. –3.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM534253A										
		-6		-7		-8		-10			Test conditions	
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	RAM port	SAM port
Operating current	I_{CC1}	—	75	—	70	—	60	—	55	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC7}	—	125	—	120	—	100	—	95	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Standby current	I_{CC2}	—	7	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ =V_{IH}	SC =V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC8}	—	50	—	50	—	40	—	40	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
$\overline{RAS}$-only refresh current	I_{CC3}	—	75	—	70	—	60	—	55	mA	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH} t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC9}	—	125	—	120	—	100	—	95	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Page mode current	I_{CC4}	—	80	—	80	—	70	—	65	mA	$\overline{CAS}$ cycling $\overline{RAS}$ = V_{IL} t_{PC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10}	—	130	—	130	—	110	—	105	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	—	50	—	45	—	40	—	35	mA	$\overline{RAS}$ cycling t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC11}	—	100	—	95	—	80	—	75	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Data transfer current	I_{CC6}	—	80	—	75	—	65	—	60	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC12}	—	130	—	125	—	105	—	100	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	–10	10	µA		
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	–10	10	µA		
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V	I_{OH} = –2 mA	
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V	I_{OL} = 4.2 mA	

Note: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once while $\overline{RAS}$ is low and $\overline{CAS}$ is high.

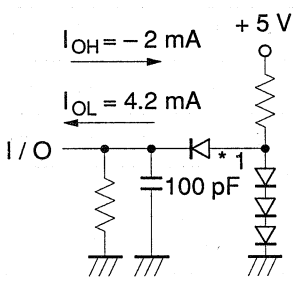
Capacitance (Ta = 25°C, V_{CC} = 5 V, f = 1 MHz, Bias: Clock, I/O = V_{CC}, address = V_{SS})

Item	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clock	C_{I2}	—	—	5	pF
I/O, SI/O, QSF	$C_{I/O}$	—	—	7	pF

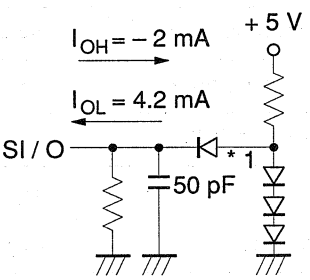
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) *1, *16

Test Conditions

- Input rise and fall time: 5 ns
- Output load: See figures
- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V



Output Load (A)



Output Load (B)

Note: 1. Including scope & jig.

Common Parameter

Item	Symbol	HM534253A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
Random read or write cycle time	t_{RC}	125	—	135	—	150	—	180	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	55	—	55	—	60	—	70	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	—	20	—	20	—	25	—	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	20	60	20	75	ns	2
$\overline{RAS}$ hold time referenced to $\overline{CAS}$	t_{RSH}	20	—	20	—	20	—	25	—	ns	
$\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Transition time (rise to fall)	t_T	3	50	3	50	3	50	3	50	ns	3
Refresh period	t_{REF}	—	8	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ setup time	t_{DTS}	0	—	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ hold time	t_{DTH}	10	—	10	—	10	—	10	—	ns	
DSF to $\overline{RAS}$ setup time	t_{FSR}	0	—	0	—	0	—	0	—	ns	
DSF to $\overline{RAS}$ hold time	t_{RFH}	10	—	10	—	10	—	10	—	ns	
DSF to $\overline{CAS}$ setup time	t_{FSC}	0	—	0	—	0	—	0	—	ns	
DSF to $\overline{CAS}$ hold time	t_{CFH}	15	—	15	—	15	—	15	—	ns	
Data-in to $\overline{CAS}$ delay time	t_{DZC}	0	—	0	—	0	—	0	—	ns	4
Data-in to $\overline{OE}$ delay time	t_{DZO}	0	—	0	—	0	—	0	—	ns	4
Output buffer turn-off delay referenced to $\overline{CAS}$	t_{OFF1}	—	20	—	20	—	20	—	20	ns	5
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	—	20	—	20	—	20	—	20	ns	5

Read Cycle (RAM), Page Mode Read Cycle

		HM534253A									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	35	—	40	—	45	ns	7, 9
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	0	—	ns	10
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	10
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	2
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	35	—	40	—	45	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	35	—	35	—	40	—	45	—	ns	
Page mode cycle time	t_{PC}	45	—	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	10	—	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	—	40	—	45	—	50	ns	
Page mode $\overline{RAS}$ pulse width	t_{RASP}	60	100000	70	100000	80	100000	100	100000	ns	

Write Cycle (RAM), Page Mode Write Cycle Color Register Set Cycle

		HM534253A									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
Write command setup time	t_{WCS}	0	—	0	—	0	—	0	—	ns	11
Write command hold time	t_{WCH}	15	—	15	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	15	—	15	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	15	—	15	—	15	—	15	—	ns	12
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	10	—	10	—	10	—	10	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	10	—	10	—	10	—	10	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	20	—	20	—	20	—	20	—	ns	
Page mode cycle time	t_{PC}	45	—	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ to data-in delay time	t_{CDD}	20	—	20	—	20	—	20	—	ns	13
Page mode $\overline{RAS}$ pulse width	t_{RASP}	60	100000	70	100000	80	100000	100	100000	ns	

Read-Modify-Write Cycle

		HM534253A									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
Read-modify-write cycle time	t_{RWC}	175	—	185	—	200	—	230	—	ns	
$\overline{RAS}$ pulse width (read-modify-write cycle)	t_{RWS}	110	10000	120	10000	130	10000	150	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	45	—	45	—	45	—	50	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	60	—	60	—	65	—	70	—	ns	14
$\overline{OE}$ to data-in delay time	t_{ODD}	20	—	20	—	20	—	20	—	ns	12
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	35	—	40	—	45	ns	7, 9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	20	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	15	—	15	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	15	—	15	—	15	—	15	—	ns	12
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	20	—	20	—	20	—	20	—	ns	

Refresh Cycle

Item	Symbol	HM534253A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

Flash Write Cycle, Block Write Cycle

Item	Symbol	HM534253A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
$\overline{CAS}$ to data-in delay time	t_{CDD}	20	—	20	—	20	—	20	—	ns	13
$\overline{OE}$ to data-in delay time	t_{ODD}	20	—	20	—	20	—	20	—	ns	13

Read Transfer Cycle

Item	Symbol	HM534253A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
$\overline{DT}$ hold time referenced to $\overline{RAS}$	t_{RDH}	50	10000	60	—	65	10000	80	10000	ns	
$\overline{DT}$ hold time referenced to $\overline{CAS}$	t_{CDH}	20	—	20	—	20	—	25	—	ns	
$\overline{DT}$ hold time referenced to column address	t_{ADH}	25	—	25	—	30	—	30	—	ns	
$\overline{DT}$ precharge time	t_{DTP}	20	—	20	—	20	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ delay time	t_{DRD}	65	—	65	—	70	—	80	—	ns	
SC to $\overline{RAS}$ setup time	t_{SRS}	25	—	25	—	30	—	30	—	ns	
1'st SC to $\overline{RAS}$ hold time	t_{SRH}	60	—	70	—	80	—	100	—	ns	
1'st SC to $\overline{CAS}$ hold time	t_{SCH}	25	—	25	—	25	—	25	—	ns	

Read Transfer Cycle (cont)

Item	Symbol	HM534253A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
1'st SC to colume address hold time	t_{SAH}	40	—	40	—	45	—	50	—	ns	
Last SC to $\overline{DT}$ delay time	t_{SDD}	5	—	5	—	5	—	5	—	ns	
1'st SC to $\overline{DT}$ hold time	t_{SDH}	10	—	10	—	15	—	15	—	ns	
$\overline{RAS}$ to QSF delay time	t_{RQD}	—	65	—	70	—	75	—	85	ns	15
$\overline{CAS}$ to QSF delay time	t_{CQD}	—	35	—	35	—	40	—	40	ns	15
$\overline{DT}$ to QSF delay time	t_{DQD}	—	35	—	35	—	35	—	35	ns	15
QSF hold time referenced to $\overline{RAS}$	t_{RQH}	20	—	20	—	20	—	25	—	ns	
QSF hold time referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	5	—	5	—	ns	
QSF hold time referenced to $\overline{DT}$	t_{DQH}	5	—	5	—	5	—	5	—	ns	
Serial data-in to 1'st SC delay time	t_{SZS}	0	—	0	—	0	—	0	—	ns	
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	35	—	40	—	45	—	ns	
$\overline{RAS}$ precharge to $\overline{DT}$ high hold time	t_{DTHH}	10	—	10	—	10	—	10	—	ns	

Pseudo Transfer Cycle, Write Transfer Cycle

Item	Symbol	HM534253A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
$\overline{SE}$ setup time referenced to $\overline{RAS}$	t_{ES}	0	—	0	—	0	—	0	—	ns	
$\overline{SE}$ hold time referenced to $\overline{RAS}$	t_{EH}	10	—	10	—	10	—	10	—	ns	
SC setup time referenced to $\overline{RAS}$	t_{SRS}	25	—	25	—	30	—	30	—	ns	
$\overline{RAS}$ to SC delay time	t_{SRD}	20	—	20	—	25	—	25	—	ns	
Serial output buffer turn-off time referenced to $\overline{RAS}$	t_{SRZ}	10	40	10	40	10	45	10	50	ns	
$\overline{RAS}$ to serial data-in delay time	t_{SID}	40	—	40	—	45	—	50	—	ns	
$\overline{RAS}$ to QSF delay time	t_{RQD}	—	65	—	70	—	75	—	85	ns	15
$\overline{CAS}$ to QSF delay time	t_{CQD}	—	35	—	35	—	40	—	40	ns	15
QSF hold time referenced to $\overline{RAS}$	t_{RQH}	20	—	20	—	20	—	25	—	ns	
QSF hold time referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	5	—	5	—	ns	
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
$\overline{SE}$ access time	t_{SEA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial write enable setup time	t_{SWS}	5	—	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	

Split Read Transfer Cycle, Split Write Transfer Cycle

		HM534253A									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
Split transfer setup time	t_{STS}	20	—	20	—	20	—	25	—	ns	
Split transfer hold time referenced to $\overline{RAS}$	t_{RST}	60	—	70	—	80	—	100	—	ns	
Split transfer hold time referenced to $\overline{CAS}$	t_{CST}	20	—	20	—	20	—	25	—	ns	
Split transfer hold time referenced to column address	t_{AST}	35	—	35	—	40	—	45	—	ns	
SC to QSF delay time	t_{SQD}	—	30	—	30	—	30	—	30	ns	15
QSF hold time referenced to SC	t_{SQH}	5	—	5	—	5	—	5	—	ns	
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	35	—	40	—	45	—	ns	

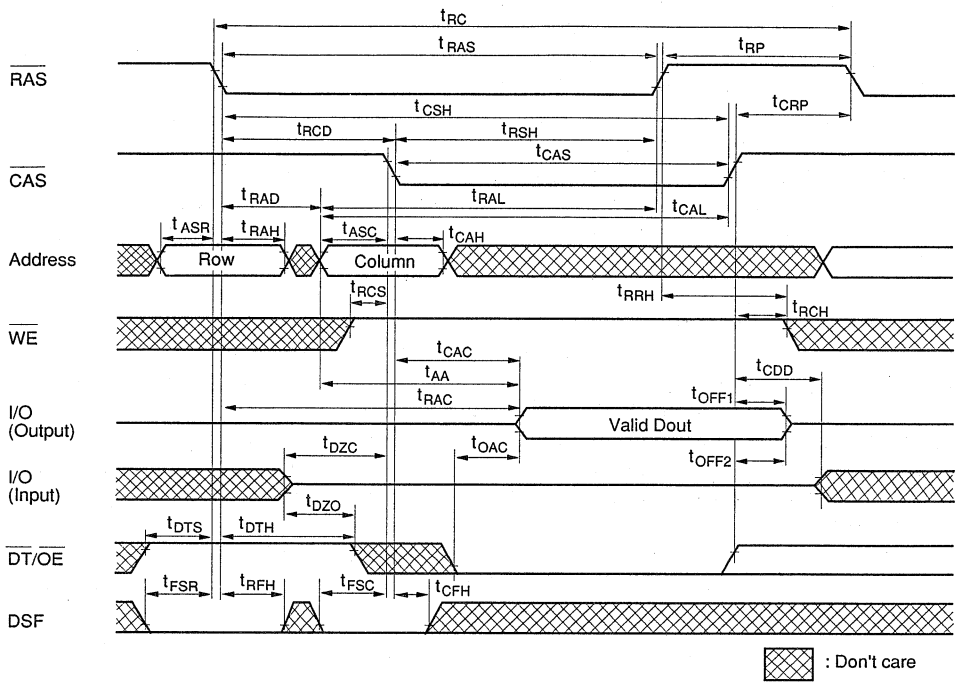
Serial Read Cycle, Serial Write Cycle

		HM534253A									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Access time from SC	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
Access time from $\overline{SE}$	t_{SEA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial output buffer turn-off time referenced to $\overline{SE}$	t_{SEZ}	—	20	—	20	—	20	—	20	ns	5
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	
Serial write enable setup time	t_{SWS}	5	—	5	—	5	—	5	—	ns	
Serial write enable hold time	t_{SWH}	15	—	15	—	15	—	15	—	ns	
Serial write disable setup time	t_{SWIS}	5	—	5	—	5	—	5	—	ns	
Serial write disable hold time	t_{SWIH}	15	—	15	—	15	—	15	—	ns	

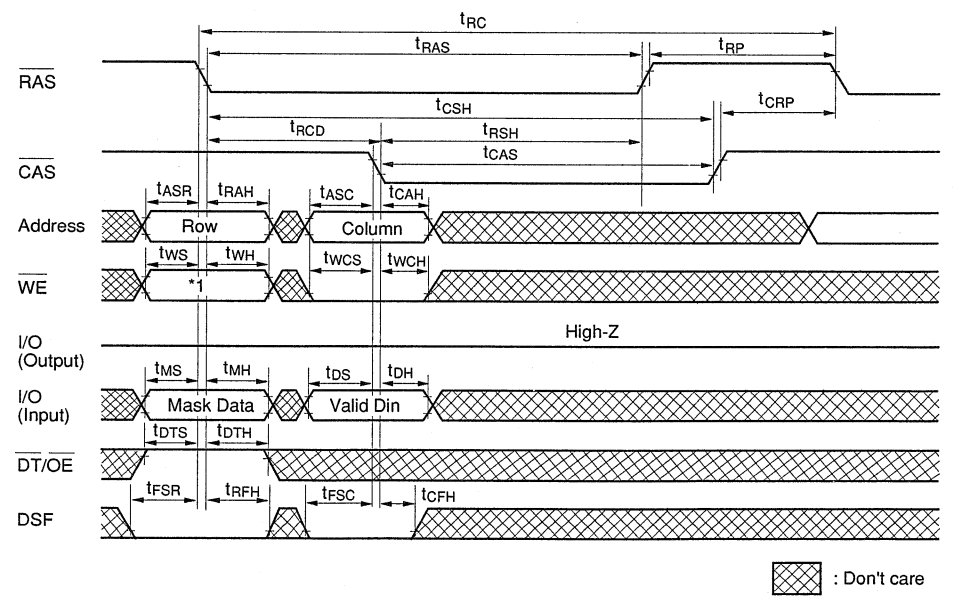
Notes:
1. AC measurements assume t_T = 5 ns.
2. When $t_{RCD} > t_{RCD}$ (max) or $t_{RAD} > t_{RAD}$ (max), access time is specified by t_{CAC} or t_{AA}.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition time t_T is measured between V_{IH} and V_{IL}.
4. Data input must be floating before output buffer is turned on. In read cycle, read-modify-write cycle and delayed write cycle, either t_{DZC} (min) or t_{DZO} (min) must be satisfied.
5. t_{OFF1} (max), t_{OFF2} (max) and t_{SEZ} (max) are defined as the time at which the output achieves the open circuit condition (V_{OH} −100 mV, V_{OL} +100 mV).
6. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
8. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
9. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
10. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.
11. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
12. These parameters are specified by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
13. Either t_{CDD} (min) or t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{CAS}$ or $\overline{OE}$ prior to applying data to the device when output buffer is on.
14. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min) in read-modify-write cycle, the data of the selected address outputs to an I/O pin and input data is written into the selected address. t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{OE}$ prior to applying data to the device.
15. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
16. After power-up, pause for 100 µs or more and execute at least 8 initialization cycle (normal memory cycle or refresh cycle), then start operation.

Timing Waveforms

Read Cycle

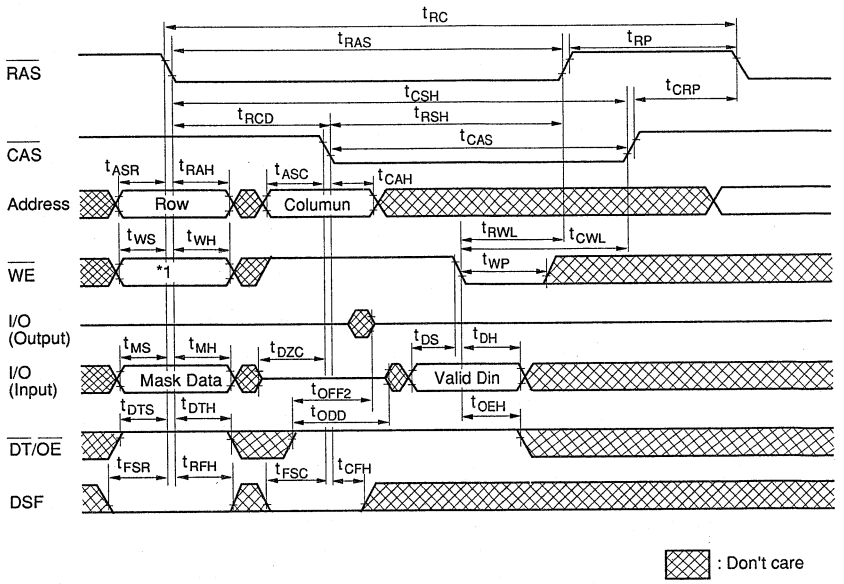


Early Write Cycle



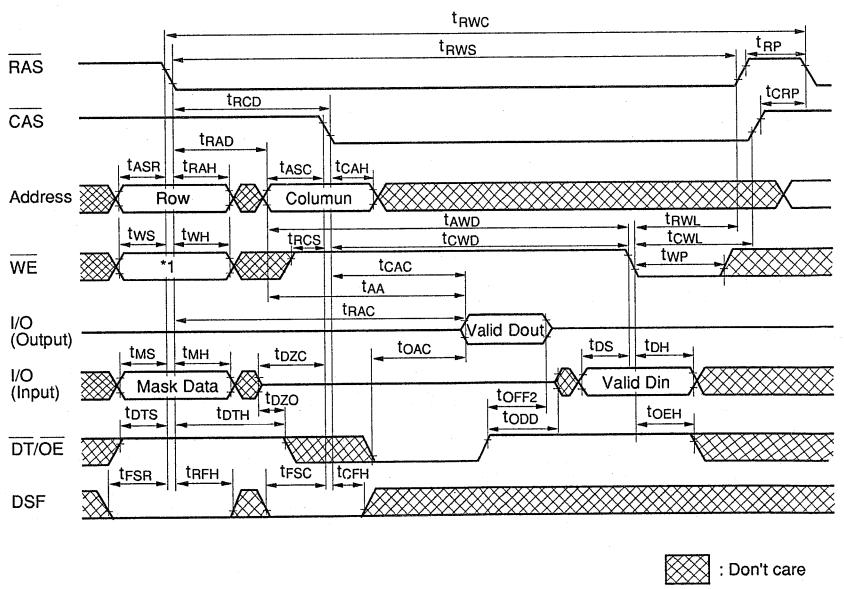
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Delayed Write Cycle



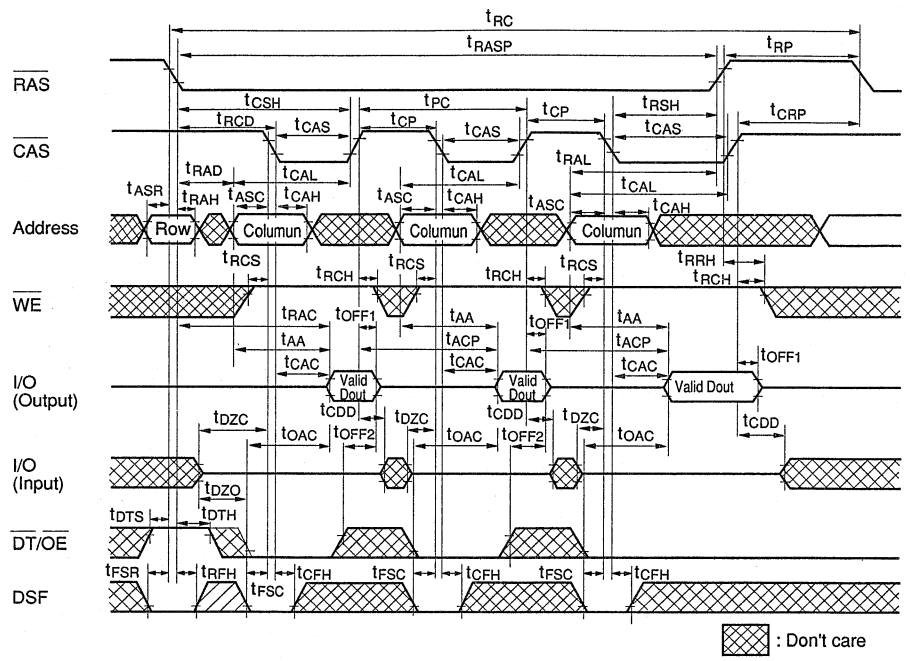
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Read-Modify-Write Cycle

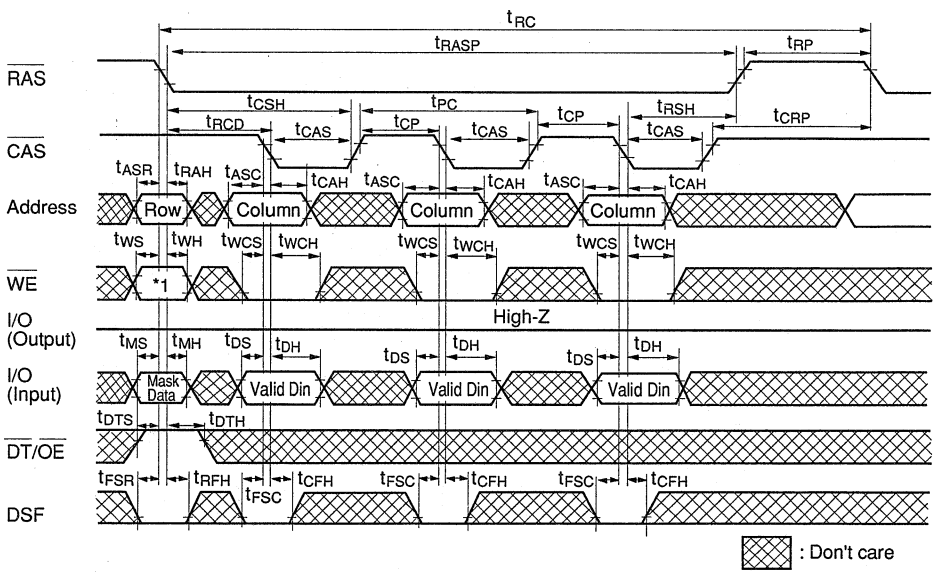


Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Page Mode Read Cycle

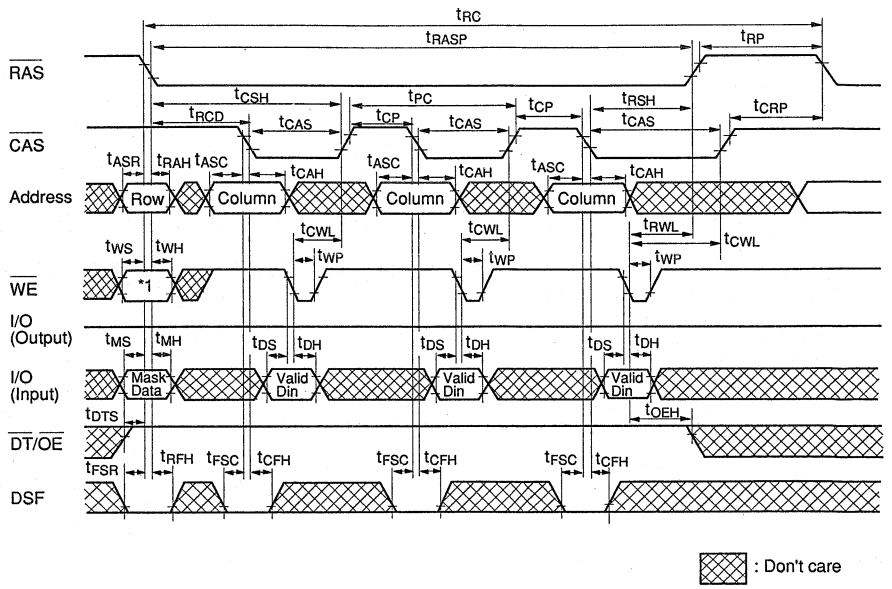


Page Mode Write Cycle (Early Write)



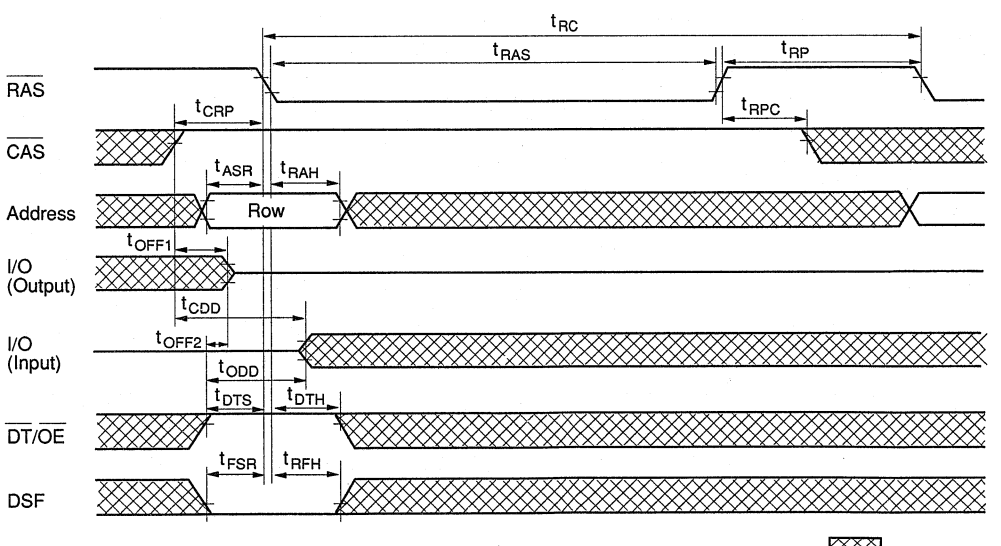
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Page Mode Write Cycle (Delayed Write)

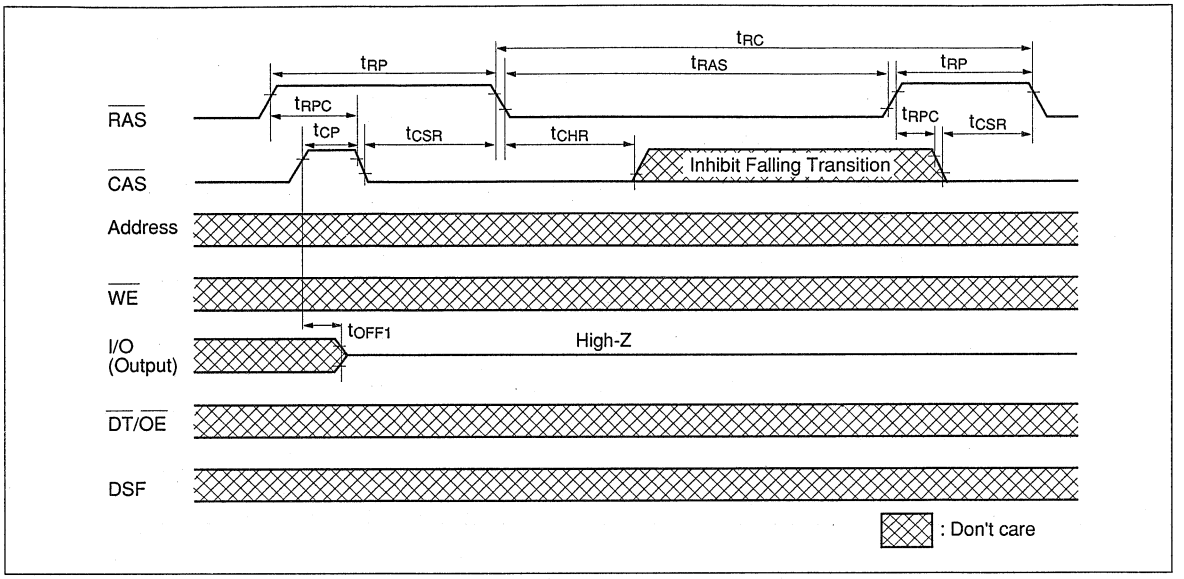


Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

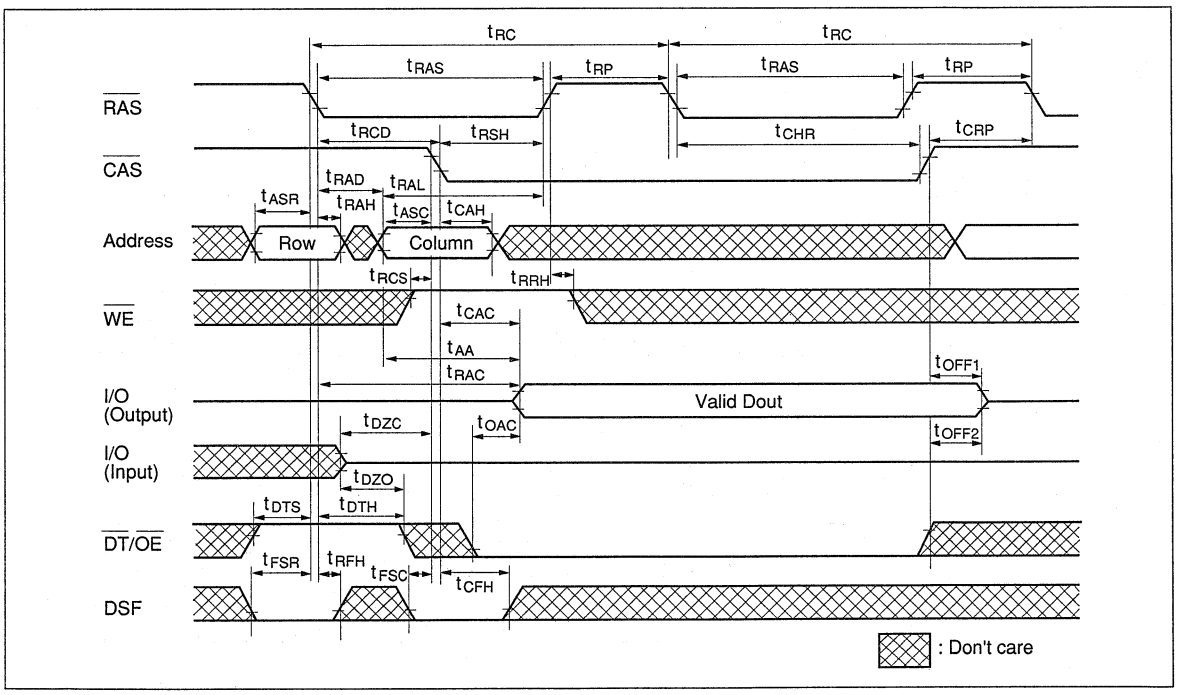
$\overline{RAS}$-Only Refresh Cycle



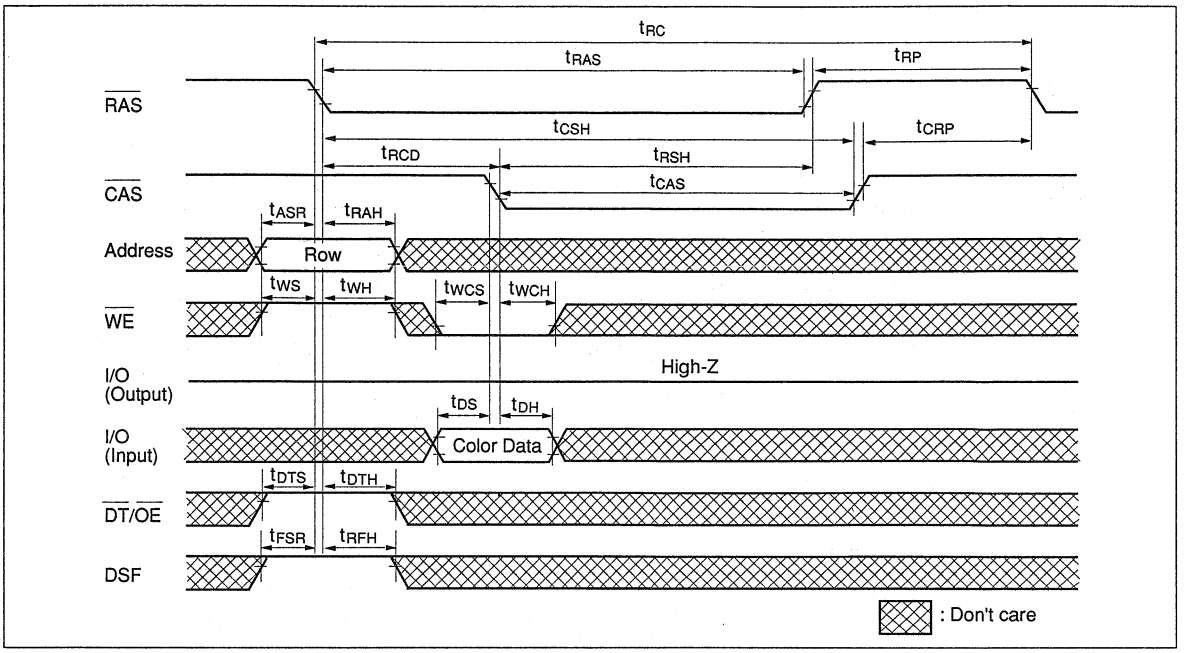
CAS-Before-RAS Refresh Cycle



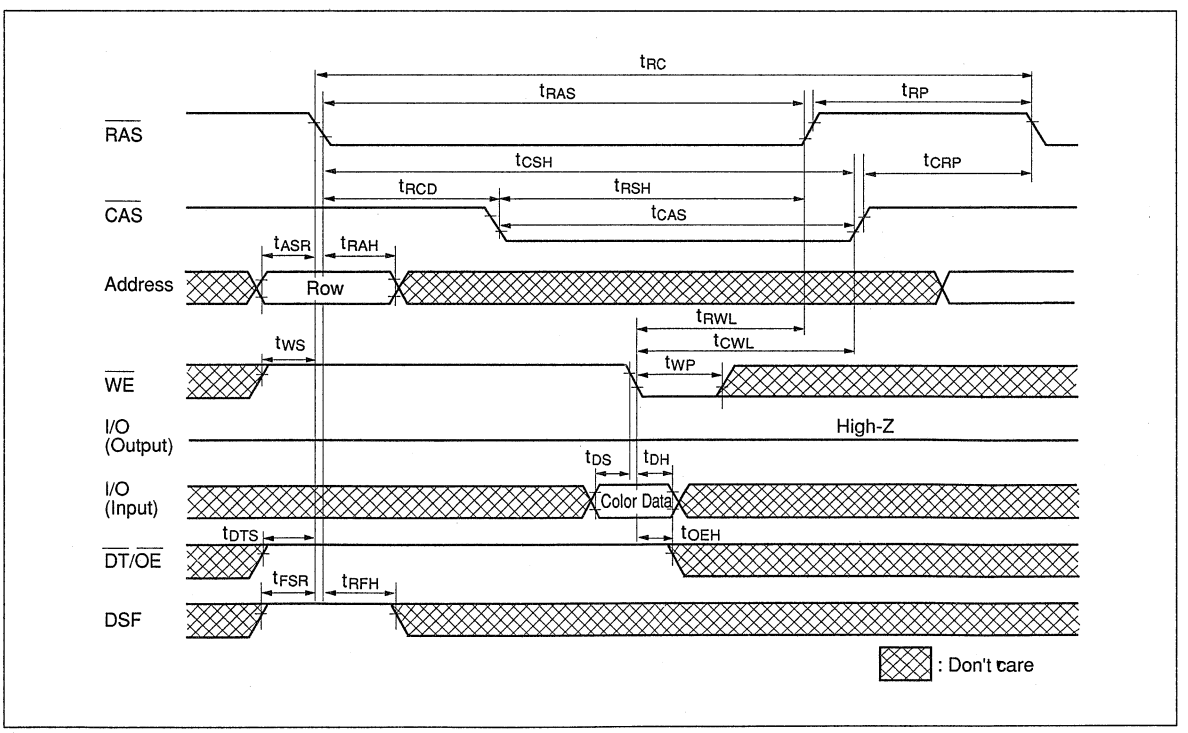
Hidden Refresh Cycle



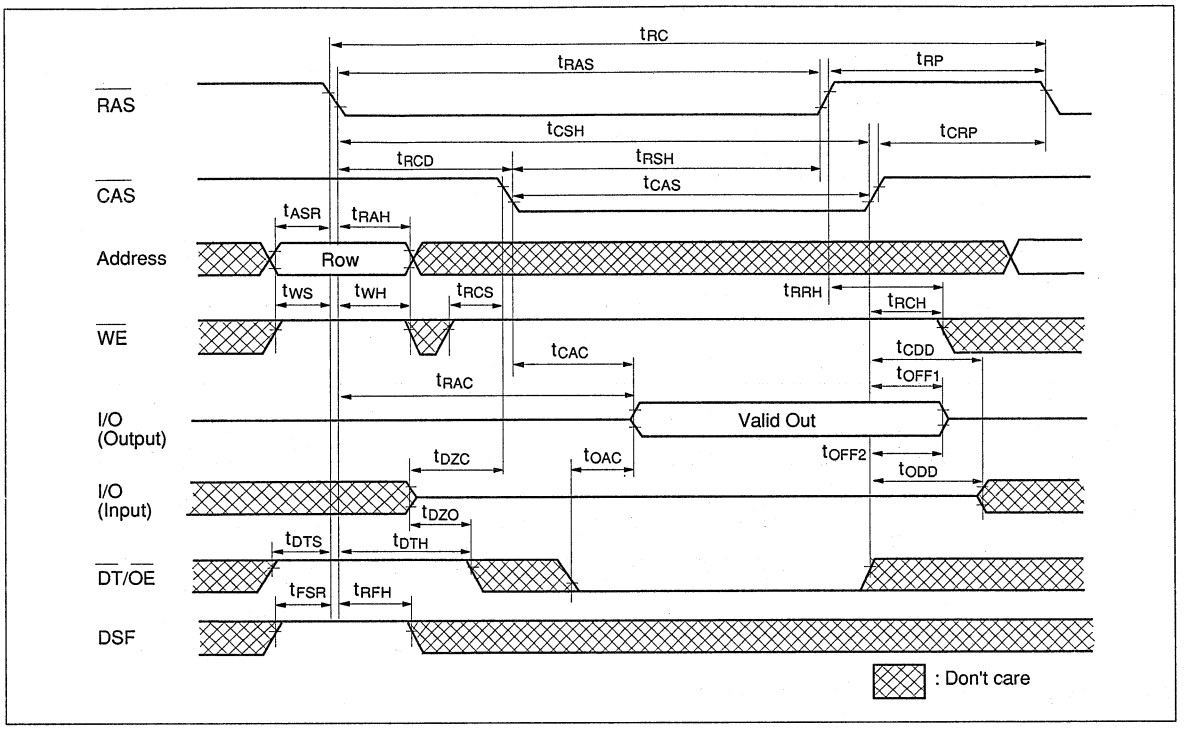
Color Register Set Cycle (Early Write)



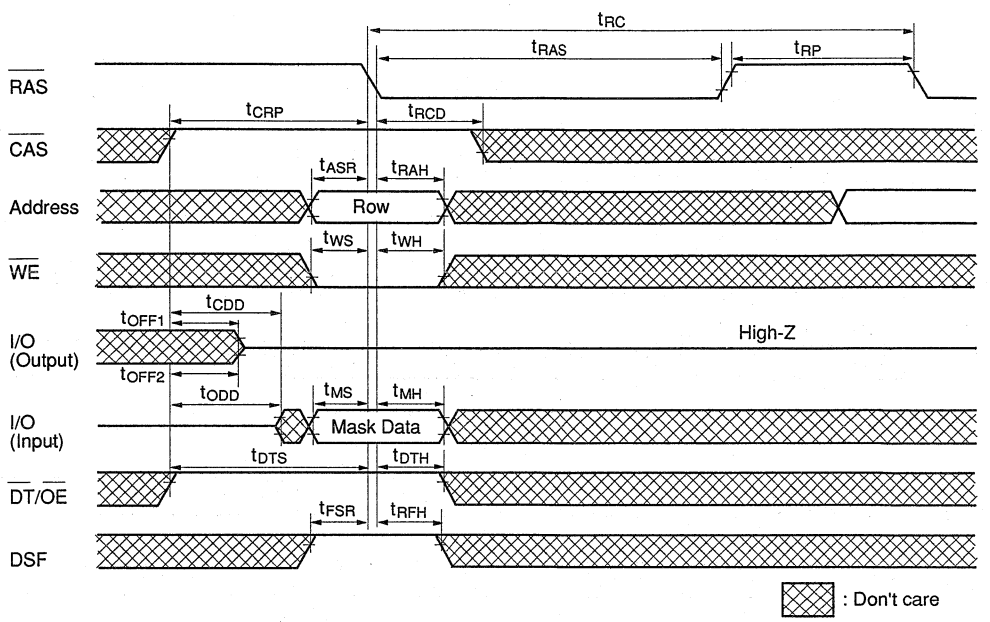
Color Register Set Cycle (Delayed Write)



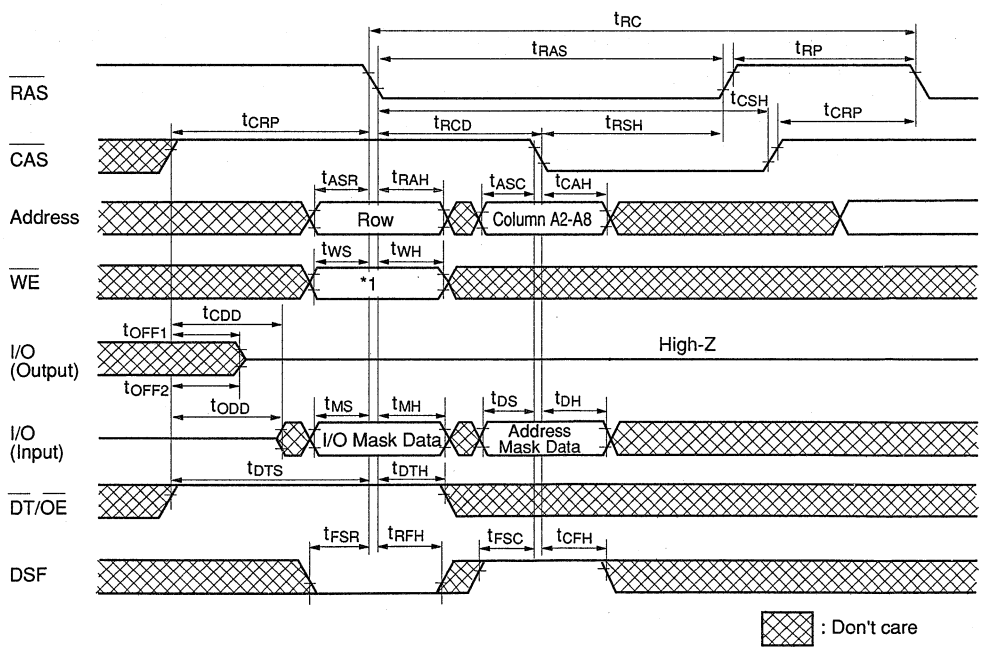
Color Register Read Cycle



Flash Write Cycle

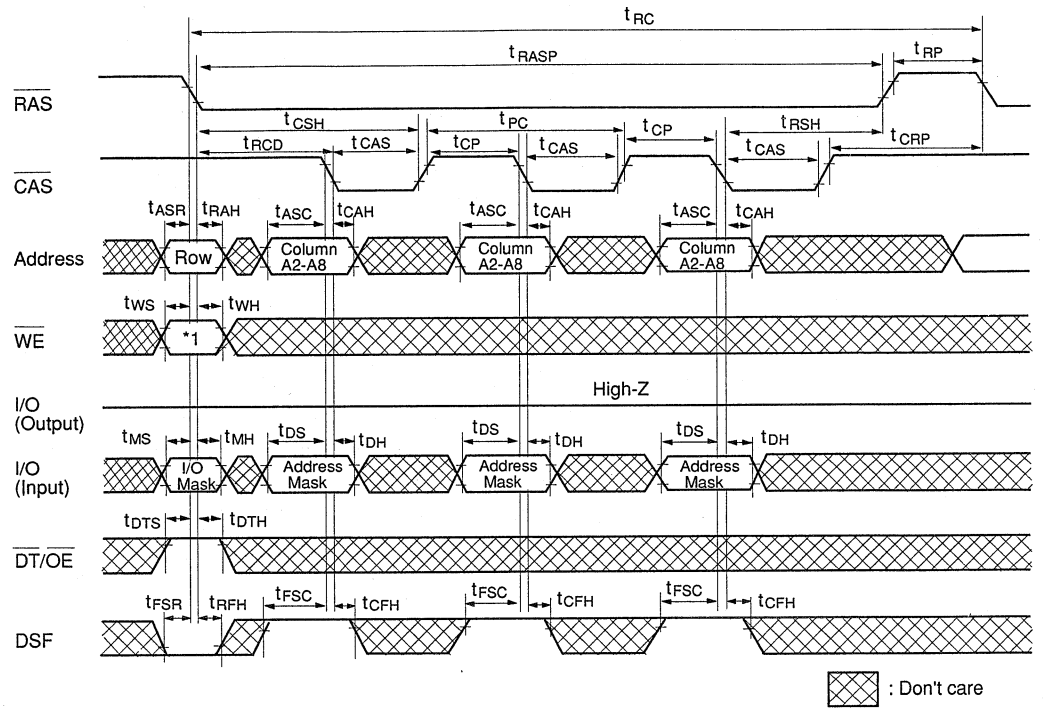


Block Write Cycle



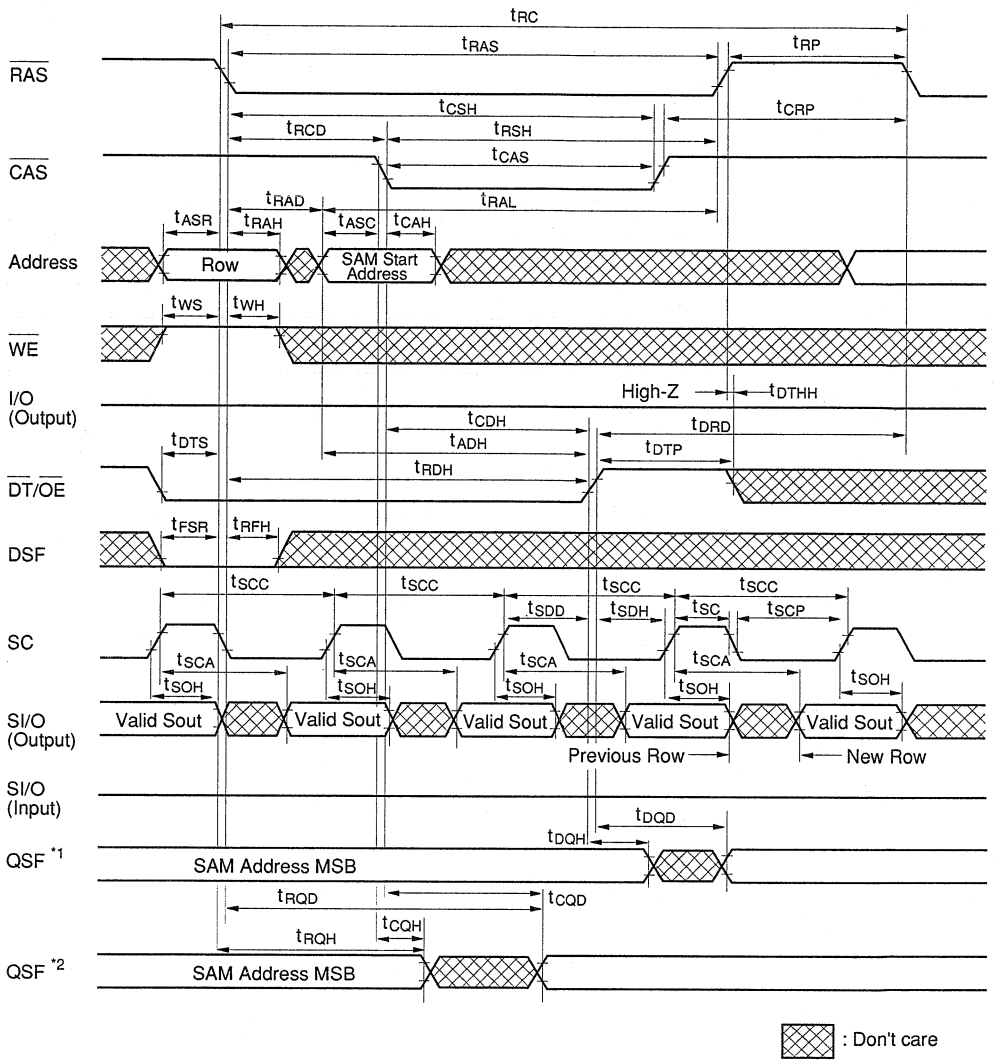
Note: 1. This cycle becomes a normal block write cycle when $\overline{WE}$ is high and a mask block write cycle when $\overline{WE}$ is low.

Page Mode Block Write Cycle



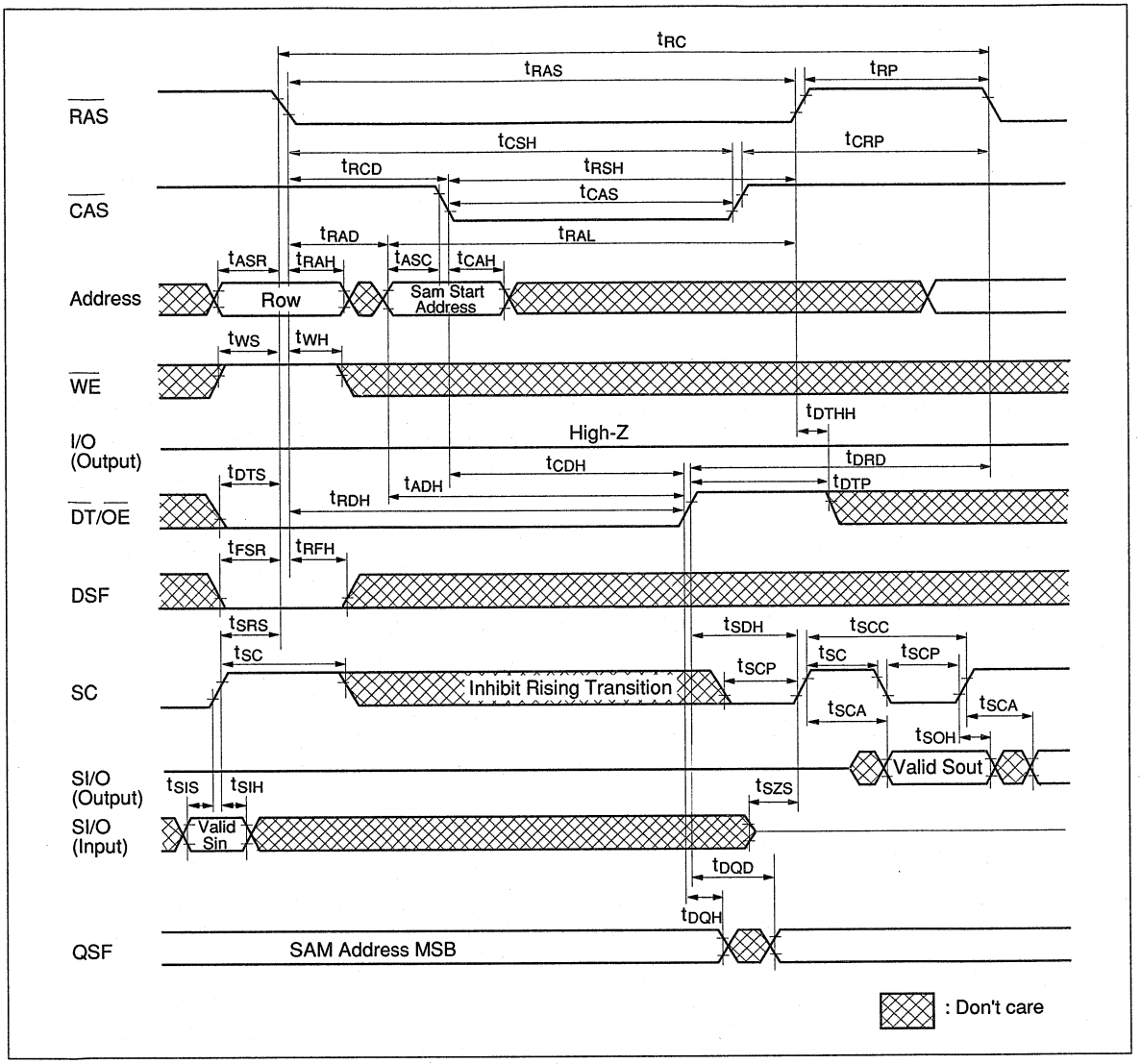
Note: 1. This cycle becomes a normal block write cycle when $\overline{WE}$ is high and a mask block write cycle when $\overline{WE}$ is low.

Read Transfer Cycle (1)

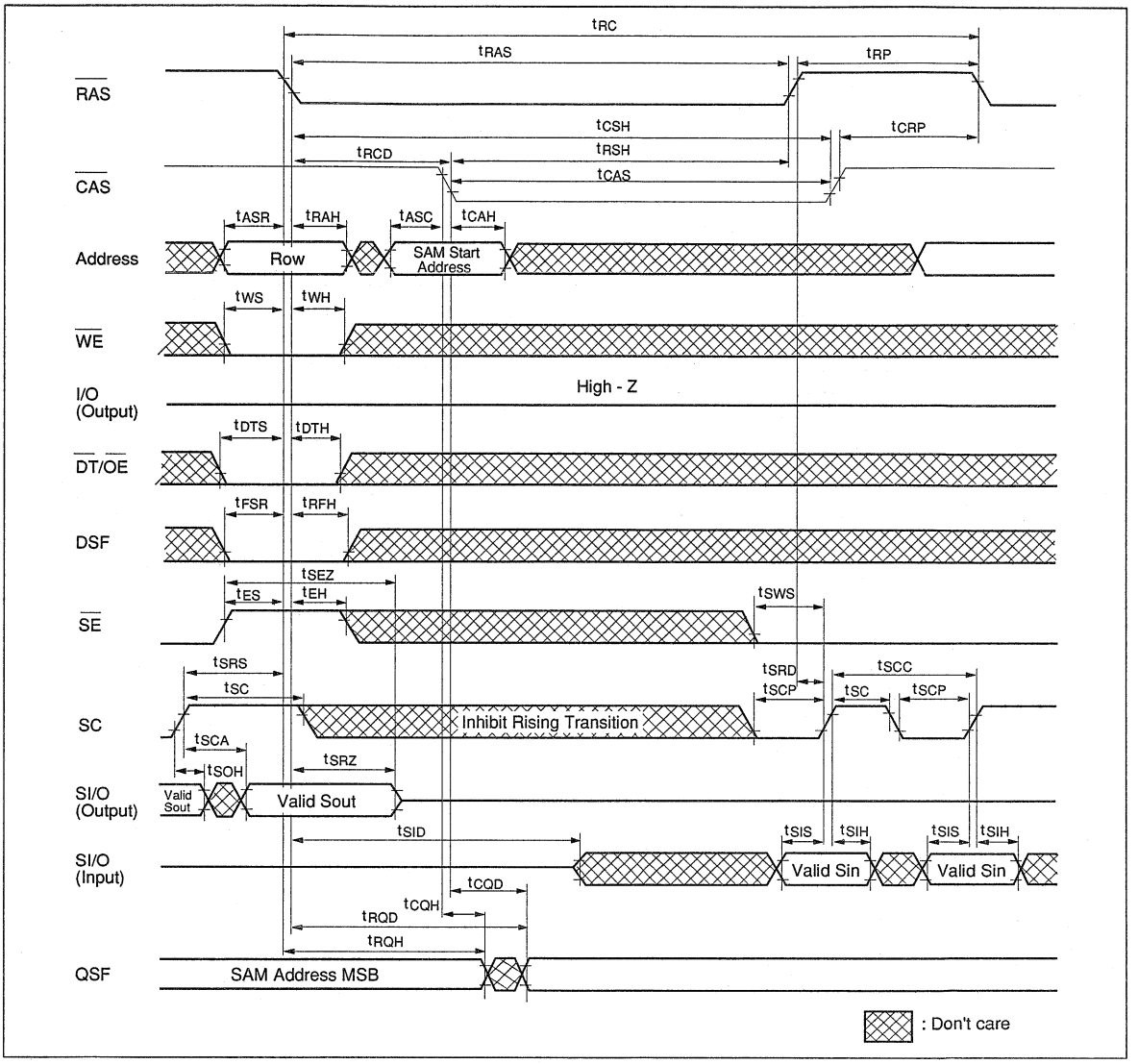


Notes: 1. This QSF timing is referred when SC is risen once or more between the previous transfer cycle and $\overline{CAS}$ falling edge of this cycle (QSF is switched by $\overline{DT}$ rising).
2. This QSF timing is referred when SC isn't risen between the previous transfer cycle and $\overline{CAS}$ falling edge of this cycle (QSF is switched by $\overline{RAS}$ or $\overline{CAS}$ falling).

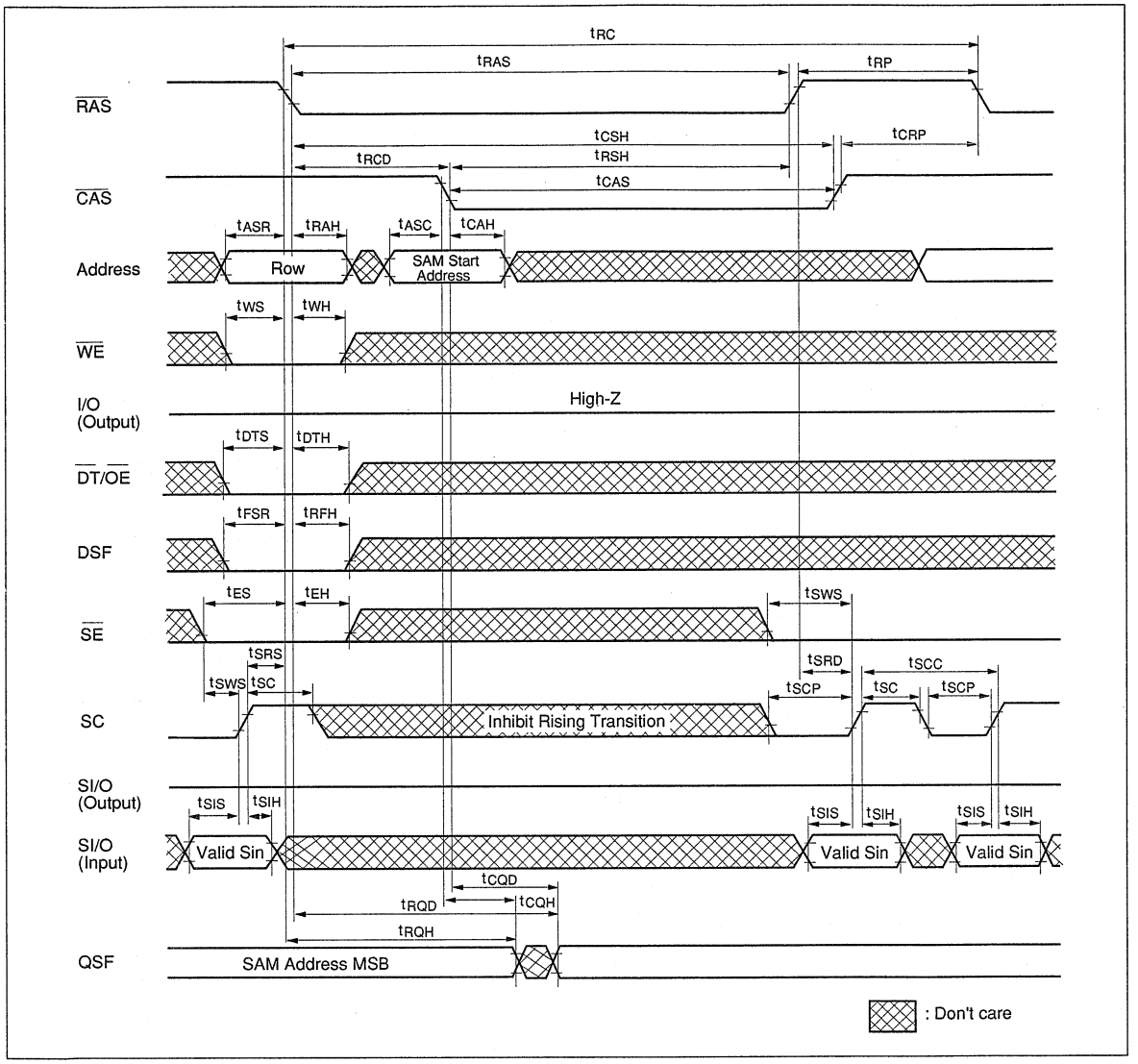
Read Transfer Cycle (2)



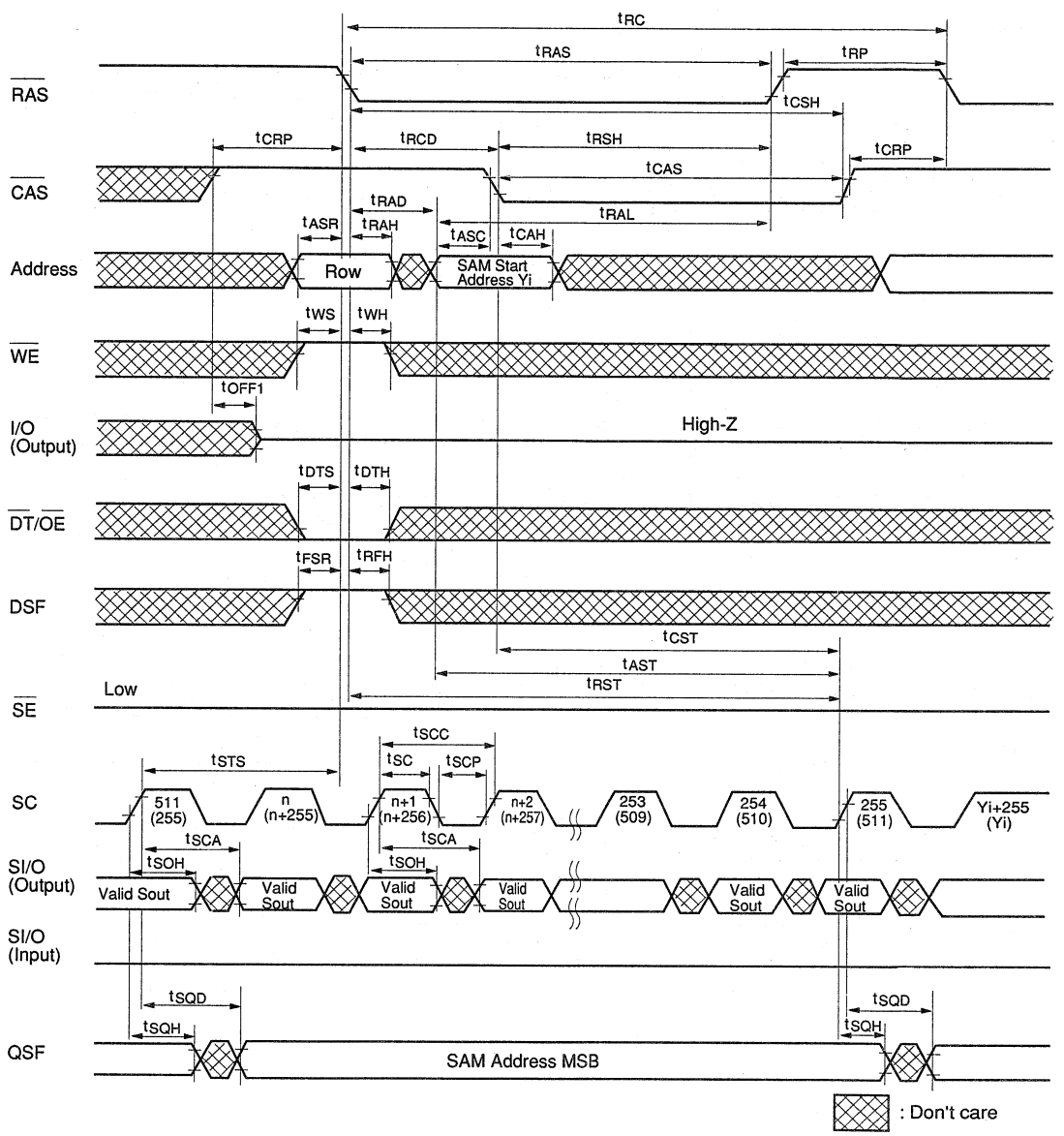
Pseudo Transfer Cycle



Write Transfer Cycle

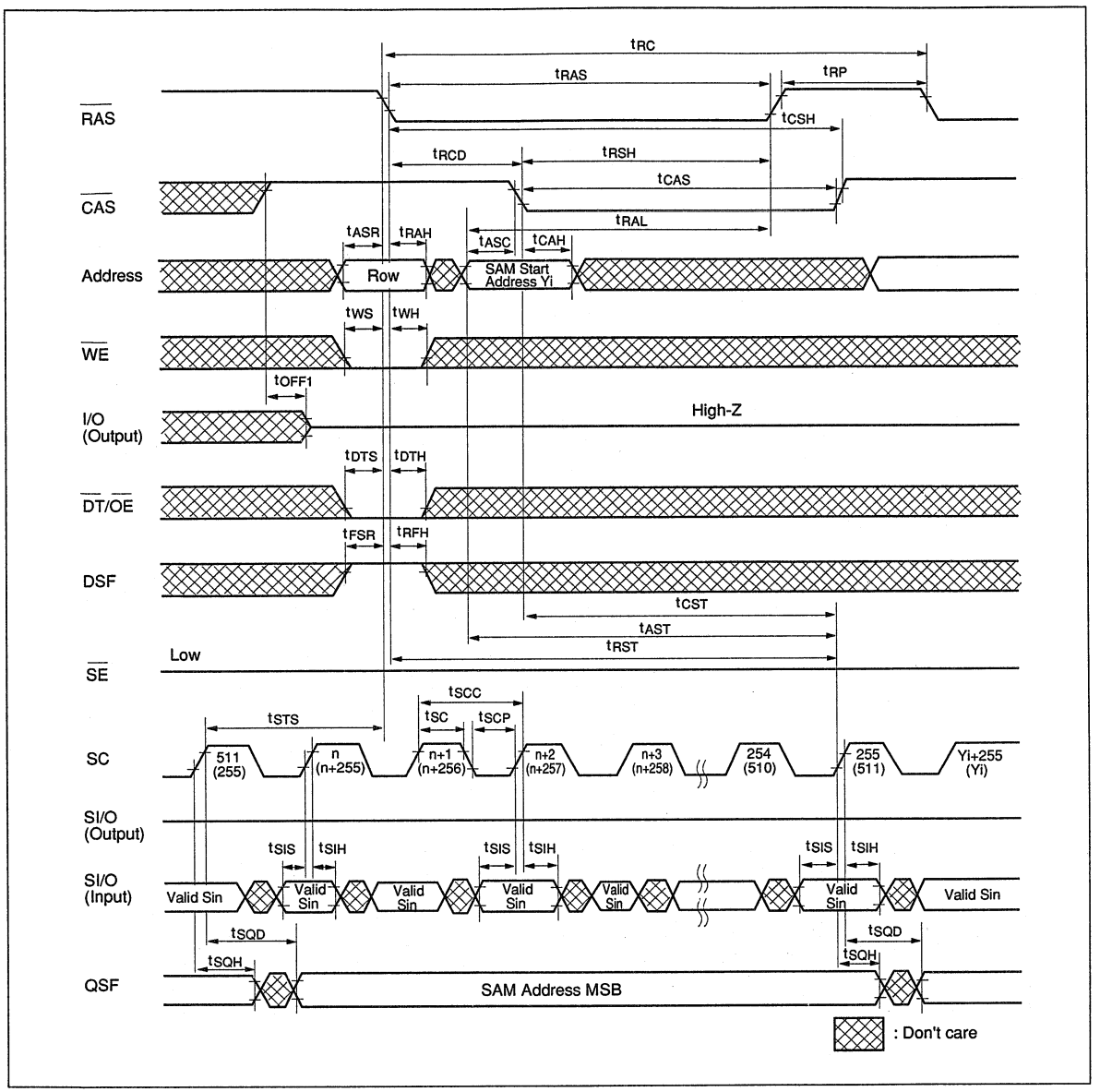


Split Read Transfer Cycle

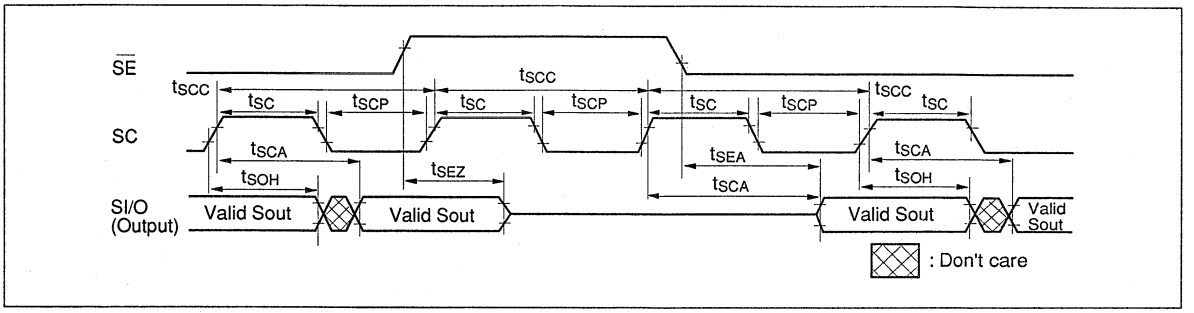


Note: 1. If the next transfer cycle after read transfer cycle is split read transfer cycle, one or more access to SC are required between read transfer cycle and split read transfer cycle.

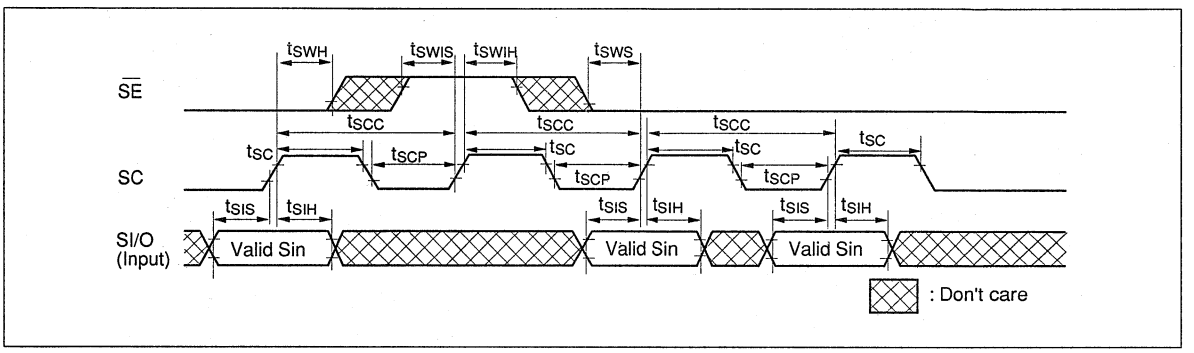
Split Write Transfer Cycle



Serial Read Cycle



Serial Write Cycle



HM538121A Series

131072-word × 8-bit Multiport CMOS Video RAM

The HM538121A is a 1-Mbit multiport video RAM equipped with a 128-kword × 8-bit dynamic RAM and a 256-word × 8-bit SAM (serial access memory). Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has write mask function.

Features

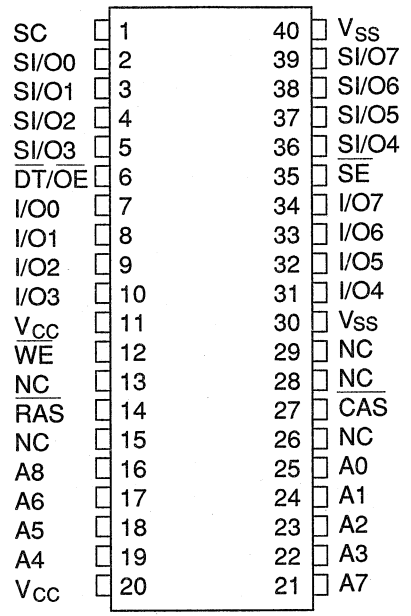
- Multiport organization
  - Asynchronous and simultaneous operation of RAM and SAM capability
    - RAM: 128 kword × 8 bit
    - SAM: 256 word × 8 bit
- Access time
  - RAM: 60 ns/70 ns/80 ns/100 ns max
  - SAM: 20 ns/22 ns/25 ns/25 ns max
- Cycle time
  - RAM: 125 ns/135 ns/150 ns/180 ns min
  - SAM: 25 ns/25 ns/30 ns/30 ns min
- Low power
  - Active RAM: 413 mW max
    SAM: 275 mW max
  - Standby 38.5 mW max
- High-speed page mode capability
- Mask write mode capability
- Bidirectional data transfer cycle between RAM and SAM capability
- Real time read transfer cycle capability
- 3 variations of refresh (8 ms/512 cycles)
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package
HM538121AJ-6	60 ns	400-mil 40-pin plastic SOJ (CP-40D)
HM538121AJ-7	70 ns	
HM538121AJ-8	80 ns	
HM538121AJ-10	100 ns	

Pin Arrangement

HM538121AJ Series

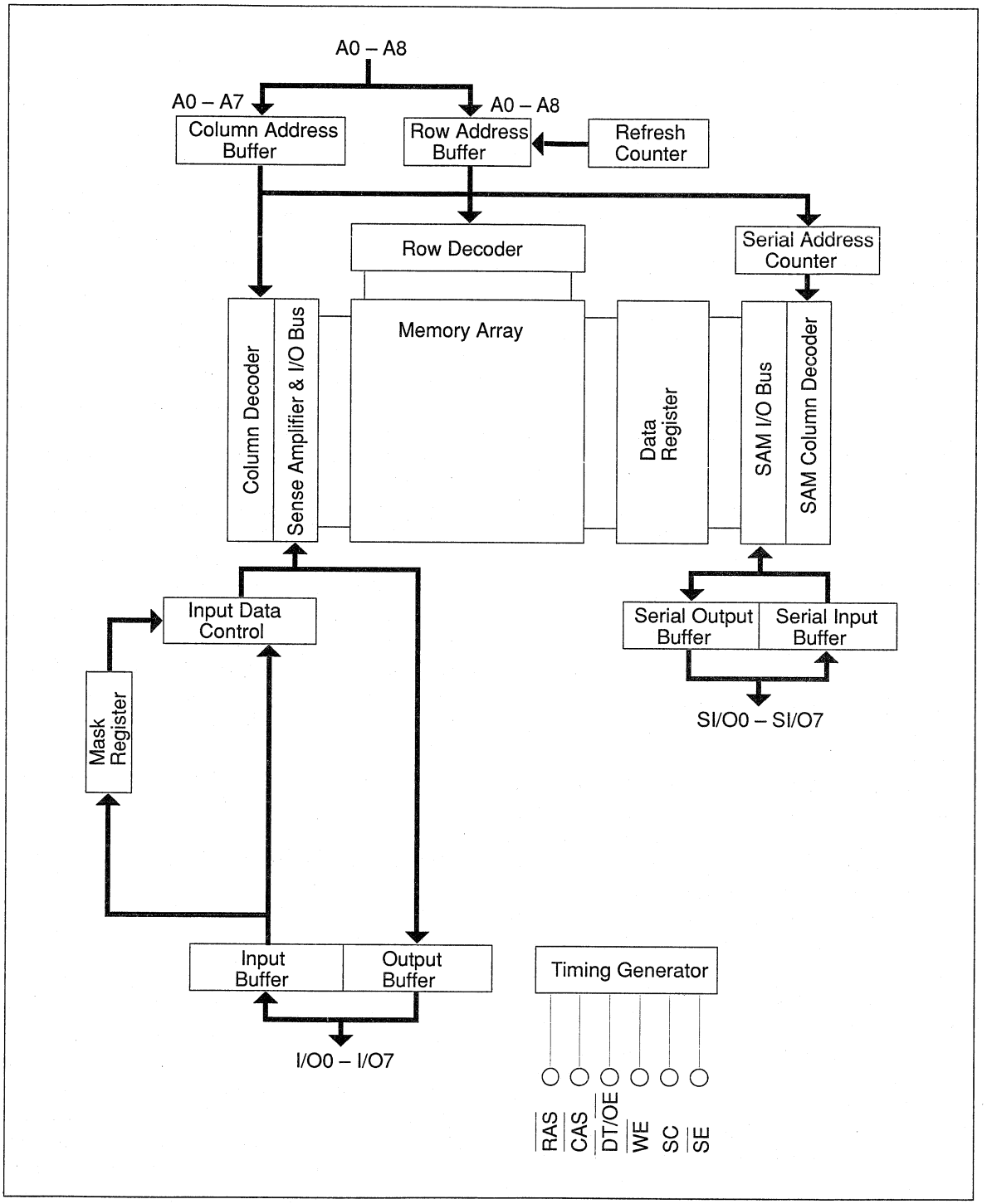


(Top View)

Pin Description

Pin name	Function
A0 - A8	Address inputs
I/O0 - I/O7	RAM port data inputs/outputs
SI/O0 - SI/O7	SAM port data inputs/outputs
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{CAS}}$	Column address strobe
$\overline{\text{WE}}$	Write enable
$\overline{\text{DT/OE}}$	Data transfer/Output enable
SC	Serial clock
$\overline{\text{SE}}$	SAM port enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



Pin Functions

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of these signals determine the operation cycle of the HM538121A.

Table 1 Operation Cycles of the HM538121A

Input Level at the Falling Edge of $\overline{RAS}$				
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	$\overline{SE}$	Operation mode
L	X	X	X	CBR refresh
H	L	L	L	Write transfer
H	L	L	H	Pseudo transfer
H	L	H	X	Read transfer
H	H	L	X	Read/mask write
H	H	H	X	Read/write

Note: X: Don't care.

$\overline{CAS}$ (input pin): Column address is fetched into chip at the falling edge of $\overline{CAS}$. $\overline{CAS}$ controls output impedance of I/O in RAM.

A0-A8 (input pins): Row address (AX0-AX8), is determined by A0-A8 level at the falling edge of $\overline{RAS}$. Column (AY0-AY7) address is determined by A0-A7 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM538121A turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O0-I/O7 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only to high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data outputs from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is fetched into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not fetched into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O0-SI/O7 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

Operation of HM538121A

RAM Read Cycle ($\overline{DT}/\overline{OE}$ high and $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data outputs through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle (Early Write, Delayed Write, Read-Modify-Write)
($\overline{DT}/\overline{OE}$ high and $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

- Normal Mode Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after driving $\overline{RAS}$ low, a write cycle is executed and I/O data is written in the selected addresses. When all 8I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.
If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes in high impedance. Data is entered at the $\overline{CAS}$ falling edge.
If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delalyed write cycle. Data is input an the $\overline{WE}$ falling. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.
If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables read/write at the same address in one cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and driving $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is retained. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode cycle, the mask data is retained during the page access.

High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high and $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle. Note that address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 256-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 µs).

Transfer Operation

The HM538121A provides the read transfer cycle, pseudo transfer cycle and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{CAS}$ high and $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)
Read transfer cycle: RAM to SAM
Write transfer cycle: SAM to RAM
(2) Determine SI/O state
Read transfer cycle: SI/O output
Pseudo transfer cycle and write transfer cycle: SI/O input
(3) Determine first SAM address to access after transferring at column address (SAM start address).
SAM start address must be determined by read transfer cycle or pseudo transfer cycle after power on, and determined for each transfer cycle.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by driving $\overline{DT}/\overline{OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address data (256 x 8-bit) determined by this cycle is transferred to SAM data register synchronously at the rising edge of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address determined by column address. In read transfer cycle, $\overline{DT}/\overline{OE}$ must be risen to transfer data from RAM to SAM.
This cycle can access SAM even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge and t_{SDH} (min) specified between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge must be satisfied. (See figure 1).When read transfer cycle is executed, SI/O becomes output state by first SAM access. Input must be set high impedance before t_{SZS} (min) of the first SAM access to avoid data contention.

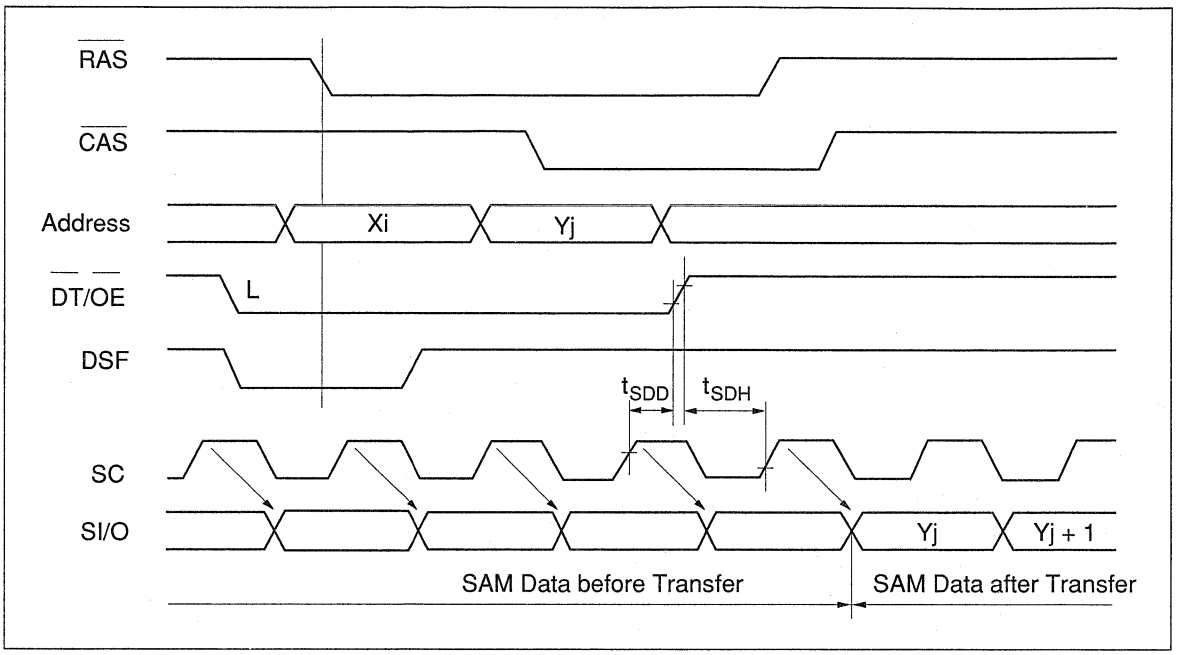


Figure 1 Real Time Read Transfer

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and $\overline{SE}$ high at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle switches SI/O to input state and set SAM start address without data transfer to RAM.

This cycle starts when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and $\overline{SE}$ high at the falling edge of $\overline{RAS}$. Data should be input to SI/O later than t_{SID} (min) after $\overline{RAS}$ becomes low to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC must not be risen.

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and $\overline{SE}$ low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address for serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC must not be risen.

Data transferred to SAM by read transfer cycle can be written to other address of RAM by write transfer cycle. However, the address to write data must be the same MSB of row address (AX8) as that of the read transfer cycle.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When $\overline{SE}$ is set high, SI/O becomes high impedance, and the internal pointer is incremented by the SC rising. After indicating the last address (address 255), the internal pointer indicates address 0 at the next access.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is fetched into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't fetched into data register. Internal pointer is incremented by the SC rising, so $\overline{SE}$ high can be used as mask

data for SAM. After indicating the last address (address 255), the internal pointer indicates address 0 at the next access.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is executed by accessing all 512 row addresses within 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required when all row addresses are accessed within 8 ms.

(1) $\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is executed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high after inputting the row address (= refresh address) from external circuits. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ must be high at the falling edge of $\overline{RAS}$.

(2) CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate.

(3) Hidden Refresh Cycle: Hidden refresh cycle executes CBR refresh with the data output by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register and selector), organized as fully static circuitry, require no refresh.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage*1	V_T	–1.0 to +7.0	V
Power supply voltage*1	V_{CC}	–0.5 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Note: 1. Relative to V_{SS}

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage*1	V_{CC}	4.5	5.0	5.5	V
Input high voltage*1	V_{IH}	2.4	—	6.5	V
Input low voltage*1	V_{IL}	–0.5*2	—	0.8	V

Notes: 1. All voltages referenced to V_{SS}
2. –3.0 V for pulse width ≤ 10 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM538121A										
		-6		-7		-8		-10			Test conditions	
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	RAM port	SAM port
Operating current	I_{CC1}	—	75	—	70	—	60	—	55	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC7}	—	125	—	120	—	100	—	95	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
standby current	I_{CC2}	—	7	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC8}	—	50	—	50	—	40	—	40	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
$\overline{RAS}$-only refresh current	I_{CC3}	—	75	—	70	—	60	—	55	mA	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH} t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC9}	—	125	—	120	—	100	—	95	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
Page mode current	I_{CC4}	—	80	—	80	—	70	—	65	mA	$\overline{CAS}$ cycling $\overline{RAS}$ = V_{IL} t_{PC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10}	—	130	—	130	—	110	—	105	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	—	50	—	45	—	40	—	35	mA	$\overline{RAS}$ cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC11}	—	100	—	95	—	80	—	75	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
Data transfer current	I_{CC6}	—	80	—	75	—	65	—	60	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC12}	—	130	—	125	—	105	—	100	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	–10	10	µA		
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	–10	10	µA		
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V	I_{OH} = –2 mA	
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V	I_{OL} = 4.2 mA	

Note: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once while $\overline{RAS}$ is low and $\overline{CAS}$ is high.

Capacitance

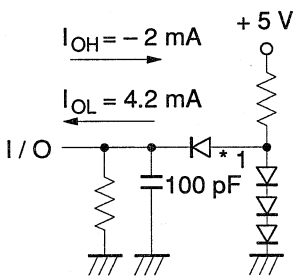
($Ta = 25°C$, $V_{CC} = 5$ V, f = 1 MHz, Bias: Clock, I/O = V_{CC}, address = V_{SS})

Item	Symbol	Min	Typ	Max	Unit
Address	CI1	—	—	5	pF
Clock	CI2	—	—	5	pF
I/O, SI/O	CI/O	—	—	7	pF

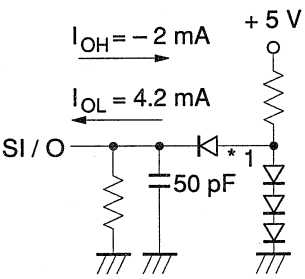
AC Characteristics ($Ta = 0$ to $+70°C$, $V_{CC} = 5$ V ± 10%, $V_{SS} = 0$ V)*1, *16

Test Conditions

- Input rise and fall time: 5 ns
- Output load: See figures
- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V



Output Load (A)



Output Load (B)

Note: 1. Including scope & jig.

Common Parameter

		HM538121A									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
Random read or write cycle time	t_{RC}	125	—	135	—	150	—	180	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	55	—	55	—	60	—	70	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	—	20	—	20	—	25	—	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	20	60	20	75	ns	2
$\overline{RAS}$ hold time referenced to $\overline{CAS}$	t_{RSH}	20	—	20	—	20	—	25	—	ns	
$\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Transition time (rise to fall)	t_T	3	50	3	50	3	50	3	50	ns	3
Refresh period	t_{REF}	—	8	—	8	—	8	—	8	ns	
$\overline{DT}$ to $\overline{RAS}$ setup time	t_{DTS}	0	—	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ hold time	t_{DTH}	10	—	10	—	10	—	10	—	ns	
Data-in to $\overline{CAS}$ delay time	t_{DZC}	0	—	0	—	0	—	0	—	ns	4
Data-in to $\overline{OE}$ delay time	t_{DZO}	0	—	0	—	0	—	0	—	ns	4
Output buffer turn-off delay referenced to $\overline{CAS}$	t_{OFF1}	—	20	—	20	—	20	—	20	ns	5
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	—	20	—	20	—	20	—	20	ns	5

Read Cycle (RAM), Page Mode Read Cycle

Item	Symbol	HM538121A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	35	—	40	—	45	ns	7, 9
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	0	—	ns	10
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	10
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	2
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	35	—	40	—	45	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	35	—	35	—	40	—	45	—	ns	
Page mode cycle time	t_{PC}	45	—	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	10	—	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	—	40	—	45	—	50	ns	
Page mode $\overline{RAS}$ pulse width	t_{RASP}	60	100000	70	100000	80	100000	100	100000	ns	

Write Cycle (RAM), Page Mode Write Cycle

		HM538121A									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
Write command setup time	t_{WCS}	0	—	0	—	0	—	0	—	ns	11
Write command hold time	t_{WCH}	15	—	15	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	15	—	15	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	15	—	15	—	15	—	15	—	ns	12
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	10	—	10	—	10	—	10	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	10	—	10	—	10	—	10	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	20	—	20	—	20	—	20	—	ns	
Page mode cycle time	t_{PC}	45	—	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ to data-in delay time	t_{CDD}	20	—	20	—	20	—	20	—	ns	13
Page mode $\overline{RAS}$ pulse width	t_{RASP}	60	100000	70	100000	80	100000	100	100000	ns	

Read-Modify-Write Cycle

Item	Symbol	HM538121A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
Read-modify-write cycle time	t_{RWC}	175	—	185	—	200	—	230	—	ns	
$\overline{RAS}$ pulse width (read-modify-write cycle)	t_{RWS}	110	10000	120	10000	130	10000	150	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	45	—	45	—	45	—	50	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	60	—	60	—	65	—	70	—	ns	14
$\overline{OE}$ to data-in delay time	t_{ODD}	20	—	20	—	20	—	20	—	ns	12
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	35	—	40	—	45	ns	7, 9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	20	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	15	—	15	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	15	—	15	—	15	—	15	—	ns	12
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	20	—	20	—	20	—	20	—	ns	

Refresh Cycle

Item	Symbol	HM538121A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

Read Transfer Cycle

Item	Symbol	HM538121A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
$\overline{DT}$ hold time referenced to $\overline{RAS}$	t_{RDH}	50	10000	60	10000	65	10000	80	10000	ns	
$\overline{DT}$ hold time referenced to $\overline{CAS}$	t_{CDH}	20	—	20	—	20	—	25	—	ns	
$\overline{DT}$ hold time referenced to column address	t_{ADH}	25	—	25	—	30	—	30	—	ns	
$\overline{DT}$ precharge time	t_{DTP}	20	—	20	—	20	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ delay time	t_{DRD}	65	—	65	—	70	—	80	—	ns	
SC to $\overline{RAS}$ setup time	t_{SRS}	25	—	25	—	30	—	30	—	ns	
1st SC to $\overline{RAS}$ hold time	t_{SRH}	60	—	70	—	80	—	100	—	ns	
1st SC to $\overline{CAS}$ hold time	t_{SCH}	25	—	25	—	25	—	25	—	ns	
1st SC to column address hold time	t_{SAH}	40	—	40	—	45	—	50	—	ns	
Last SC to $\overline{DT}$ delay time	t_{SDD}	5	—	5	—	5	—	5	—	ns	
1st SC to $\overline{DT}$ hold time	t_{SDH}	10	—	10	—	15	—	15	—	ns	
Serial data-in to 1st SC delay time	t_{SZS}	0	—	0	—	0	—	0	—	ns	
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	10	—	ns	

Read Transfer Cycle (cont)

		HM538121A									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
SC access time	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	35	—	40	—	45	—	ns	
$\overline{DT}$ high hold time to $\overline{RAS}$ precharge time	t_{DTHH}	10	—	10	—	10	—	10	—	ns	

Pseudo Transfer Cycle, Write Transfer Cycle

		HM538121A									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
$\overline{SE}$ setup time referenced to $\overline{RAS}$	t_{ES}	0	—	0	—	0	—	0	—	ns	
$\overline{SE}$ hold time referenced to $\overline{RAS}$	t_{EH}	10	—	10	—	10	—	10	—	ns	
SC setup time referenced to $\overline{RAS}$	t_{SRS}	25	—	25	—	30	—	30	—	ns	
$\overline{RAS}$ to SC delay time	t_{SRD}	20	—	20	—	25	—	25	—	ns	
Serial output buffer turn-off time referenced to $\overline{RAS}$	t_{SRZ}	10	40	10	40	10	45	10	50	ns	
$\overline{RAS}$ to serial data-in delay time	t_{SID}	40	—	40	—	45	—	50	—	ns	
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
$\overline{SE}$ access time	t_{SEA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	

Pseudo Transfer Cycle, Write Transfer Cycle (cont)

		HM538121A									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
Serial write enable setup time	t_{SWS}	5	—	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	

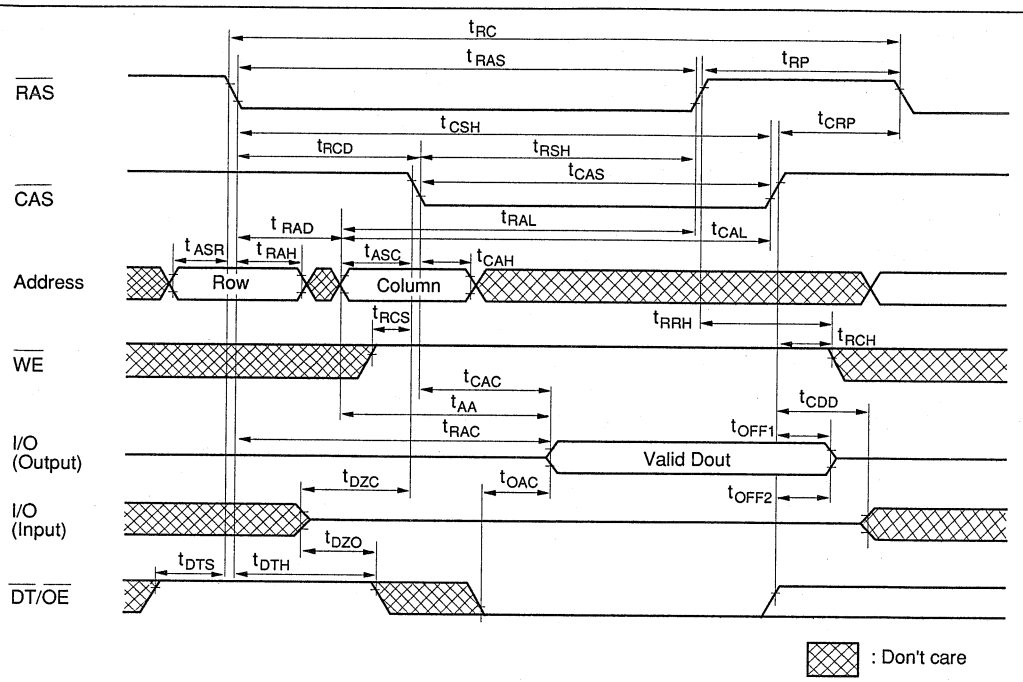
Serial Read Cycle, Serial Write Cycle

		HM538121A									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Access time from SC	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
Access time from $\overline{SE}$	t_{SEA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial output buffer turn-off time referenced to $\overline{SE}$	t_{SEZ}	—	20	—	20	—	20	—	20	ns	5
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	
Serial write enable setup time	t_{SWS}	5	—	5	—	5	—	5	—	ns	
Serial write enable hold time	t_{SWH}	15	—	15	—	15	—	15	—	ns	
Serial write disable setup time	t_{SWIS}	5	—	5	—	5	—	5	—	ns	
Serial write disable hold time	t_{SWIH}	15	—	15	—	15	—	15	—	ns	

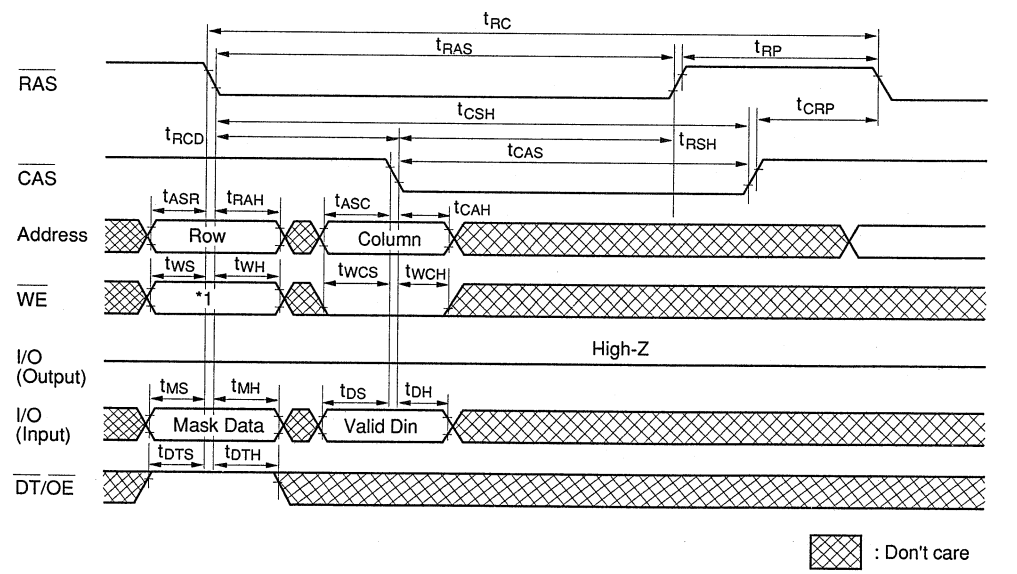
Notes:
1. AC measurements assume t_T = 5 ns.
2. When $t_{RCD} > t_{RCD}$ (max) or $t_{RAD} > t_{RAD}$ (max), access time is specified by t_{CAC} or t_{AA}.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition time t_T is measured between V_{IH} and V_{IL}.
4. Data input must be floating before output buffer is turned on. In read cycle, read-modify-write cycle and delayed write cycle, either t_{DZC} (min) or t_{DZO} (min) must be satisfied.
5. t_{OFF1} (max), t_{OFF2} (max) and t_{SEZ} (max) are defined as the time at which the output acheives the open circuit condition (V_{OH} − 100 mV, V_{OL} + 100 mV).
6. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
8. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
9. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
10. If either t_{RCH} of t_{RRH} is satisfied, operation is guaranteed.
11. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
12. These parameters are specified by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
13. Either t_{CDD} (min) or t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{CAS}$ or $\overline{OE}$ prior to applying data to the device when output buffer is on.
14. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min) in read-modify-write cycle, the data of the selected address outputs to an I/O pin and input data is written into the selected address. t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{OE}$ prior to applying data to the device.
15. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
16. After power-up, pause for 100 µs or more and execute at least 8 initialization cycle (normal memory cycle or refresh cycle), then start operation.

Timing Waveforms

Read Cycle

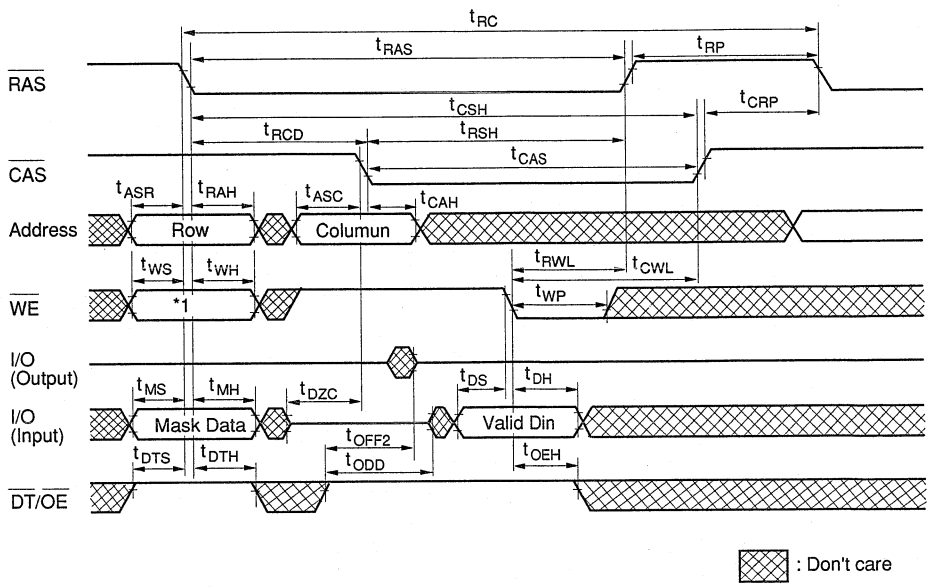


Early Write Cycle



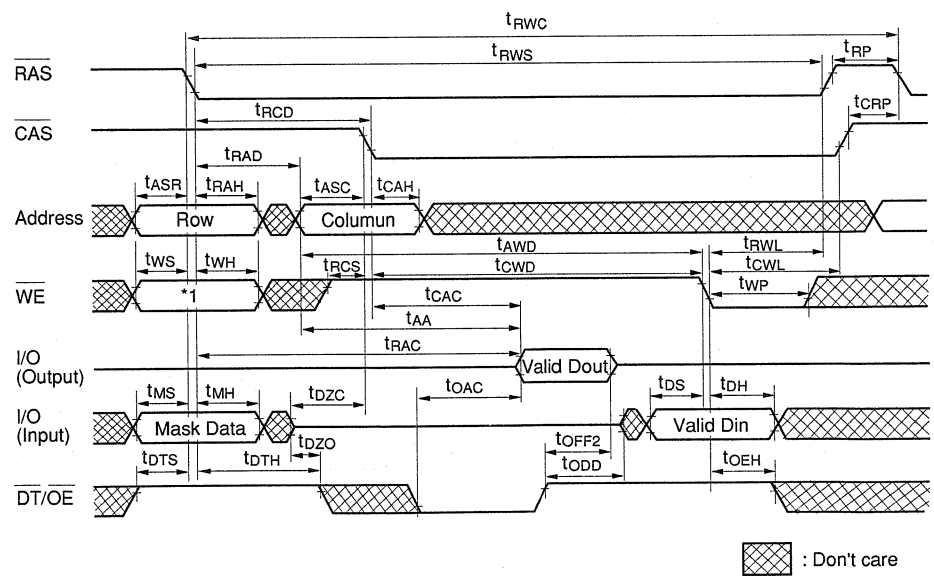
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Delayed Write Cycle



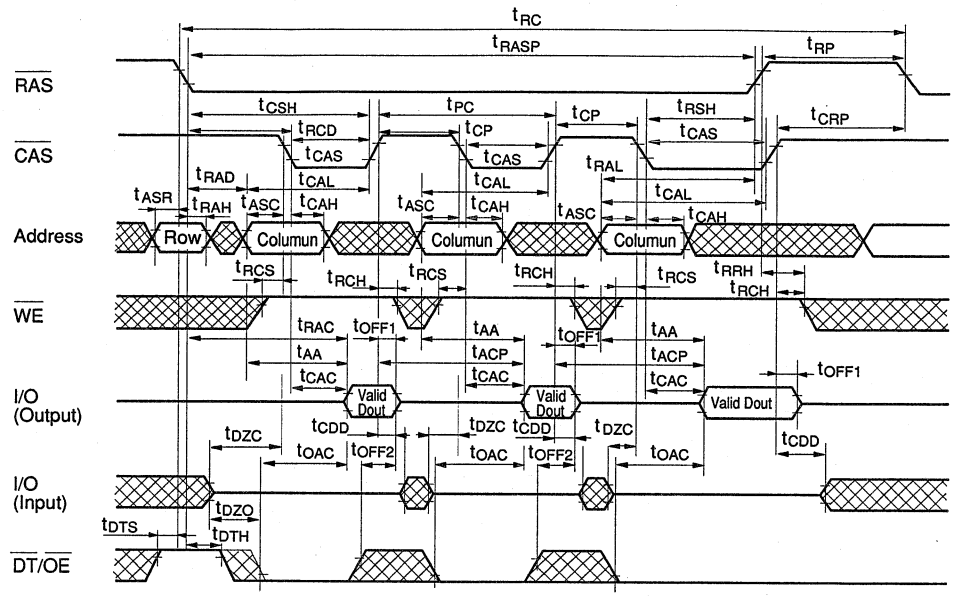
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Read-Modify-Write Cycle

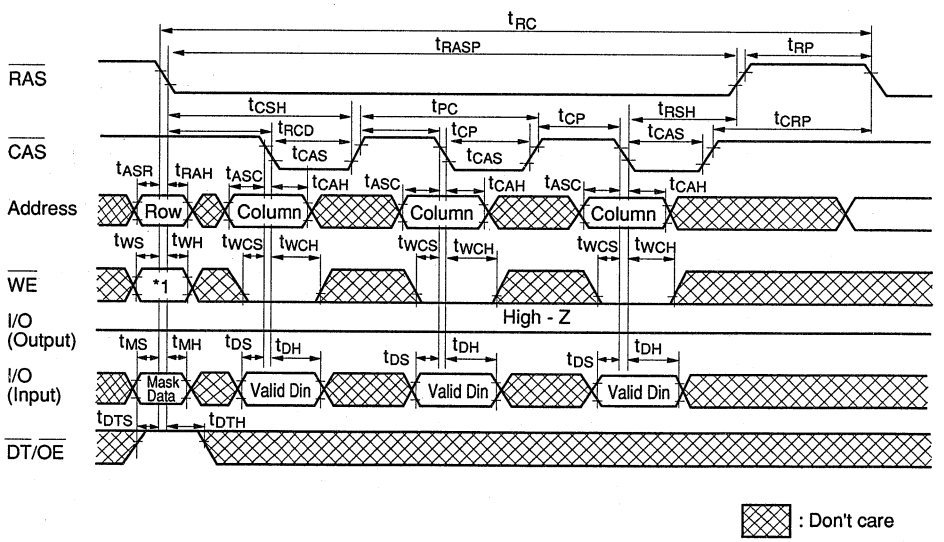


Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Page Mode Read Cycle

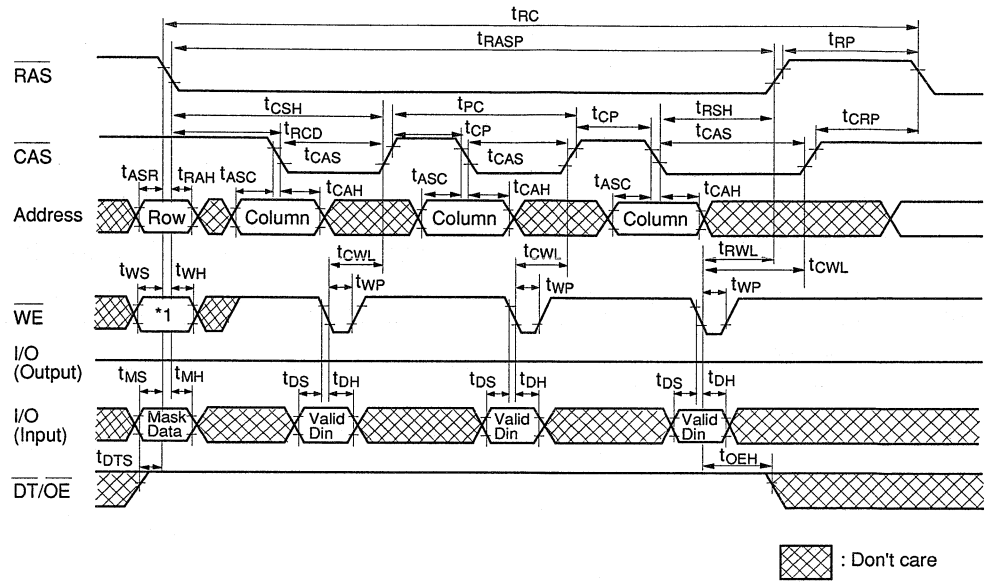


Page Mode Write Cycle (Early Write)



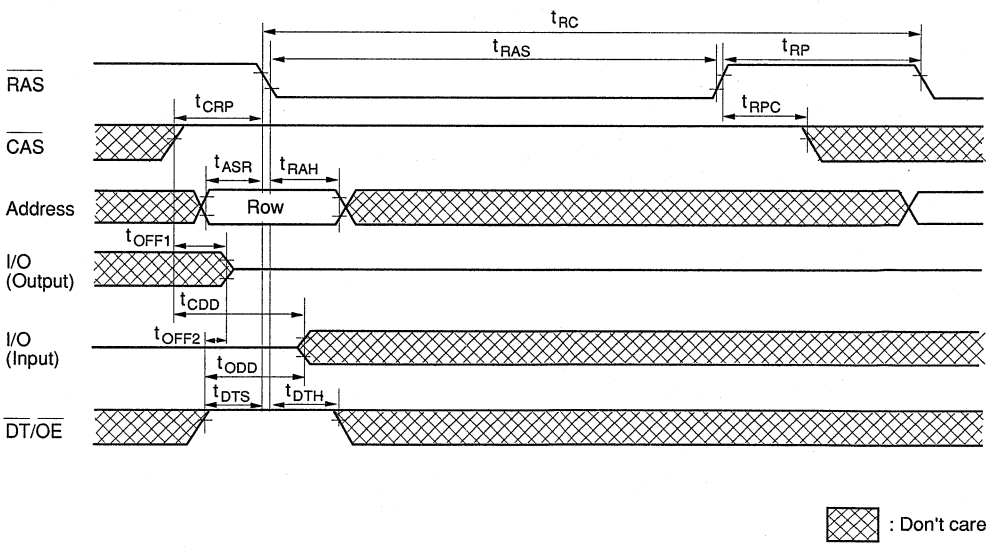
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Page Mode Write Cycle (Delayed Write)

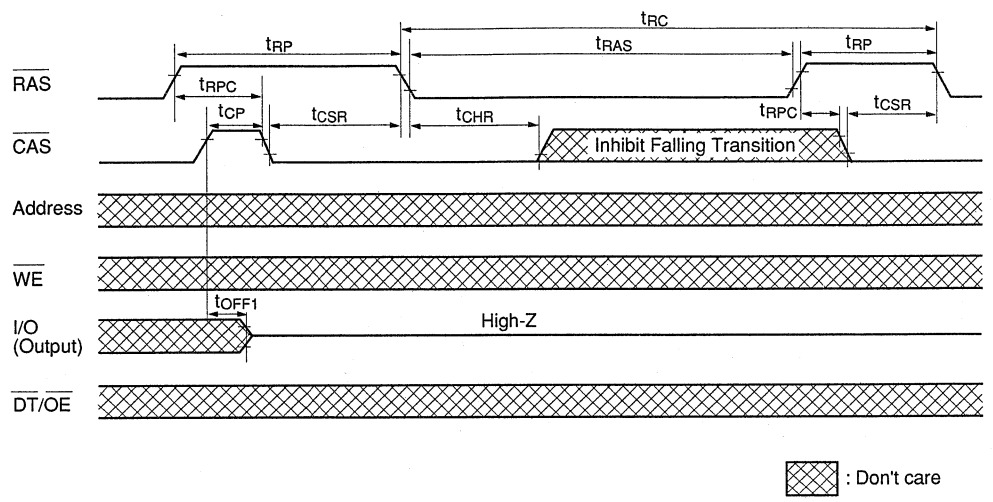


Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

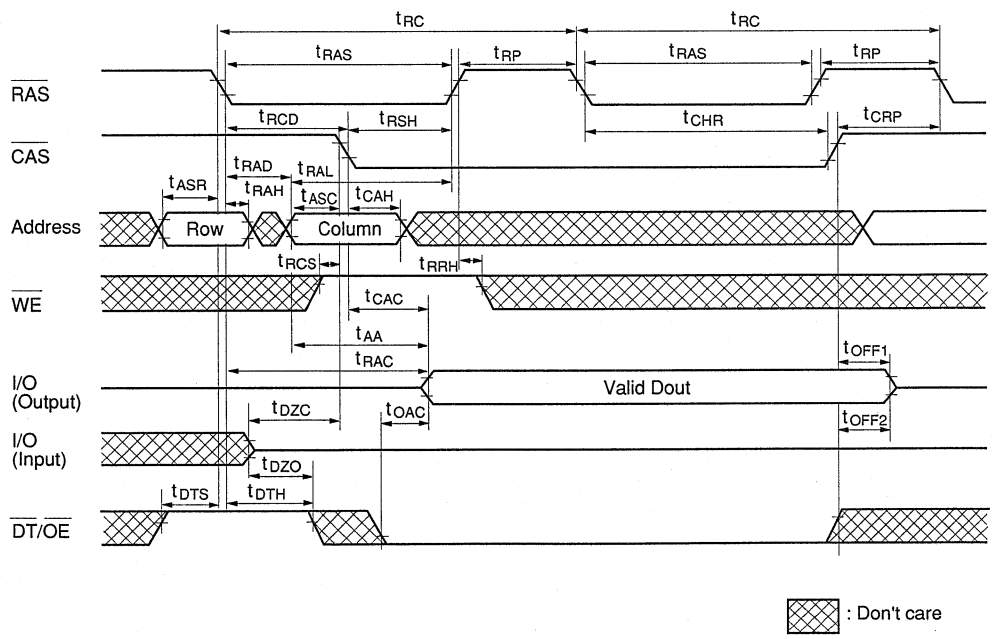
$\overline{RAS}$-Only Refresh Cycle



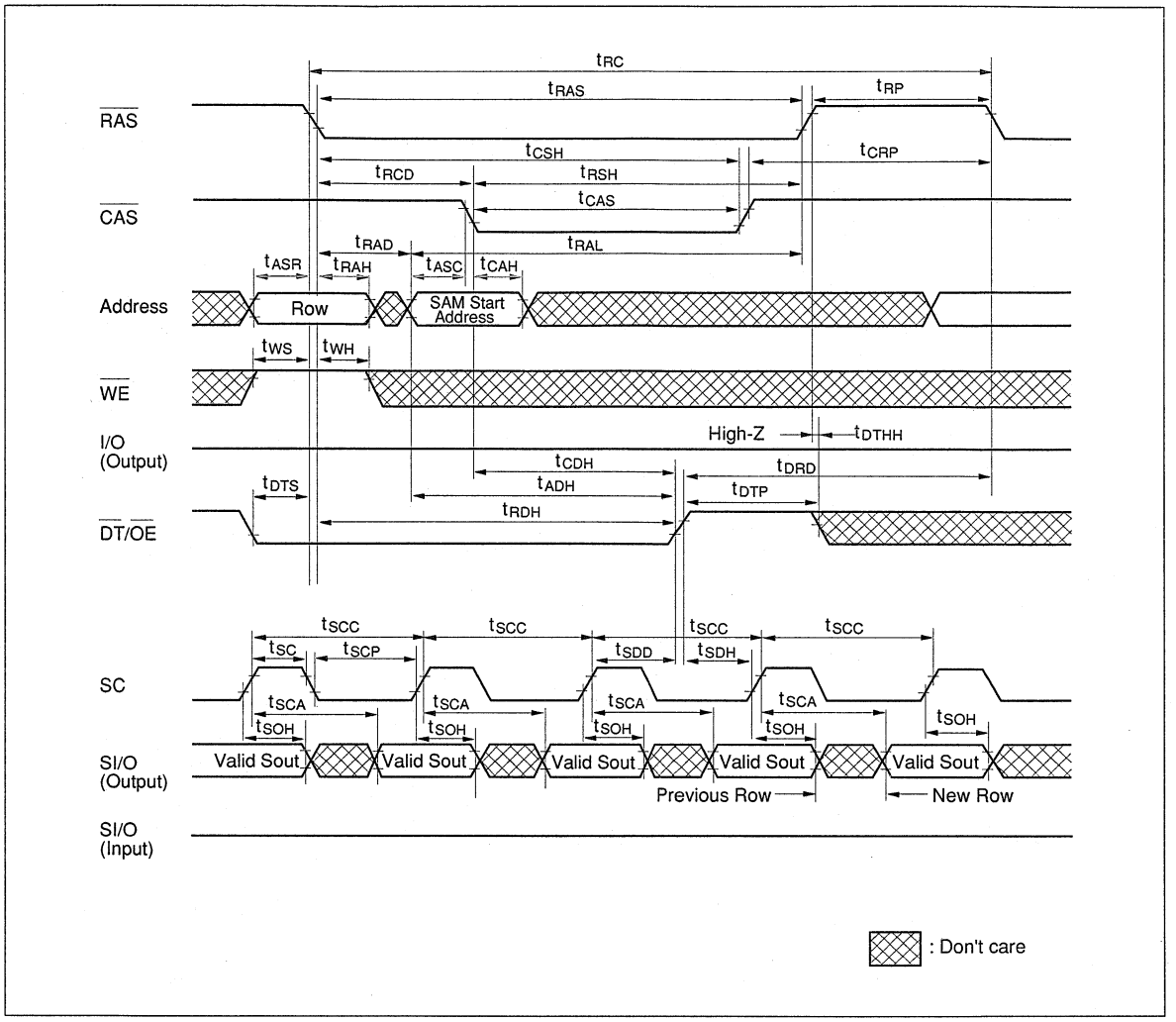
CAS-Before-RAS Refresh Cycle



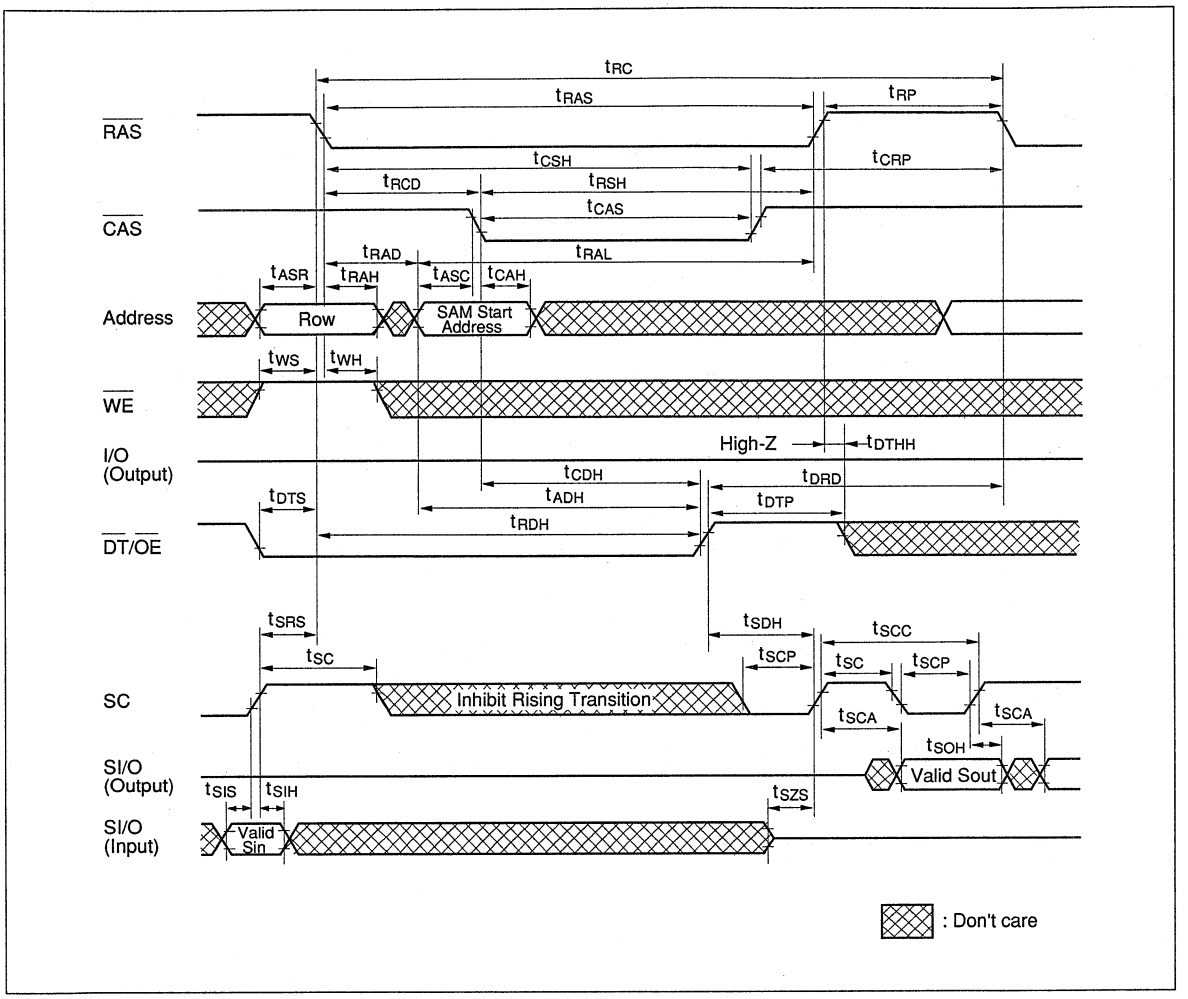
Hidden Refresh Cycle



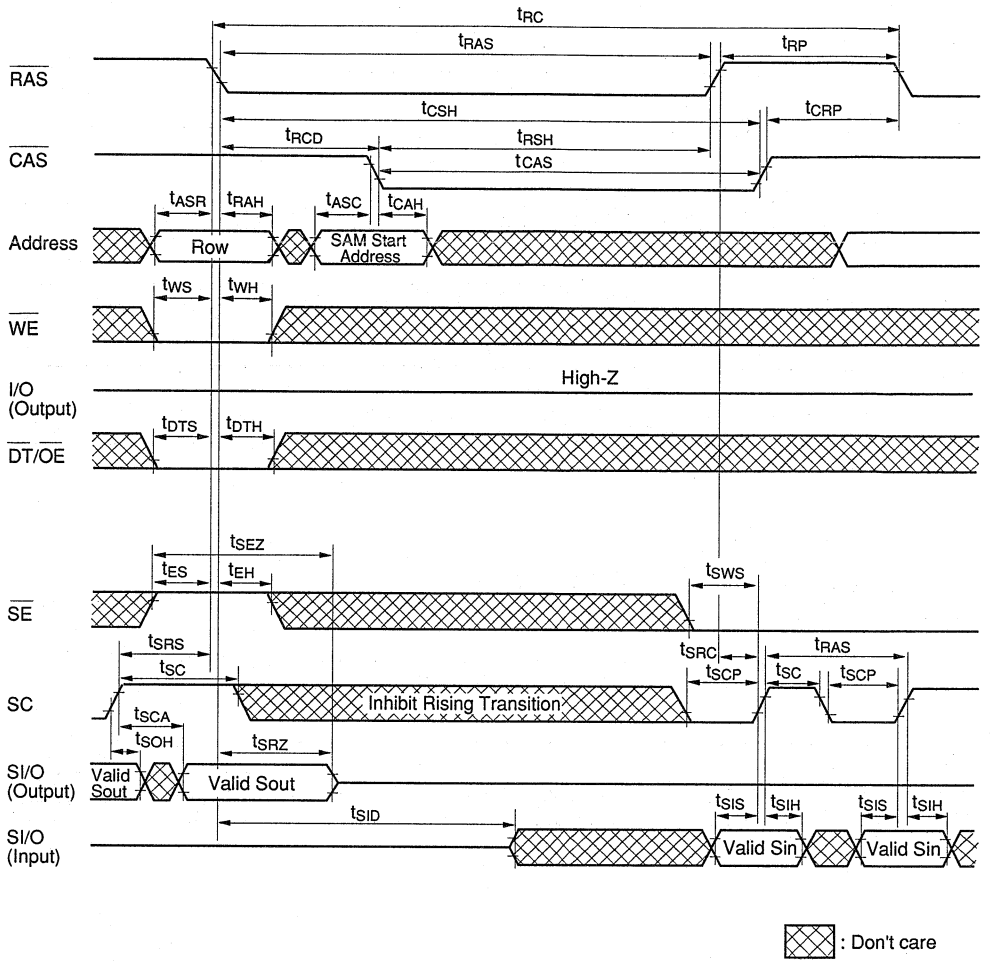
Read Transfer Cycle (1)



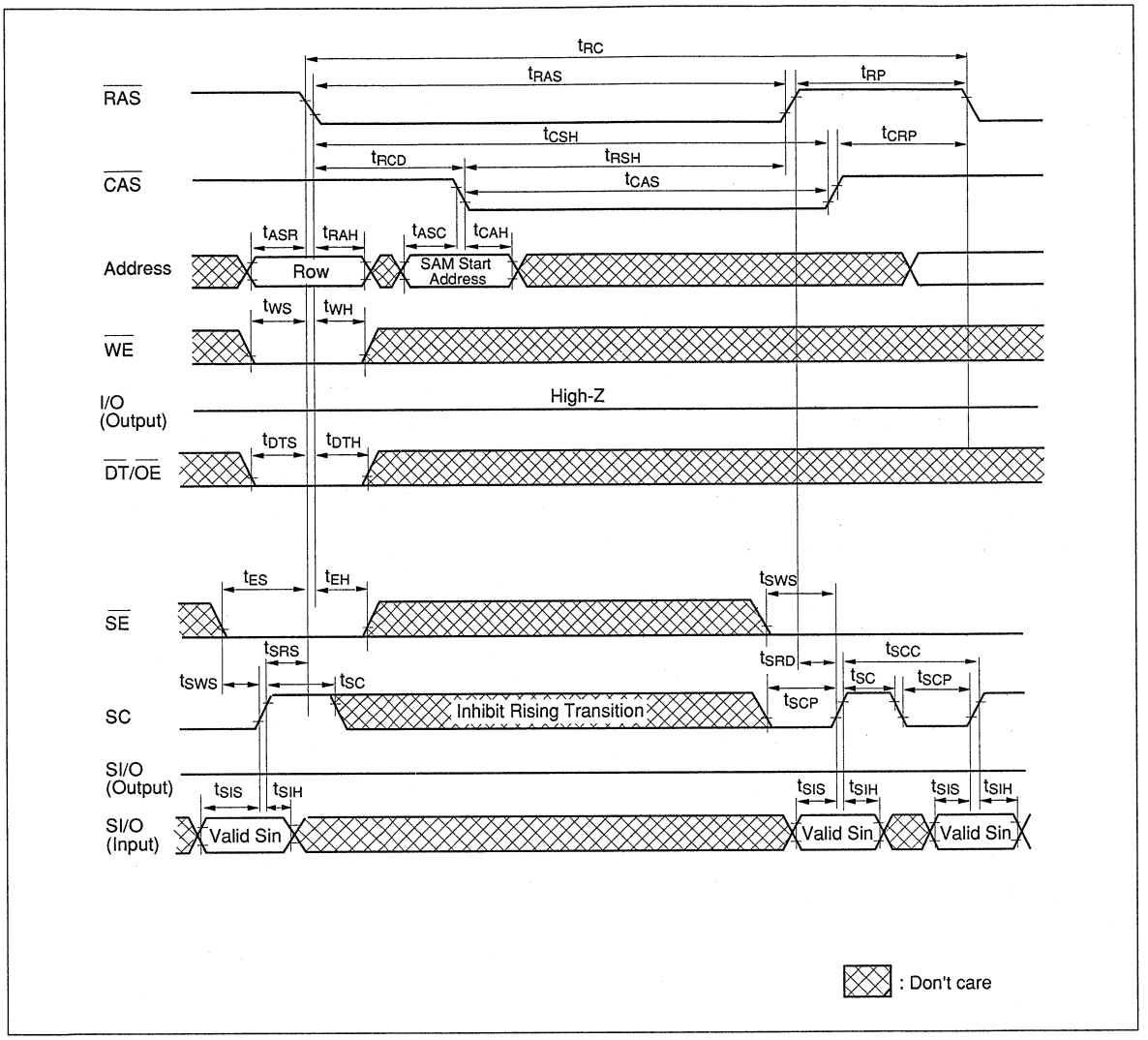
Read Transfer Cycle (2)



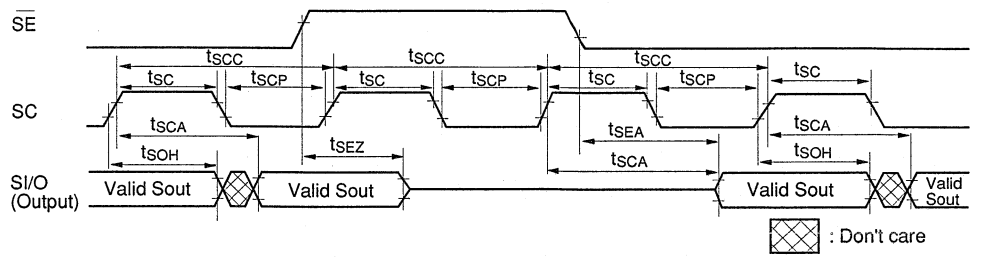
Pseudo Transfer Cycle



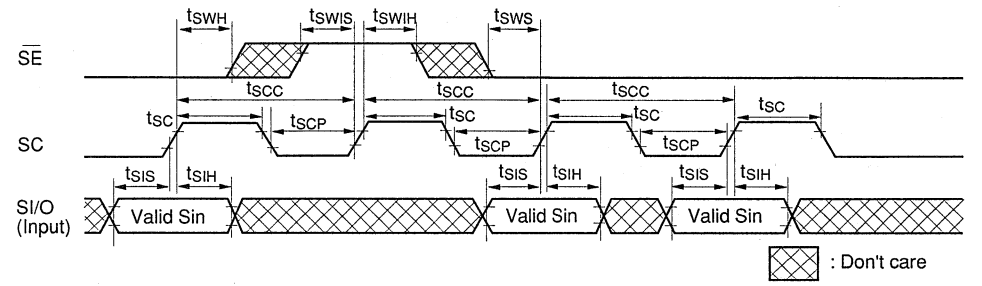
Write Transfer Cycle



Serial Read Cycle



Serial Write Cycle



HM538123A Series

131072-word × 8-bit Multiport CMOS Video RAM

The HM538123A is a 1-Mbit multiport video RAM equipped with a 128-kword × 8-bit dynamic RAM and a 256-word × 8-bit SAM (serial access memory). Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM. In addition, it has two modes to realize fast writing in RAM. Block write and flash write modes clear the data of 4-word × 8-bit and the data of one row (256-word × 8-bit) respectively in one cycle of RAM. And the HM538123A makes split transfer cycle possible by dividing SAM into two split buffers equipped with 128-word × 8-bit each. This cycle can transfer data to SAM which is not active, and enables a continuous serial access.

Features

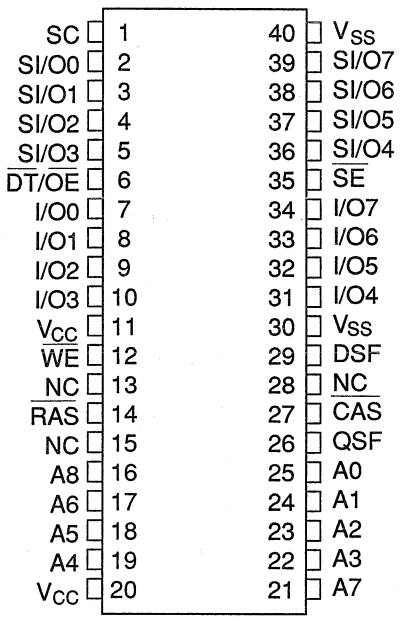
- Multiport organization
  - Asynchronous and simultaneous operation of RAM and SAM capability
    - RAM : 128 kword × 8 bit and
    - SAM : 256 word × 8 bit
- Access time
  - RAM : 60 ns/70 ns/80 ns/100 ns max
  - SAM : 20 ns/22 ns/25 ns/25 ns max
- Cycle time
  - RAM : 125 ns/135 ns/150 ns/180 ns min
  - SAM : 25 ns/25 ns/30 ns/30 ns min
- Low power
  - Active RAM : 413 mW max
  - SAM : 275 mW max
  - Standby 38.5 mW max
- High-speed page mode capability
- Mask write mode capability
- Bidirectional data transfer cycle between RAM and SAM capability
- Split transfer cycle capability
- Block write mode capability
- Flash write mode capability
- 3 variations of refresh (8 ms/512 cycles)
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package
HM538123AJ-6	60 ns	400-mil 40-pin plastic SOJ (CP-40D)
HM538123AJ-7	70 ns	
HM538123AJ-8	80 ns	
HM538123AJ-10	100 ns	

Pin Arrangement

HM538123AJ Series

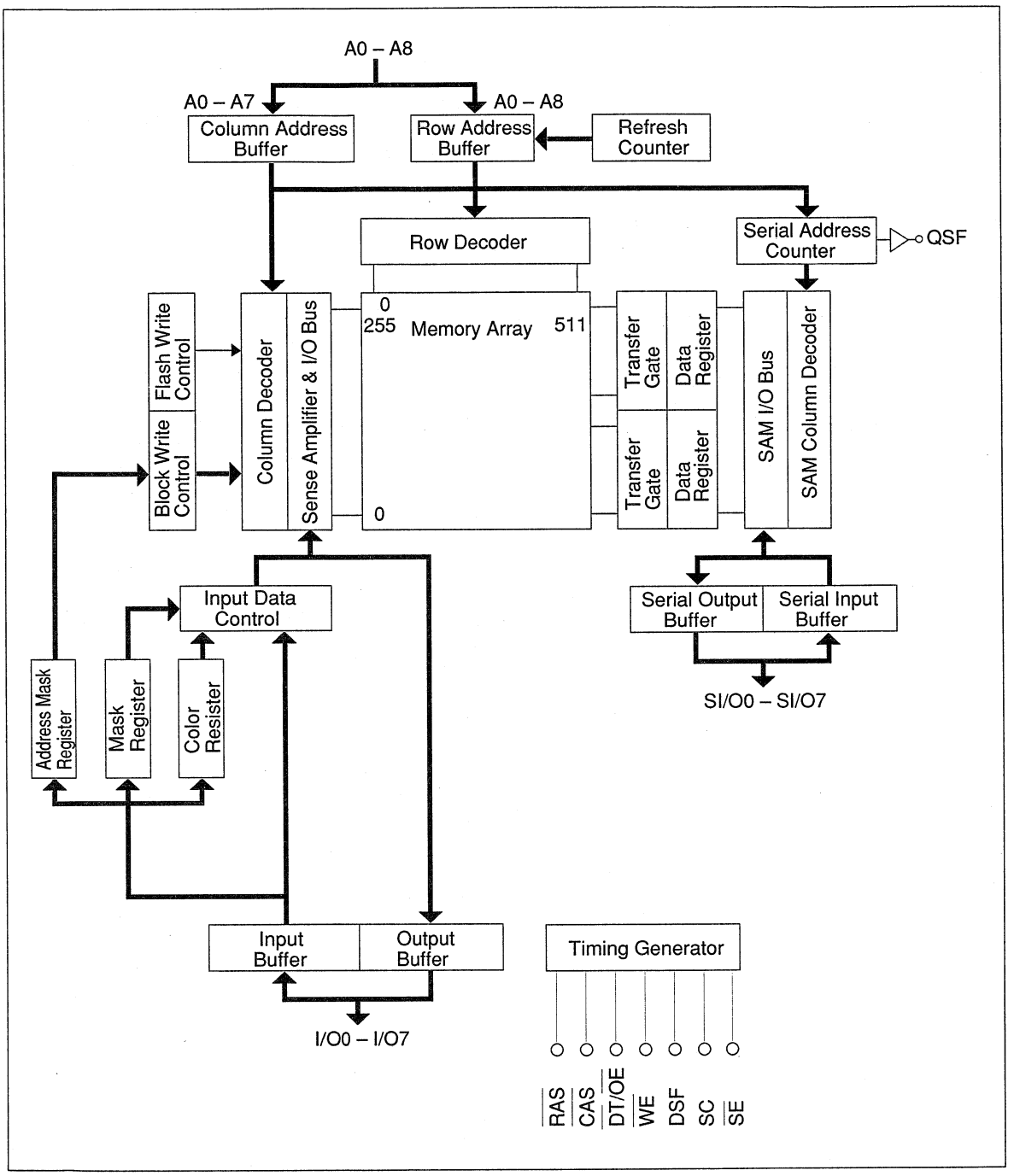


(Top View)

Pin Description

Pin name	Function
A0-A8	Address inputs
I/O0-I/O7	RAM port data inputs/outputs
SI/O0-SI/O7	SAM port data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{DT/OE}$	Data transfer/Output enable
SC	Serial clock
$\overline{SE}$	SAM port enable
DSF	Special function input flag
QSF	Special function output flag
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



Pin Functions

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level.

Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of these signals determine the operation cycle of the HM538123A.

Table 1 Operation Cycles of the HM538123A

Input Level at the falling edge of $\overline{RAS}$						
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WE}$	$\overline{SE}$	DSF	DSF at the falling edge of $\overline{CAS}$	Operation Mode
L	X	X	X	X	—	CBR refresh
H	L	L	L	L	X	Write transfer
H	L	L	H	L	X	Pseudo transfer
H	L	L	X	H	X	Split write transfer
H	L	H	X	L	X	Read transfer
H	L	H	X	H	X	Split read transfer
H	H	L	X	L	L	Read/mask write
H	H	L	X	L	H	Mask block write
H	H	L	X	H	X	Flash write
H	H	H	X	L	L	Read/write
H	H	H	X	L	H	Block write
H	H	H	X	H	X	Color register read/write

Note: X; Don't care.

$\overline{CAS}$ (input pin): Column address and DSF signal are fetched into chip at the falling edge of $\overline{CAS}$, which determines the operation mode of HM538123A. $\overline{CAS}$ controls output impedance of I/O in RAM.

A0-A8 (input pins): Row address (AX0-AX8) is determined by A0-A8 level at the falling edge of $\overline{RAS}$. Column address (AY0-AY7) is determined by A0-A7 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM538123A turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O0-I/O7 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only to high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM. In block write cycle, they function as address mask data at the falling edge of $\overline{CAS}$.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data outputs from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is fetched into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not fetched into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O0-SI/O7 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

DSF (input pin): DSF is a special function data input flag pin. It is set to high at the falling edge of $\overline{RAS}$ when new functions such as color register read/write, split transfer, and flash write, are used. DSF is set to high at the falling edge of $\overline{CAS}$ when block write is executed.

QSF (output pin): QSF outputs data of address A7 in SAM. QSF is switched from low to high by accessing address 127 in SAM and from high to low by accessing 255 address in SAM.

Operation of HM538123A

RAM Read Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF low at the falling edge of $\overline{RAS}$, DSF low at the falling edge of $\overline{CAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data outputs through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle (Early Write, Delayed Write, Read-Modify-Write)
($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF low at the falling edge of $\overline{RAS}$, DSF low at the falling edge of $\overline{CAS}$)

• Normal Mode Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)
When $\overline{CAS}$ and $\overline{WE}$ are set low after driving $\overline{RAS}$ low, a write cycle is executed and I/O data is written in the selected addresses. When all 8 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes in high impedance. Data is entered at the $\overline{CAS}$ falling edge.

If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables read/write at the same address in one cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and driving $\overline{OE}$ high.

• Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is retained. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode, the mask data is retained during the page access.

High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF low at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle. In this cycle, read, write, and block write cycles can be mixed. Note that address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 256-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 µs).

Color Register Set/Read Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high, $\overline{WE}$ high and DSF high at the falling edge of $\overline{RAS}$)

In color register set cycle, color data is set to the internal color register used in flash write cycle or block write cycle. 8 bits of internal color register are provided at each I/O. This register is composed of static circuits, so once it is set, it retains the data until reset. Color register set cycle is just as same as the usual write cycle except that DSF is set high at the falling edge of $\overline{RAS}$, and read, early write and delayed write cycle can be executed. In this cycle, HM538123A refreshs the row address fetched at the falling edge of $\overline{RAS}$.

Flash Write Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high, $\overline{WE}$ low and DSF high at the falling edge of $\overline{RAS}$)

In a flash write cycle, a row of data (256-word x 8-bit) is cleared to 0 or 1 at each I/O according to the data of color register mentioned before. It is also necessary to mask I/O in this cycle. When $\overline{CAS}$ and $\overline{DT}/\overline{OE}$ is set high, $\overline{WE}$ is low, and DSF is high at the falling edge of $\overline{RAS}$, this cycle starts. Then, the row address to clear is given to row address and mask data is given to I/O. Mask data is as same as that of a RAM write cycle. High I/O is cleared, low I/O is not cleared and the internal data is retained. Cycle time is the same as those of RAM read/write cycles, so all bits can be cleared in 1/256 of the usual cycle time. (See figure 1.)

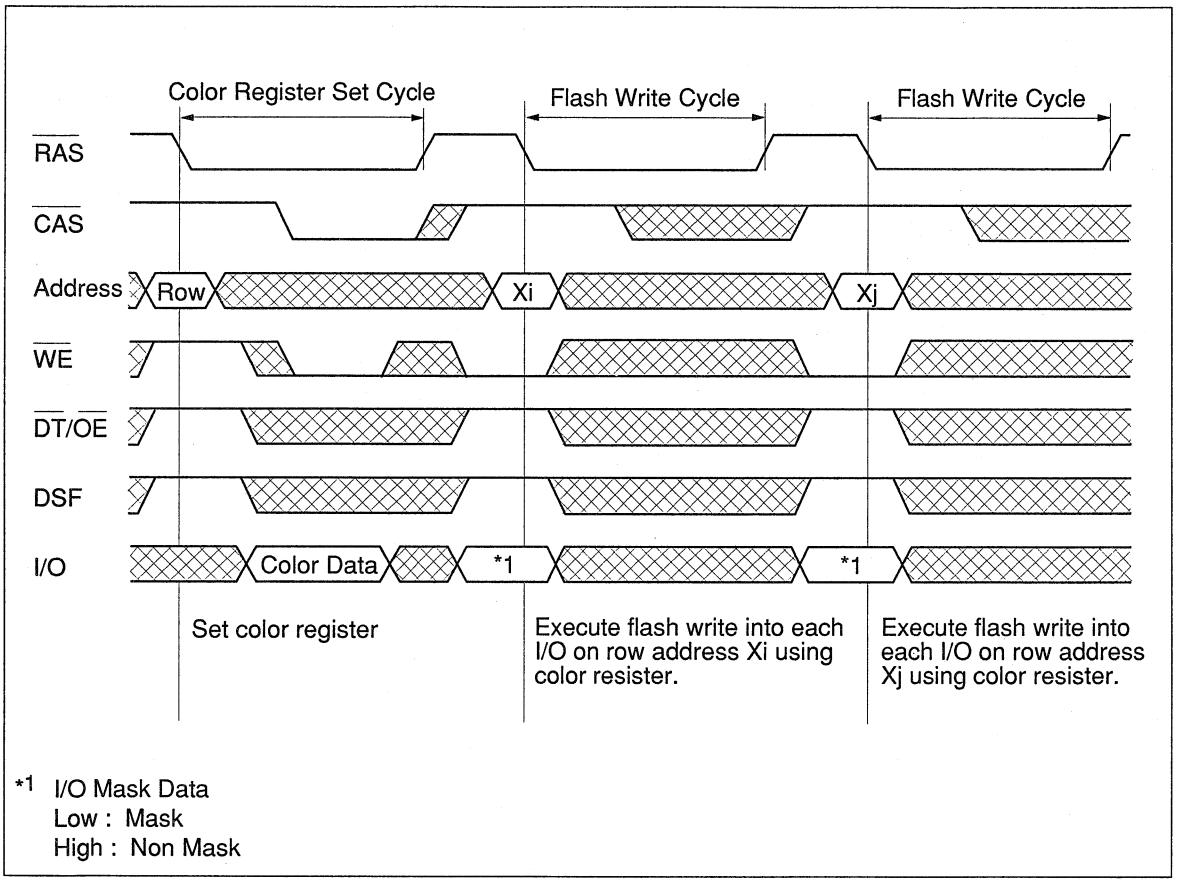


Figure 1 Use of Flash Write

Block Write Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high and DSF low at the falling edge of $\overline{RAS}$, DSF high at the falling edge of $\overline{CAS}$)

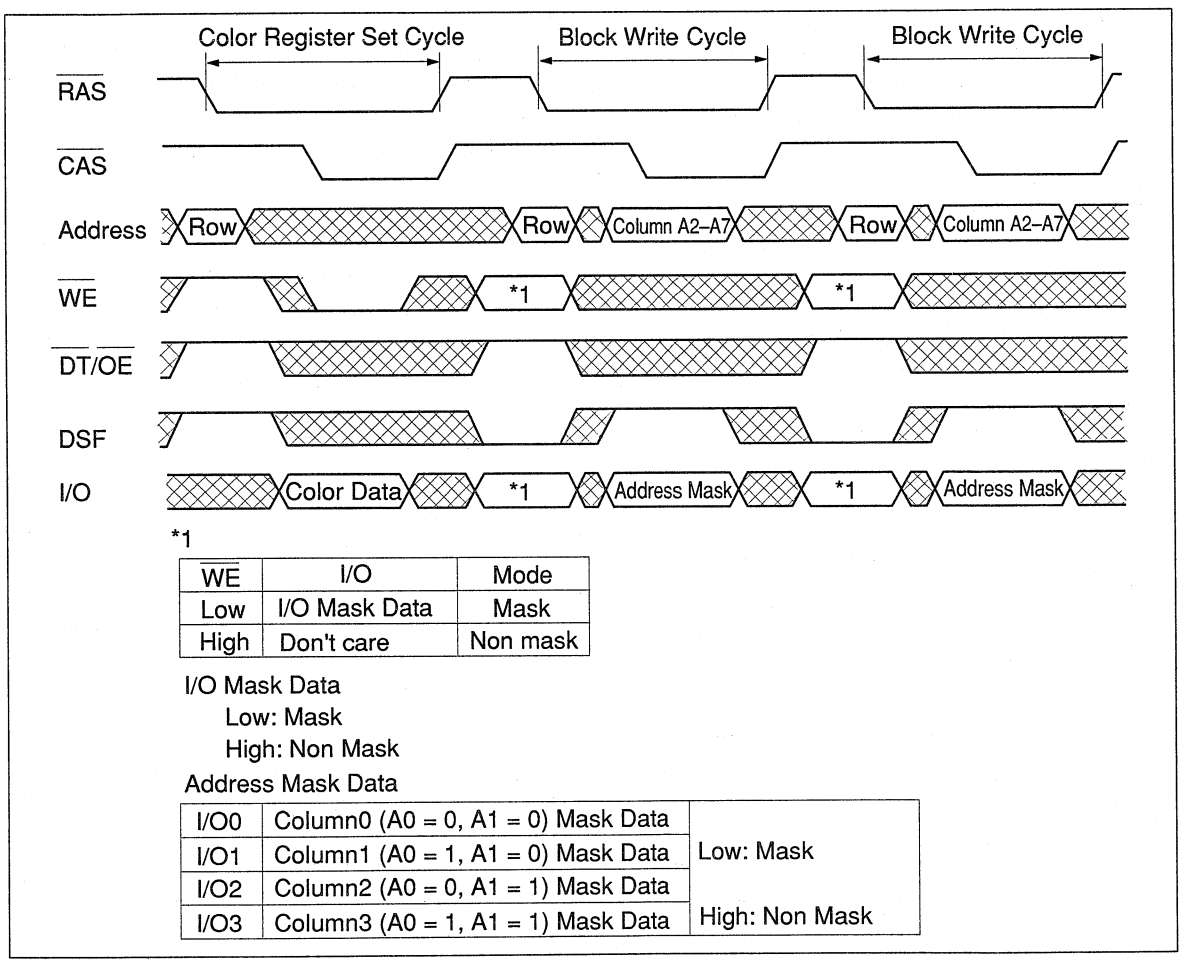
In a block write cycle, 4 columns of data (4-word x 8-bit) is cleared to 0 or 1 at each I/O according to the data of color register. Column addresses A0 and A1 are disregarded. The data on I/Os and addresses can be masked. I/O level at the falling edge of $\overline{CAS}$ determines the address to be cleared. (See figure 2.)

- Normal Mode Block Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

The data on 8 I/Os are all cleared when $\overline{WE}$ is high at the falling edge of $\overline{RAS}$.

- Mask Block Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, HM538123A starts mask block write mode to clear the data on an optional I/O. The mask data is the same as that of a RAM write cycle. High I/O is cleared, low I/O is not cleared and the internal data is retained. The mask data is available in the $\overline{RAS}$ cycle. In page mode block write cycle, the mask data is retained during the page access.



*1

$\overline{WE}$	I/O	Mode
Low	I/O Mask Data	Mask
High	Don't care	Non mask

I/O Mask Data
Low: Mask
High: Non Mask

Address Mask Data

I/O0	Column0 (A0 = 0, A1 = 0) Mask Data	Low: Mask
I/O1	Column1 (A0 = 1, A1 = 0) Mask Data	
I/O2	Column2 (A0 = 0, A1 = 1) Mask Data	High: Non Mask
I/O3	Column3 (A0 = 1, A1 = 1) Mask Data	

Figure 2 Use of Block Write

Transfer Operation

The HM538123A provides the read transfer cycle, split read transfer cycle, pseudo transfer cycle, write transfer cycle and split write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{CAS}$ high and $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)
Read transfer cycle and split read transfer cycle: RAM to SAM
Write transfer cycle and split write transfer cycle: SAM to RAM

(2) Determine SI/O state (except for split read transfer cycle and split write transfer cycle)
Read transfer cycle: SI/O output
Pseudo transfer cycle and write transfer cycle: SI/O input

(3) Determine first SAM address to access after transferring at column address (SAM start address).

SAM start address must be determined by read transfer cycle or pseudo transfer cycle (split transfer cycle isn't available) before SAM access, after power on, and determined for each transfer cycle.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high and DSF low at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by driving $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high and DSF low at the falling edge of $\overline{RAS}$. The row address data (256 x 8-bit) determined by this cycle is transferred to SAM data register synchronously at the rising edge of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address determined by column address. In read transfer cycle, $\overline{DT}/\overline{OE}$ must be risen to transfer data from RAM to SAM.

This cycle can access SAM even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge and t_{SDH} (min) specified between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge must be satisfied. (See figure 3.)

When read transfer cycle is executed, SI/O becomes output state by first SAM access. Input must be set high impedance before t_{SZS} (min) of the first SAM access to avoid data contention.

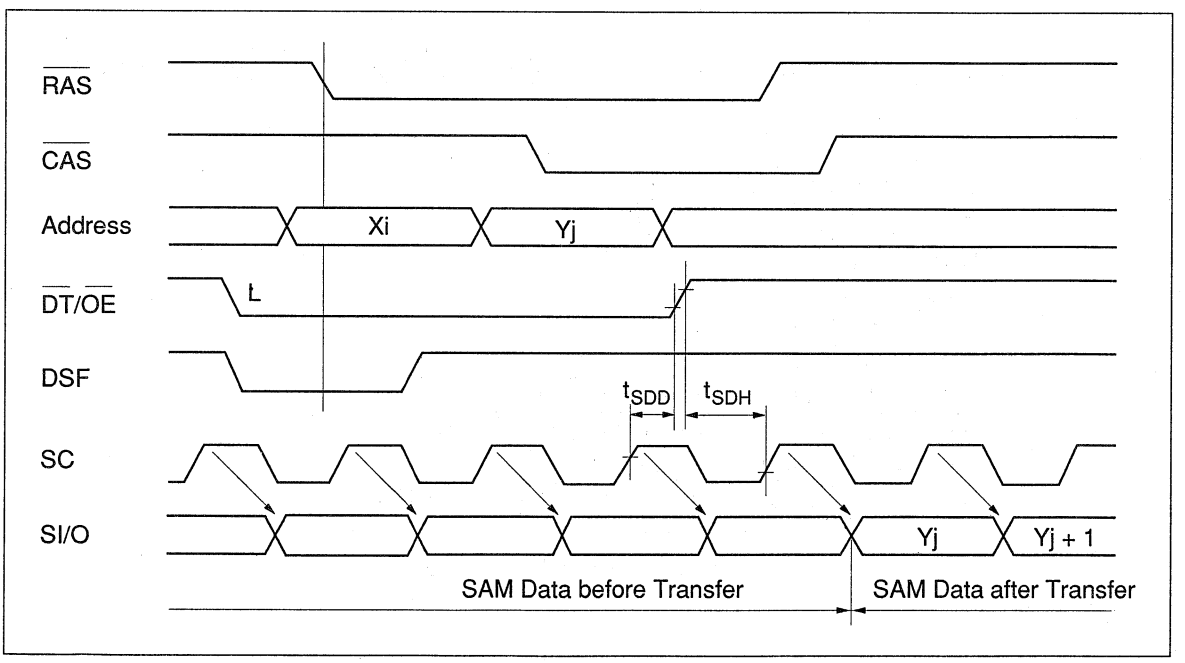


Figure 3 Real Time Read Transfer

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, $\overline{SE}$ high and DSF low at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle switches SI/O to input state and set SAM start address without data transfer to RAM.
This cycle starts when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, $\overline{SE}$ high and DSF low at the falling edge of $\overline{RAS}$. Data should be input to SI/O later than t_{SID} (min) after $\overline{RAS}$ becomes low to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC must not be risen.

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, $\overline{SE}$ low and DSF low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address for serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC must not be risen. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addresses of RAM by write transfer cycle. However, the address to write data must be the same as that of the read transfer cycle or the split read transfer cycle (row address AX8).

Split Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high and DSF high at the falling edge of $\overline{RAS}$)

To execute a continuous serial read by real time read transfer, HM538123A must satisfy SC and $\overline{DT}/\overline{OE}$ timings and requires an external circuit to detect SAM last address. Split read transfer cycle makes it possible to execute a continuous serial read without the above timing limitation. Figure 4 shows the block diagram for a split transfer. SAM data register (DR) consists of 2 split buffers, whose organizations are 128-word x 8-bit each. Let us suppose that data is read from upper data register DR1 (The row address AX8 is 0 and SAM address A7 is 1.). When split read transfer is executed setting row address AX8 0 and SAM start addresses A0 to A6, 128-word x 8-bit data are transferred from RAM to the lower data register DR0 (SAM address A7 is 0) automatically. After data are read from data register DR1, data start to be read from SAM start addresses of data register DR0. If the next split read transfer isn't executed while data are read from data register DR0, data start to be read from SAM start address 0 of DR1 after data are read from data register DR0. If split read transfer is executed setting row address AX8 1 and SAM start addresses A0 to A6 while data are read from data register DR1, 128-word x 8-bit data are transferred to data register DR2. After data are read from data register DR1, data start to be read from SAM start addresses of data register DR2. If the next split read transfer isn't executed while data is read from data register DR2, data start to be read from SAM start address 0 of data register DR3 after data are read from data register DR2. In this time, SAM data is the one transferred to data register DR3 finally while row address AX8 is 1. In split read data transfer, the SAM start address A7 is automatically set in the data register which isn't used.
The data on SAM address A7, which will be accessed next, outputs to QSF, QSF is switched from low to high by accessing SAM last address 127 and from high to low by accessing address 255.
Split read transfer cycle is set when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ is low, $\overline{WE}$ is high and DSF is high at the falling edge of $\overline{RAS}$. The cycle can be executed asyncronously with SC. However, HM538123A must be satisfied t_{STS} (min) timing specified between SC rising and $\overline{RAS}$ falling. SAM start address must be accessed, satisfying t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings specified between $\overline{RAS}$ or $\overline{CAS}$ falling and column address. (See figure 5.)
In split read transfer, SI/O isn't switched to output state. Therefore, read transfer must be executed to switch SI/O to output state when the previous transfer cycle is pseudo transfer or write transfer cycle.

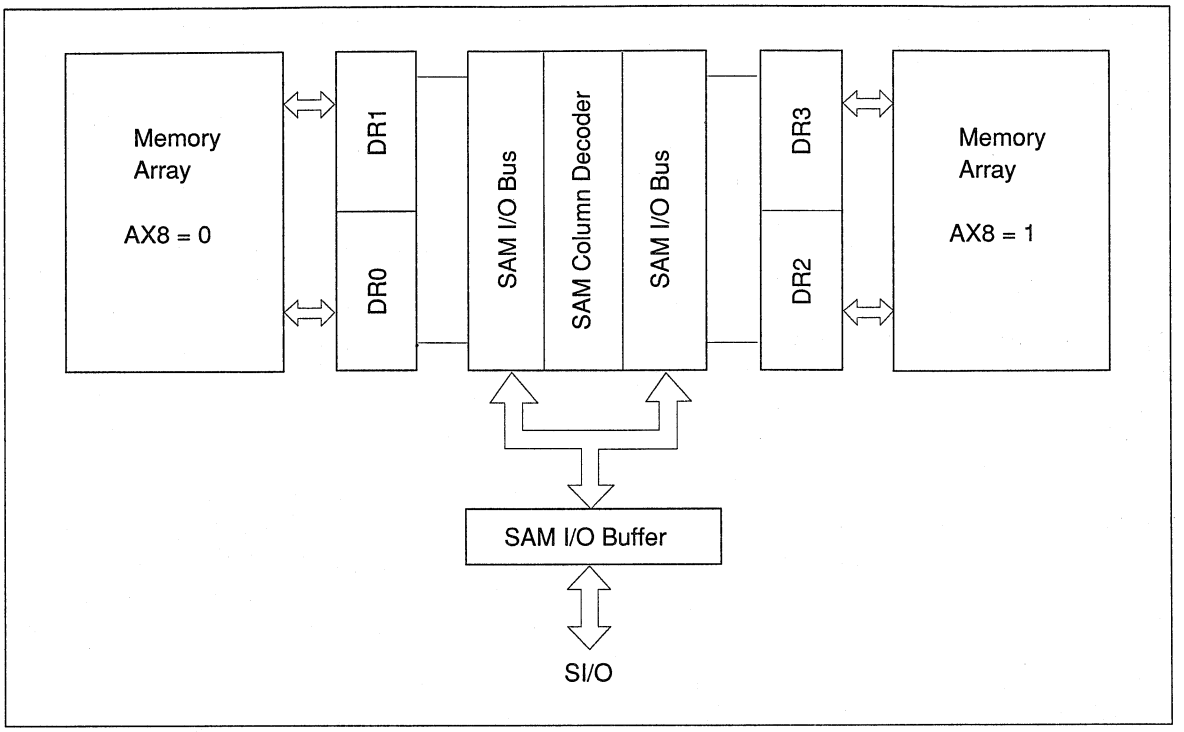


Figure 4 Block Diagram for Split Transfer

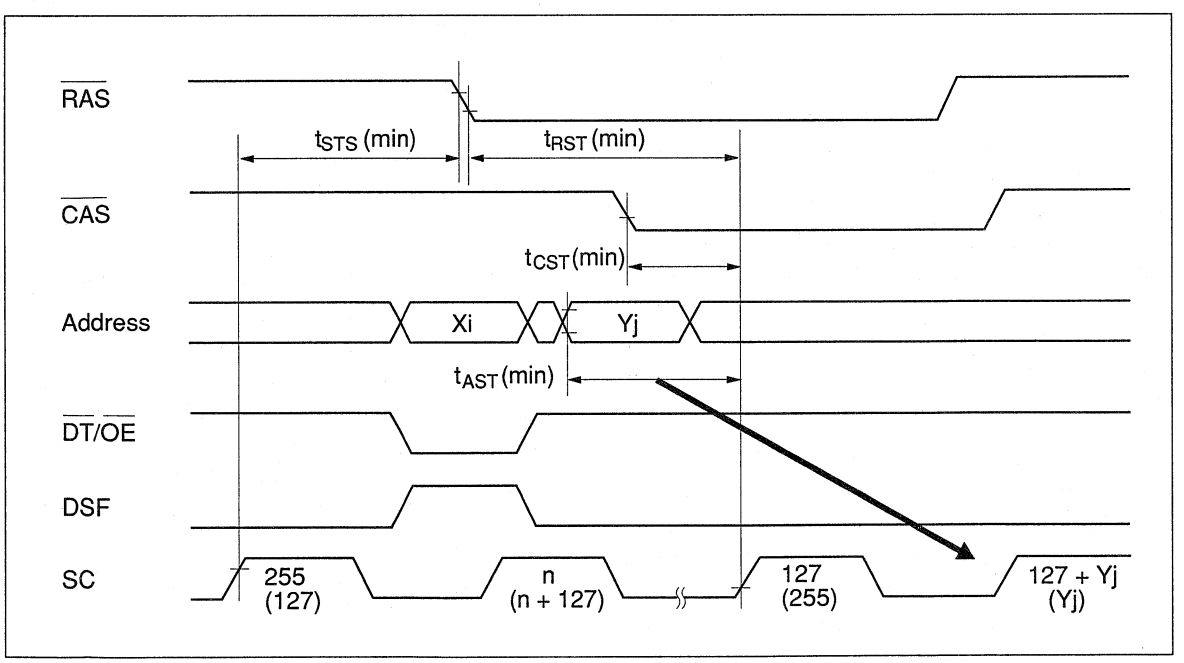


Figure 5 Limitation in Split Transfer

Split Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and DSF high at the falling edge of $\overline{RAS}$)

A continuous serial write cannot be executed because accessing SAM is inhibited during $\overline{RAS}$ low in write transfer. Split write transfer cycle makes it possible. In this cycle, t_{STS} (min), t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings must be satisfied like split read transfer cycle. And it is impossible to switch SI/O to input state in this cycle. If SI/O is in output state, pseudo transfer cycle should be executed to switch SI/O into input state. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addresses of RAM by split write transfer cycle. However, pseudo transfer cycle must be executed before split write transfer cycle. And the MSB of row address (AX8) to write data must be the same as that of the read transfer cycle or the split read transfer cycle.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When $\overline{SE}$ is set high, SI/O becomes high impedance, and the internal pointer is incremented by the SC rising. After indicating the last address (address 255), the internal pointer indicates address 0 at the next access.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is fetched into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't fetched into data register. Internal pointer is incremented by the SC rising, so $\overline{SE}$ high can be used as mask data for SAM. After indicating the last address (address 255), the internal pointer indicates address 0 at the next access.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is executed by accessing all 512 row addresses within 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required when all row addresses are accessed within 8 ms.
(1) $\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is executed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high after inputting the row address (=refresh address) from external circuits. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ must be high at the falling edge of $\overline{RAS}$.
(2) CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate.
(3) Hidden Refresh Cycle: Hidden refresh cycle executes CBR refresh with the data output by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register and selector), organized as fully static circuitry, require no refresh.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage*1	V_T	–1.0 to +7.0	V
Power supply voltage*1	V_{CC}	–0.5 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Note: 1. Relative to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage*1	V_{CC}	4.5	5.0	5.5	V
Input high voltage*1	V_{IH}	2.4	—	6.5	V
Input low voltage*1	V_{IL}	–0.5*2	—	0.8	V

Notes: 1. All voltages referenced to V_{SS}
2. –3.0 V for pulse width ≤ 10 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	HM538123A –6 Min	–6 Max	–7 Min	–7 Max	–8 Min	–8 Max	–10 Min	–10 Max	Unit	Test Conditions RAM port	Test Conditions SAM port
Operating current	I_{CC1}	—	75	—	70	—	60	—	55	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC7}	—	125	—	120	—	100	—	95	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
Standby current	I_{CC2}	—	7	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC8}	—	50	—	50	—	40	—	40	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
$\overline{RAS}$-only refresh current	I_{CC3}	—	75	—	70	—	60	—	55	mA	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH} t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC9}	—	125	—	120	—	100	—	95	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
Page mode current	I_{CC4}	—	80	—	80	—	70	—	65	mA	$\overline{CAS}$ cycling $\overline{RAS}$ = V_{IL} t_{PC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10}	—	130	—	130	—	110	—	105	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	—	50	—	45	—	40	—	35	mA	$\overline{RAS}$ cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC11}	—	100	—	95	—	80	—	75	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
Data transfer current	I_{CC6}	—	80	—	75	—	65	—	60	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC12}	—	130	—	125	—	105	—	100	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	–10	10	µA		
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	–10	10	µA		
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V	I_{OH} = –2 mA	
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V	I_{OL} = 4.2 mA	

Note: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once while $\overline{RAS}$ is low and $\overline{CAS}$ is high.

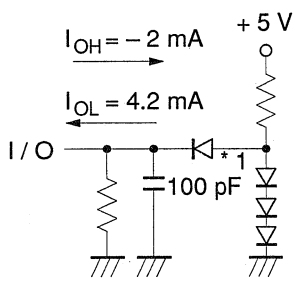
Capacitance (Ta = 25°C, V_{CC} = 5 V, f = 1 MHz, Bias: Clock, I/O = V_{CC}, address = V_{SS})

Item	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clock	C_{I2}	—	—	5	pF
I/O, SI/O, QSF	$C_{I/O}$	—	—	7	pF

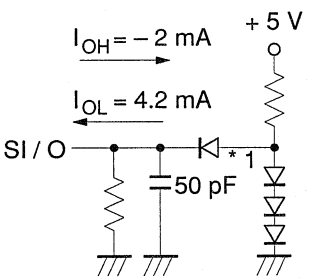
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)*1,*16

Test Conditions

Input pulse levels : V_{SS} to 3.0 V
Input rise and fall time : 5 ns
Output load : See figures
Input timing reference levels : 0.8 V, 2.4 V
Output timing reference levels : 0.8 V, 2.0 V



Output Load (A)



Output Load (B)

Note: 1. Including scope & jig

Common Parameter

Item	Symbol	HM538123A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
Random read or write cycle time	t_{RC}	125	—	135	—	150	—	180	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	55	—	55	—	60	—	70	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	—	20	—	20	—	25	—	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	20	60	20	75	ns	2
$\overline{RAS}$ hold time referenced to $\overline{CAS}$	t_{RSH}	20	—	20	—	20	—	25	—	ns	
$\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Transition time (rise to fall)	t_T	3	50	3	50	3	50	3	50	ns	3
Refresh period	t_{REF}	—	8	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ setup time	t_{DTS}	0	—	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ hold time	t_{DTH}	10	—	10	—	10	—	10	—	ns	
DSF to $\overline{RAS}$ setup time	t_{FSR}	0	—	0	—	0	—	0	—	ns	
DSF to $\overline{RAS}$ hold time	t_{RFH}	10	—	10	—	10	—	10	—	ns	
DSF to $\overline{CAS}$ setup time	t_{FSC}	0	—	0	—	0	—	0	—	ns	
DSF to $\overline{CAS}$ hold time	t_{CFH}	15	—	15	—	15	—	15	—	ns	
Data-in to $\overline{CAS}$ delay time	t_{DZC}	0	—	0	—	0	—	0	—	ns	4
Data-in to $\overline{OE}$ delay time	t_{DZO}	0	—	0	—	0	—	0	—	ns	4
Output buffer turn-off delay referenced to $\overline{CAS}$	t_{OFF1}	—	20	—	20	—	20	—	20	ns	5

Common Parameter (cont)

Item	Symbol	HM538123A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	—	20	—	20	—	20	—	20	ns	5

Read Cycle (RAM), Page Mode Read Cycle

Item	Symbol	HM538123A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	35	—	40	—	45	ns	7, 9
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	0	—	ns	10
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	10
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	2
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	35	—	40	—	45	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	35	—	35	—	40	—	45	—	ns	
Page mode cycle time	t_{PC}	45	—	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	10	—	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	—	40	—	45	—	50	ns	
Page mode $\overline{RAS}$ pulse width	t_{RASP}	60	100000	70	100000	80	100000	100	100000	ns	

Write Cycle (RAM), Page Mode Write Cycle, Color Register Set Cycle

		HM538123A									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
Write command setup time	t_{WCS}	0	—	0	—	0	—	0	—	ns	11
Write command hold time	t_{WCH}	15	—	15	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	15	—	15	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	15	—	15	—	15	—	15	—	ns	12
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	10	—	10	—	10	—	10	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	10	—	10	—	10	—	10	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	20	—	20	—	20	—	20	—	ns	
Page mode cycle time	t_{PC}	45	—	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ to data-in delay time	t_{CDD}	20	—	20	—	20	—	20	—	ns	13
Page mode $\overline{RAS}$ pulse width	t_{RASP}	60	100000	70	100000	80	100000	100	100000	ns	

Read-Modify-Write Cycle

		HM538123A									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
Read-modify-write cycle time	t_{RWC}	175	—	185	—	200	—	230	—	ns	
$\overline{RAS}$ pulse width (read-modify-write cycle)	t_{RWS}	110	10000	120	10000	130	10000	150	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	45	—	45	—	45	—	50	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	60	—	60	—	65	—	70	—	ns	14
$\overline{OE}$ to data-in delay time	t_{ODD}	20	—	20	—	20	—	20	—	ns	12
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	35	—	40	—	45	ns	7, 9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	20	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	15	—	15	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	15	—	15	—	15	—	15	—	ns	12
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	20	—	20	—	20	—	20	—	ns	

Refresh Cycle

Item	Symbol	HM538123A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

Flash Write Cycle, Block Write Cycle

Item	Symbol	HM538123A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
$\overline{CAS}$ to data-in delay time	t_{CDD}	20	—	20	—	20	—	20	—	ns	13
$\overline{OE}$ to data-in delay time	t_{ODD}	20	—	20	—	20	—	20	—	ns	13

Read Transfer Cycle

Item	Symbol	HM538123A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
$\overline{DT}$ hold time referenced to $\overline{RAS}$	t_{RDH}	50	10000	60	10000	65	10000	80	10000	ns	
$\overline{DT}$ hold time referenced to $\overline{CAS}$	t_{CDH}	20	—	20	—	20	—	25	—	ns	
$\overline{DT}$ hold time referenced to column address	t_{ADH}	25	—	25	—	30	—	30	—	ns	
$\overline{DT}$ precharge time	t_{DTP}	20	—	20	—	20	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ delay time	t_{DRD}	65	—	65	—	70	—	80	—	ns	
SC to $\overline{RAS}$ setup time	t_{SRS}	25	—	25	—	30	—	30	—	ns	
1st SC to $\overline{RAS}$ hold time	t_{SRH}	60	—	70	—	80	—	100	—	ns	
1st SC to $\overline{CAS}$ hold time	t_{SCH}	25	—	25	—	25	—	25	—	ns	

Read Transfer Cycle (cont)

Item	Symbol	HM538123A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
1st SC to column address hold time	t_{SAH}	40	—	40	—	45	—	50	—	ns	
Last SC to $\overline{DT}$ delay time	t_{SDD}	5	—	5	—	5	—	5	—	ns	
1st SC to $\overline{DT}$ hold time	t_{SDH}	10	—	10	—	15	—	15	—	ns	
$\overline{RAS}$ to QSF delay time	t_{RQD}	—	65	—	70	—	75	—	85	ns	15
$\overline{CAS}$ to QSF delay time	t_{CQD}	—	35	—	35	—	40	—	40	ns	15
$\overline{DT}$ to QSF delay time	t_{DQD}	—	35	—	35	—	35	—	35	ns	15
QSF hold time referenced to $\overline{RAS}$	t_{RQH}	20	—	20	—	20	—	25	—	ns	
QSF hold time referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	5	—	5	—	ns	
QSF hold time referenced to $\overline{DT}$	t_{DQH}	5	—	5	—	5	—	5	—	ns	
Serial data-in to 1st SC delay time	t_{SZS}	0	—	0	—	0	—	0	—	ns	
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	35	—	40	—	45	—	ns	
$\overline{RAS}$ precharge to $\overline{DT}$ high hold time	t_{DTHH}	10	—	10	—	10	—	10	—	ns	

Pseudo Transfer Cycle, Write Transfer Cycle

Item	Symbol	HM538123A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
$\overline{SE}$ setup time referenced to $\overline{RAS}$	t_{ES}	0	—	0	—	0	—	0	—	ns	
$\overline{SE}$ hold time referenced to $\overline{RAS}$	t_{EH}	10	—	10	—	10	—	10	—	ns	
SC setup time referenced to $\overline{RAS}$	t_{SRS}	25	—	25	—	30	—	30	—	ns	
$\overline{RAS}$ to SC delay time	t_{SRD}	20	—	20	—	25	—	25	—	ns	
Serial output buffer turn-off time referenced to $\overline{RAS}$	t_{SRZ}	10	40	10	40	10	45	10	50	ns	
$\overline{RAS}$ to serial data-in delay time	t_{SID}	40	—	40	—	45	—	50	—	ns	
$\overline{RAS}$ to QSF delay time	t_{RQD}	—	65	—	70	—	75	—	85	ns	15
$\overline{CAS}$ to QSF delay time	t_{CQD}	—	35	—	35	—	40	—	40	ns	15
QSF hold time referenced to $\overline{RAS}$	t_{RQH}	20	—	20	—	20	—	25	—	ns	
QSF hold time referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	5	—	5	—	ns	
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
$\overline{SE}$ access time	t_{SEA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial write enable setup time	t_{SWS}	5	—	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	

Split Read Transfer Cycle, Split Write Transfer Cycle

Item	Symbol	HM538123A -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Note
Split transfer setup time	t_{STS}	20	—	20	—	20	—	25	—	ns	
Split transfer hold time referenced to $\overline{RAS}$	t_{RST}	60	—	70	—	80	—	100	—	ns	
Split transfer hold time referenced to $\overline{CAS}$	t_{CST}	20	—	20	—	20	—	25	—	ns	
Split transfer hold time referenced to column address	t_{AST}	35	—	35	—	40	—	45	—	ns	
SC to QSF delay time	t_{SQD}	—	30	—	30	—	30	—	30	ns	15
QSF hold time referenced to SC	t_{SQH}	5	—	5	—	5	—	5	—	ns	
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	35	—	40	—	45	—	ns	

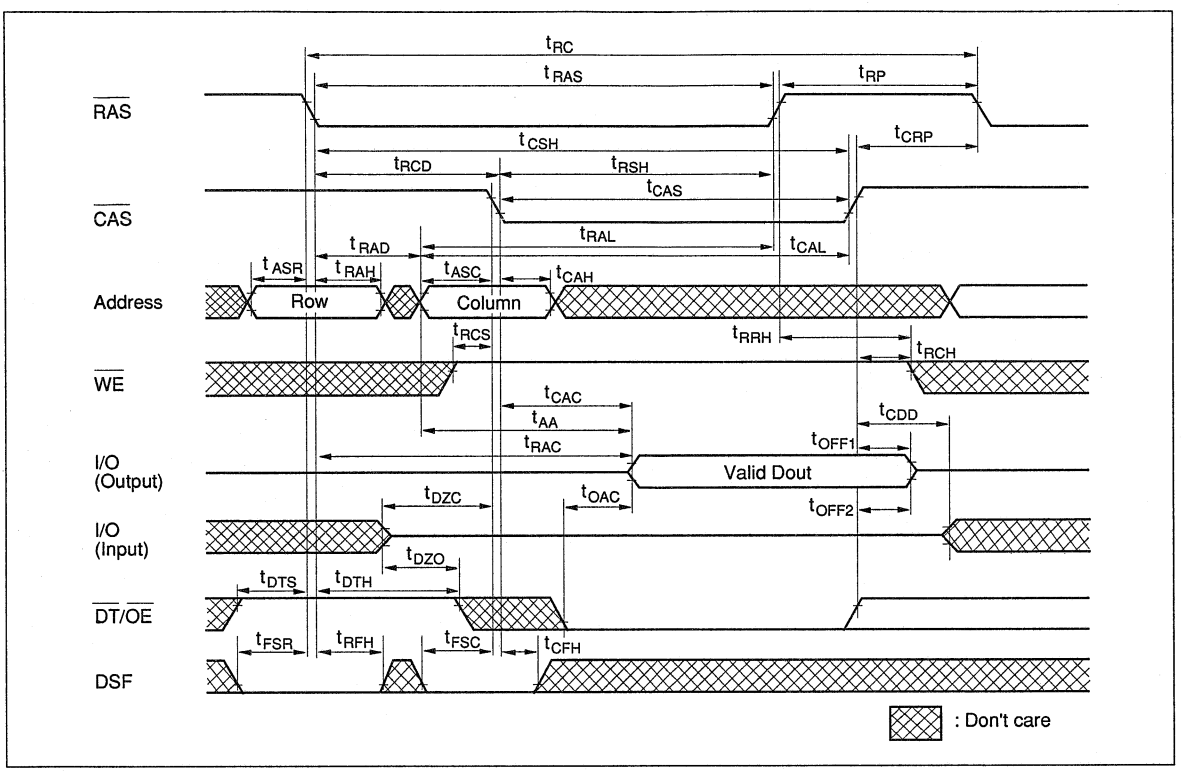
Serial Read Cycle, Serial Write Cycle

		HM538123A									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Access time from SC	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
Access time from $\overline{SE}$	t_{SEA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial output buffer turn-off time referenced to $\overline{SE}$	t_{SEZ}	—	20	—	20	—	20	—	20	ns	5
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	
Serial write enable setup time	t_{SWS}	5	—	5	—	5	—	5	—	ns	
Serial write enable hold time	t_{SWH}	15	—	15	—	15	—	15	—	ns	
Serial write disable setup time	t_{SWIS}	5	—	5	—	5	—	5	—	ns	
Serial write disable hold time	t_{SWIH}	15	—	15	—	15	—	15	—	ns	

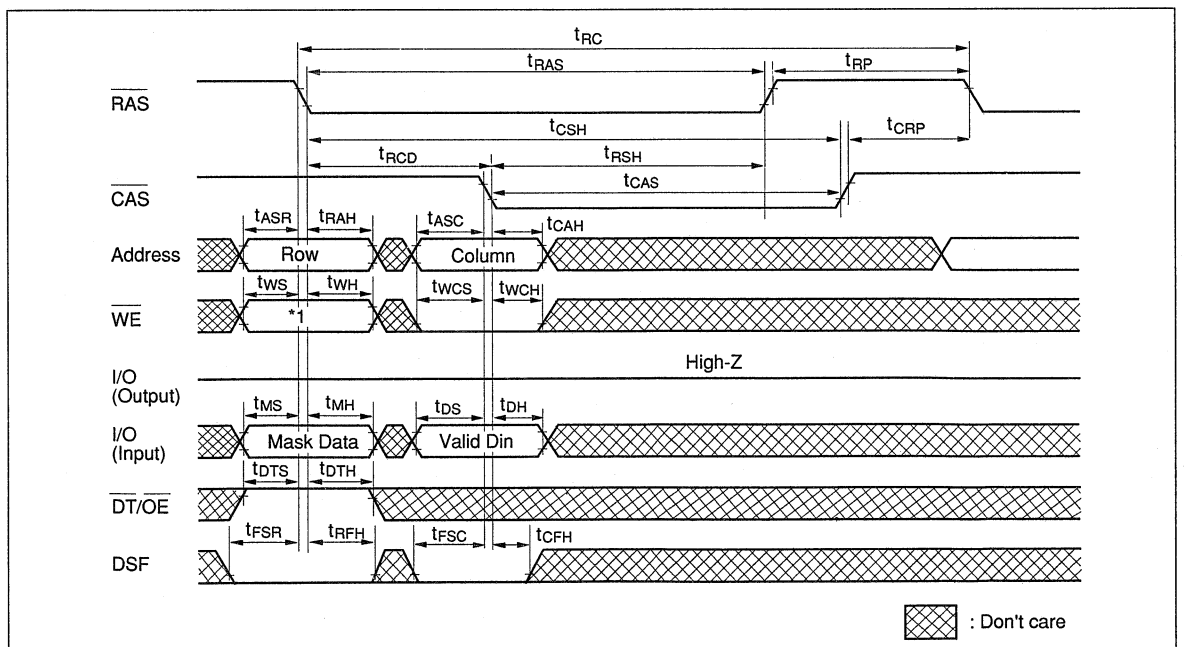
Notes:
1. AC measurements assume t_T = 5 ns.
2. When $t_{RCD} > t_{RCD}$ (max) or $t_{RAD} > t_{RAD}$ (max), access time is specified by t_{CAC} or t_{AA}.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition time t_T is measured between V_{IH} and V_{IL}.
4. Data input must be floating before output buffer is turned on. In read cycle, read-modify-write cycle and delayed write cycle, either t_{DZC} (min) or t_{DZO} (min) must be satisfied.
5. t_{OFF1} (max), t_{OFF2} (max) and t_{SEZ} (max) are defined as the time at which the output achieves the open circuit condition (V_{OH} – 100 mV, V_{OL} + 100 mV).
6. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
8. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
9. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
10. If either t_{RCH} of t_{RRH} is satisfied, operation is guaranteed.
11. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
12. These parameters are specified by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
13. Either t_{CDD} (min) or t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{CAS}$ or $\overline{OE}$ prior to applying data to the device when output buffer is on.
14. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min) in read-modify-write cycle, the data of the selected address outputs to an I/O pin and input data is written into the selected address. t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{OE}$ prior to applying data to the device.
15. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
16. After power-up, pause for 100 µs or more and execute at least 8 initialization cycle (normal memory cycle or refresh cycle), then start operation.

Timing Waveforms

Read Cycle

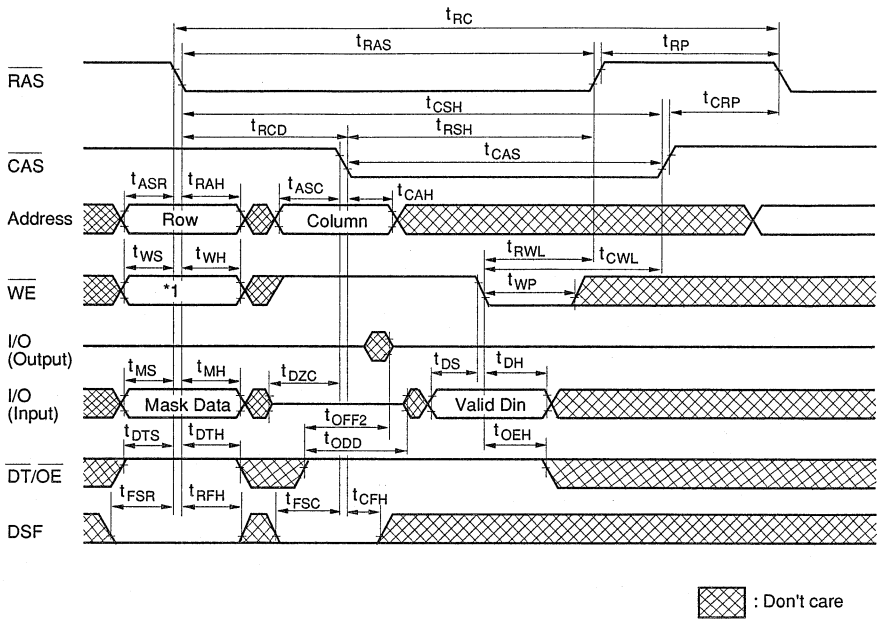


Early Write Cycle



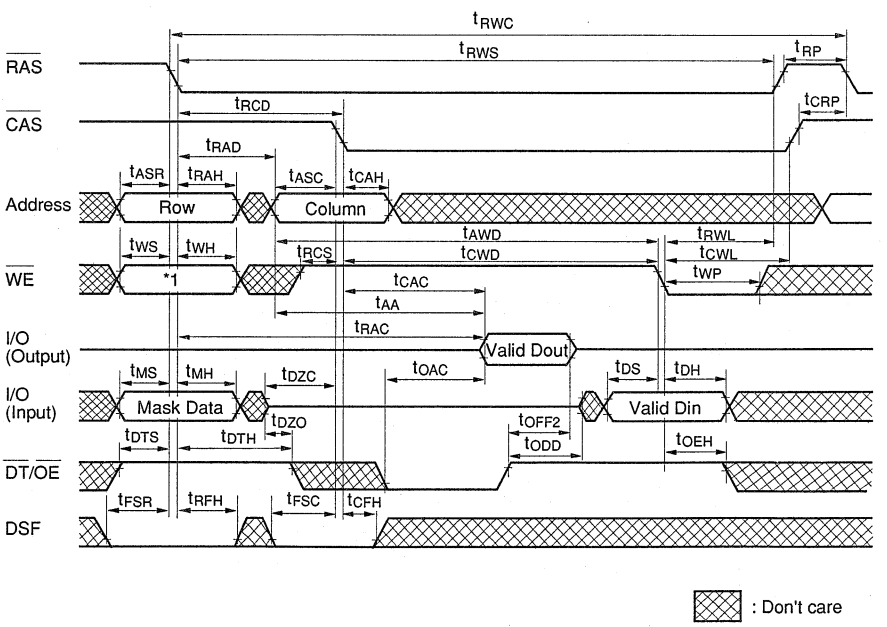
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Delayed Write Cycle



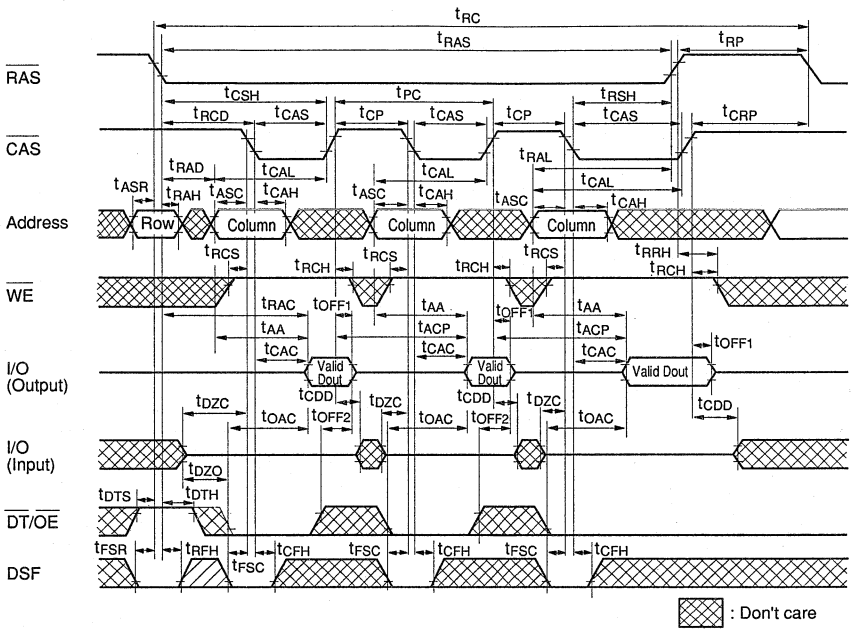
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Read-Modify-Write Cycle

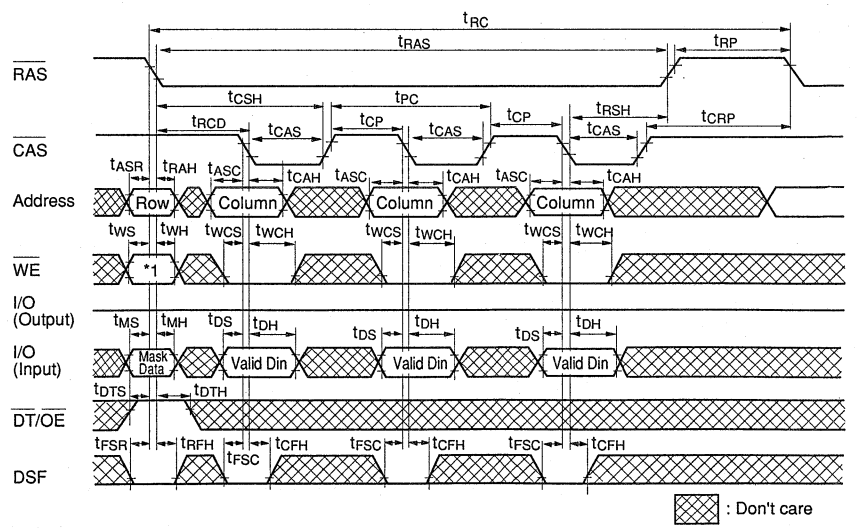


Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Page Mode Read Cycle

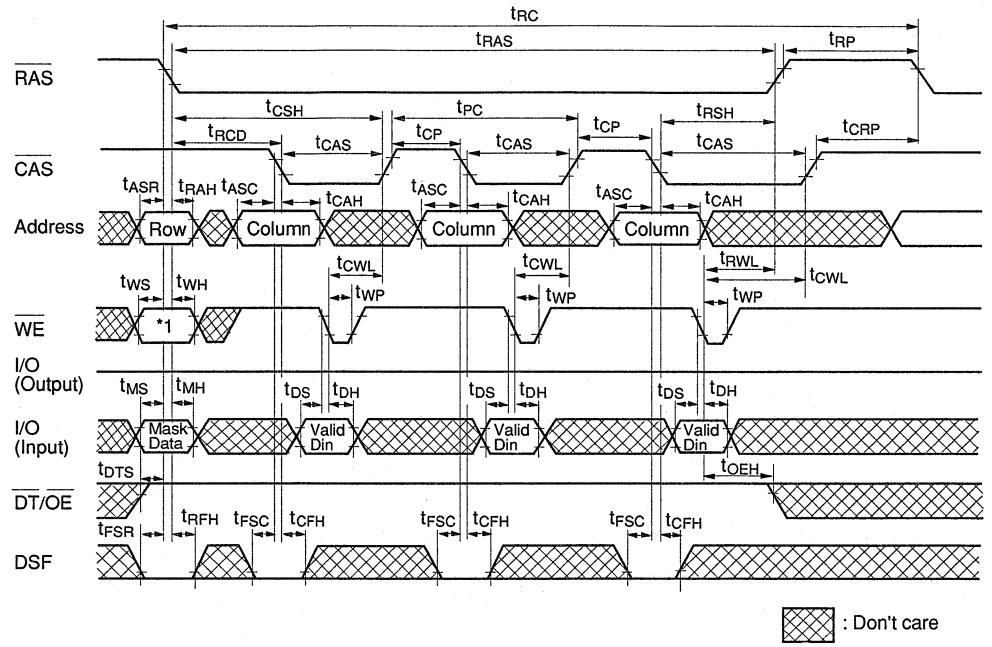


Page Mode Write Cycle (Early Write)



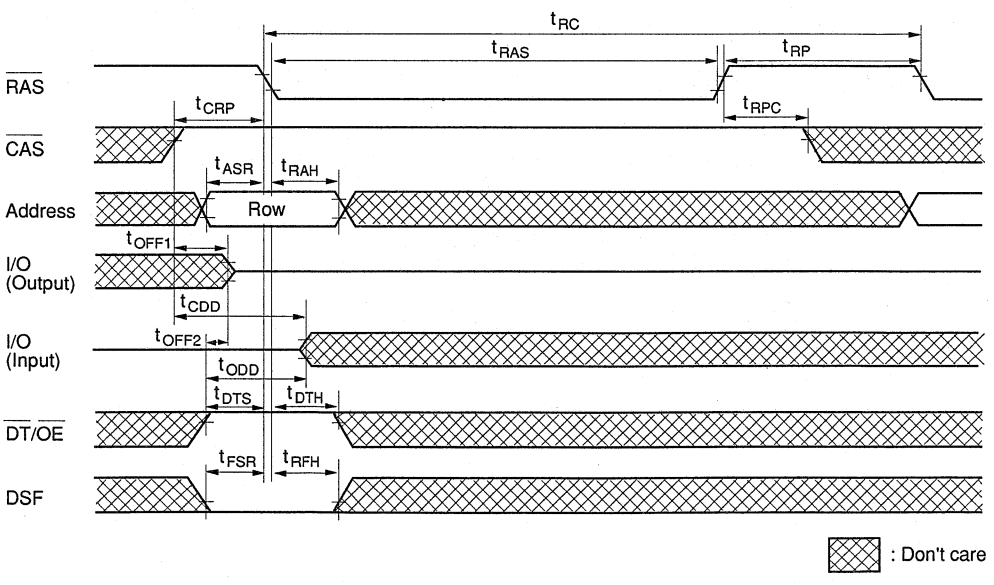
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Page Mode Write Cycle (Delayed Write)

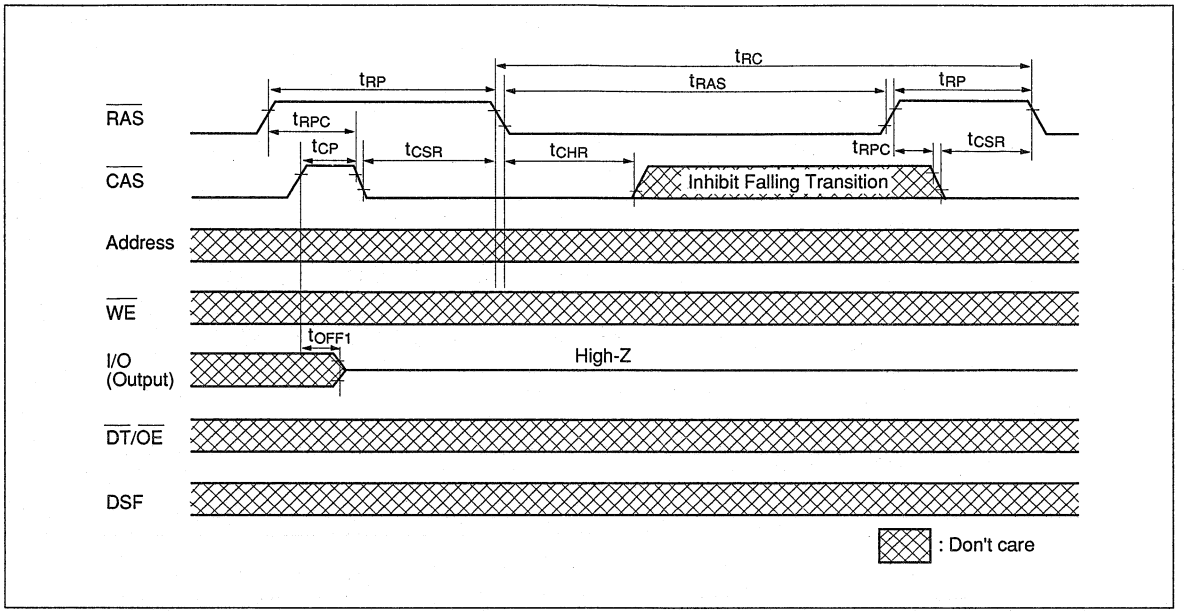


Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

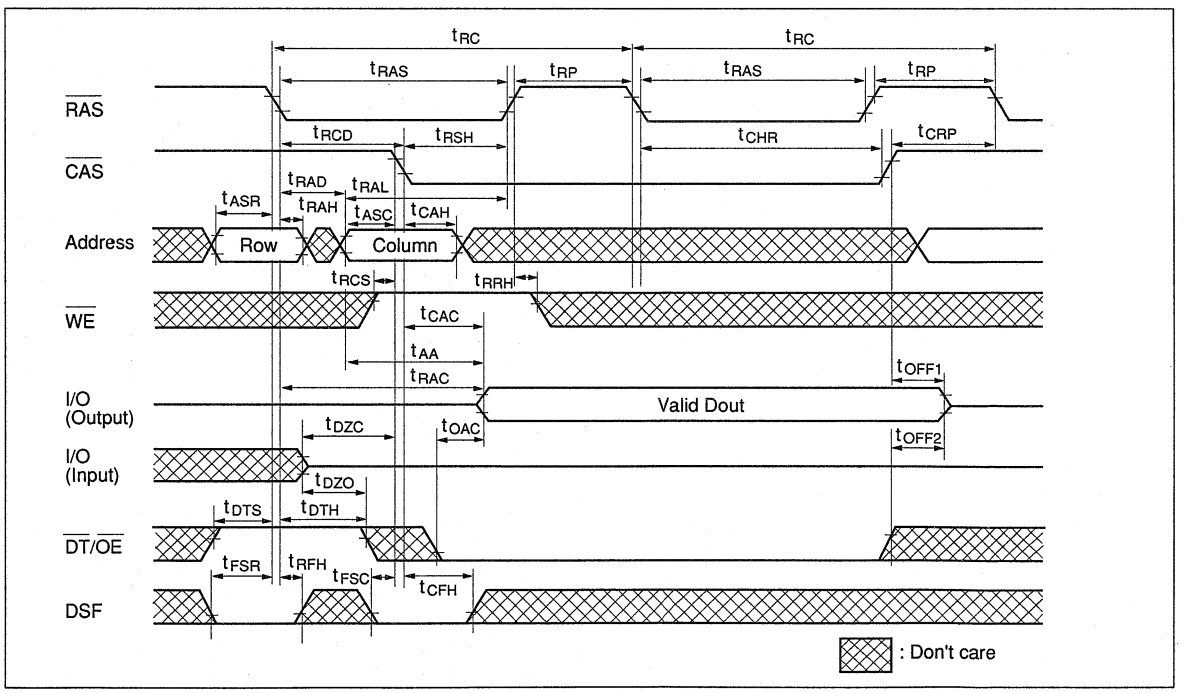
$\overline{RAS}$-Only Refresh Cycle



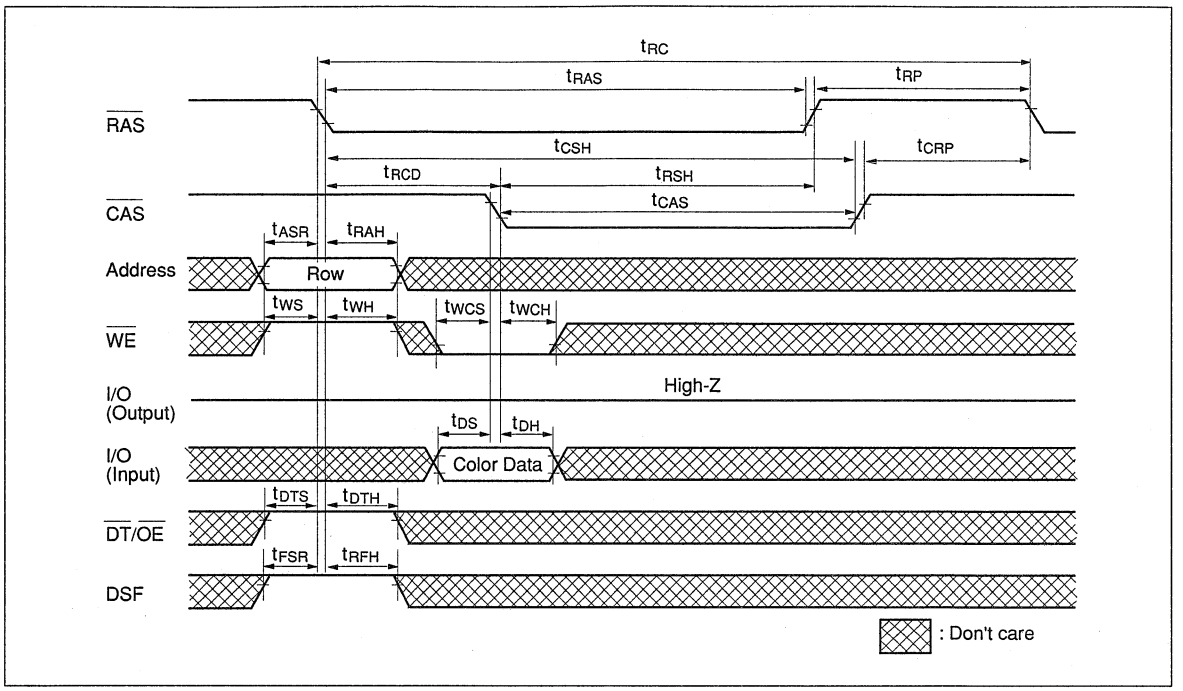
CAS-Before-RAS Refresh Cycle



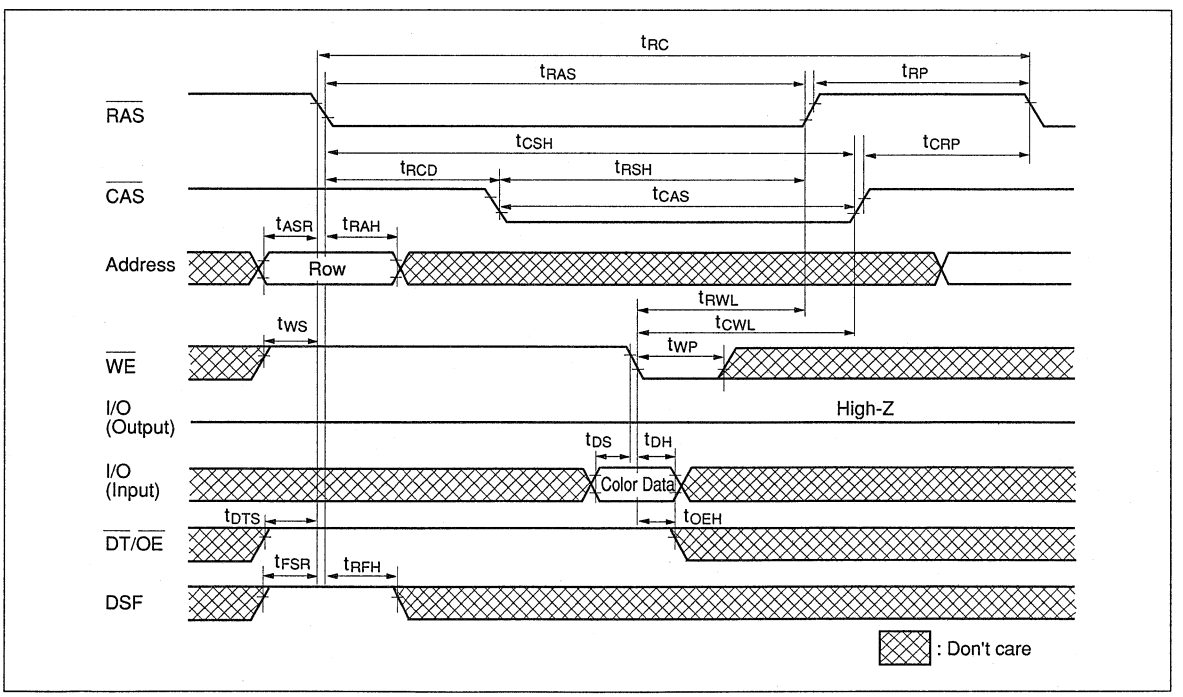
Hidden Refresh Cycle



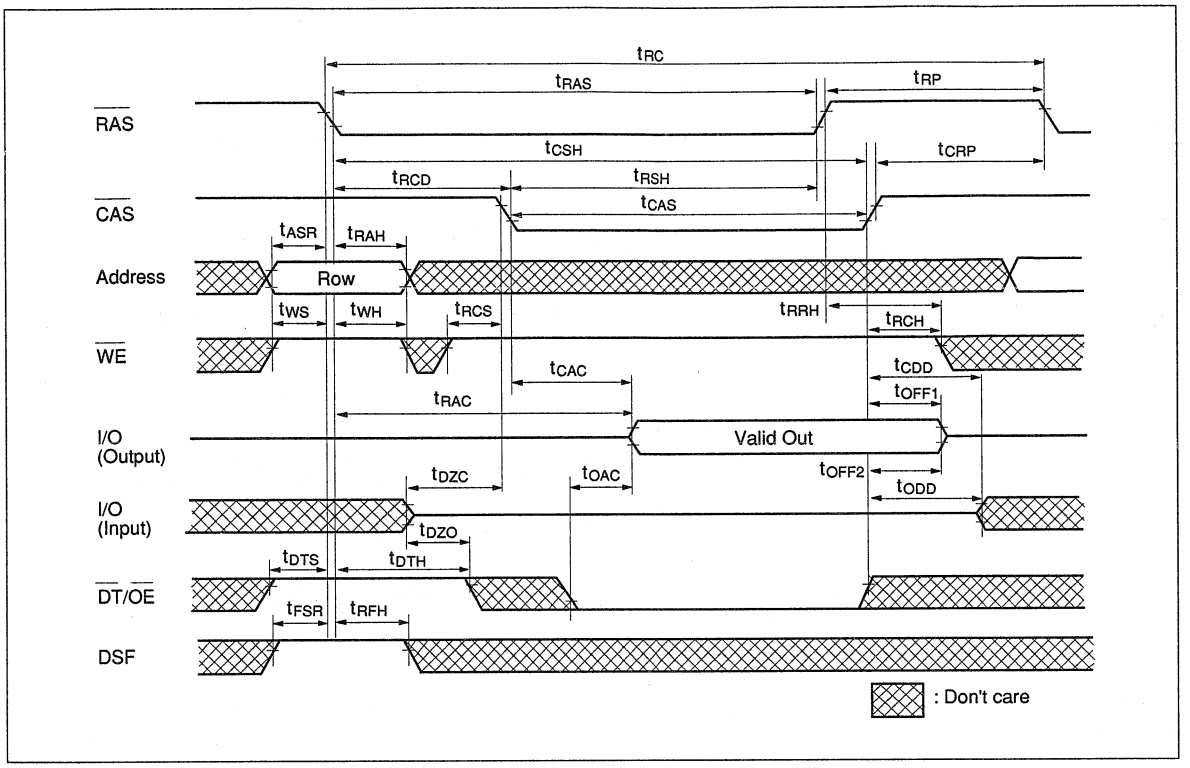
Color Register Set Cycle (Early Write)



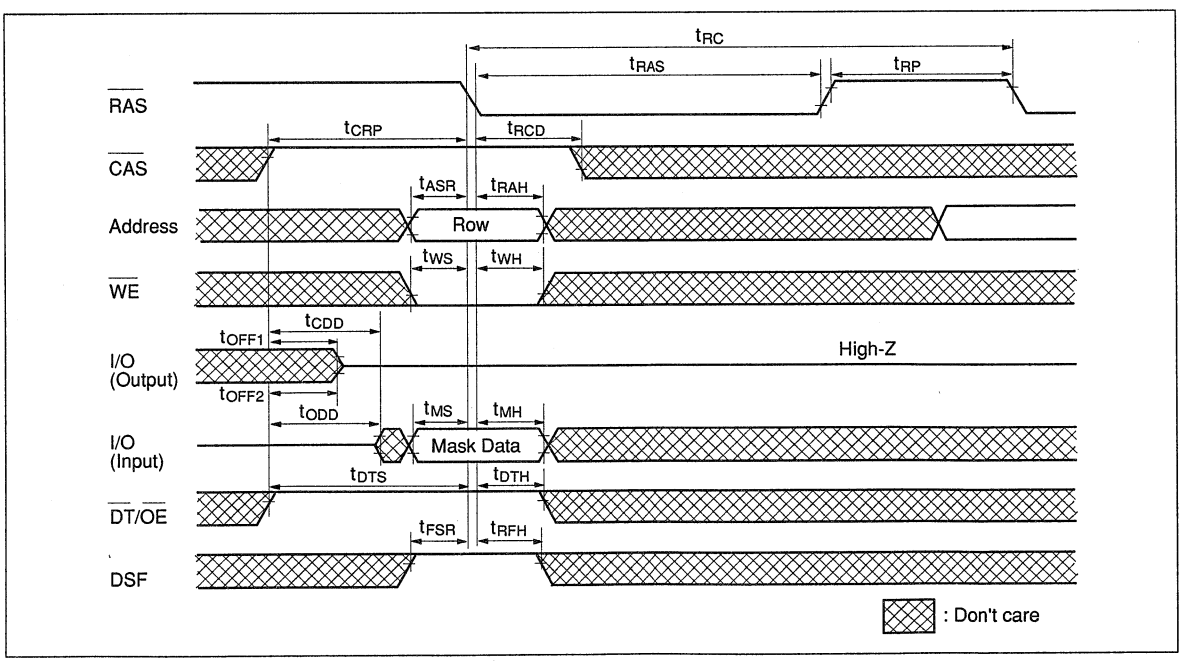
Color Register Set Cycle (Delayed Write)



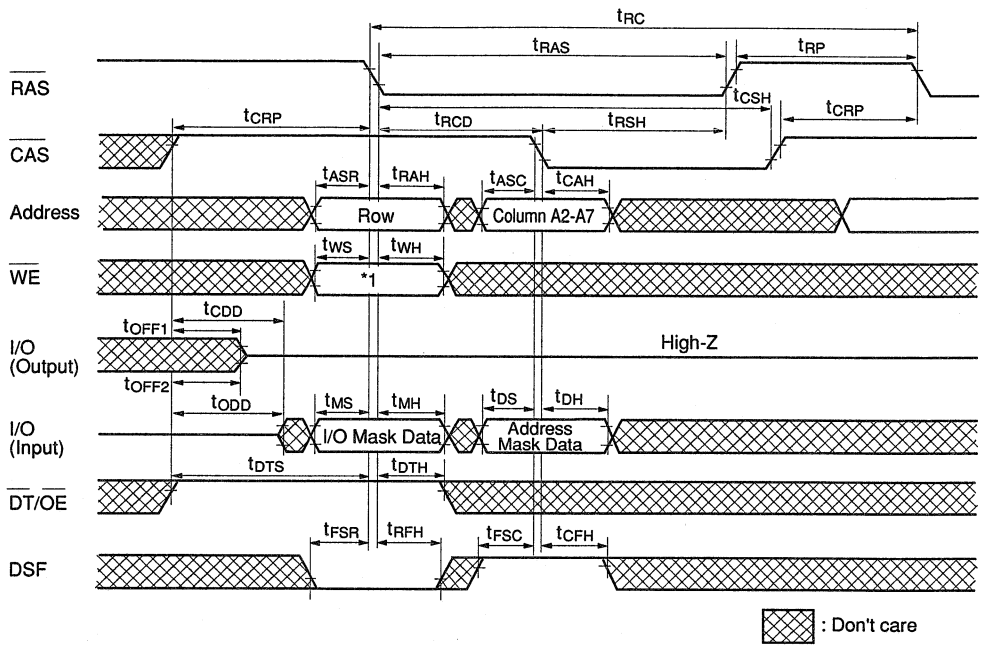
Color Register Read Cycle



Flash Write Cycle

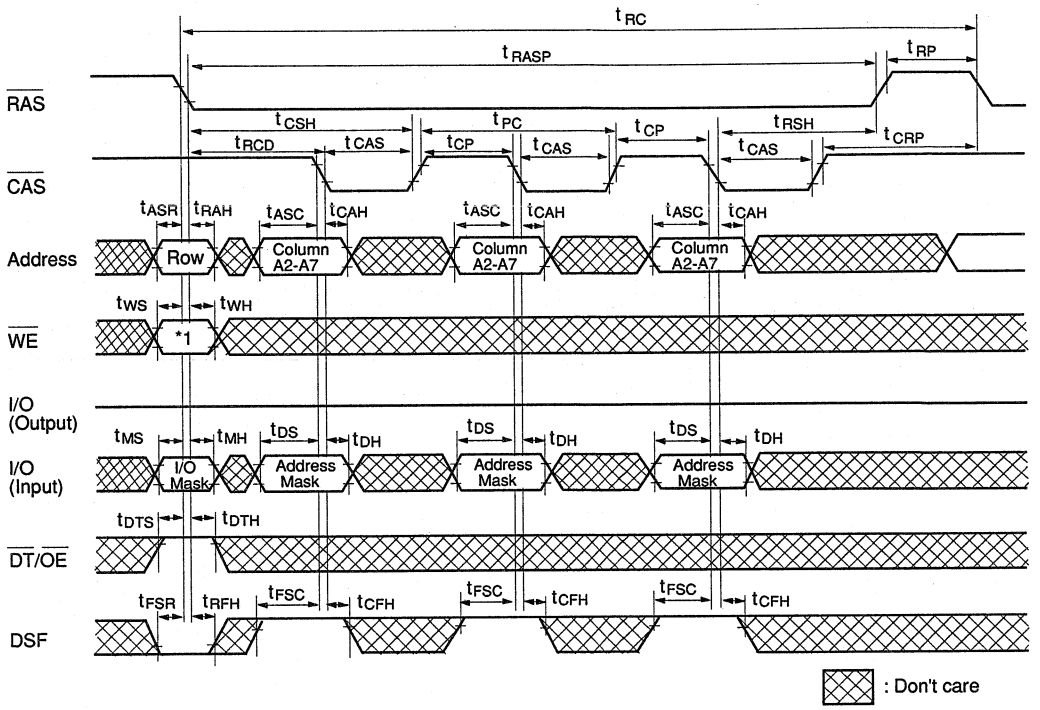


Block Write Cycle



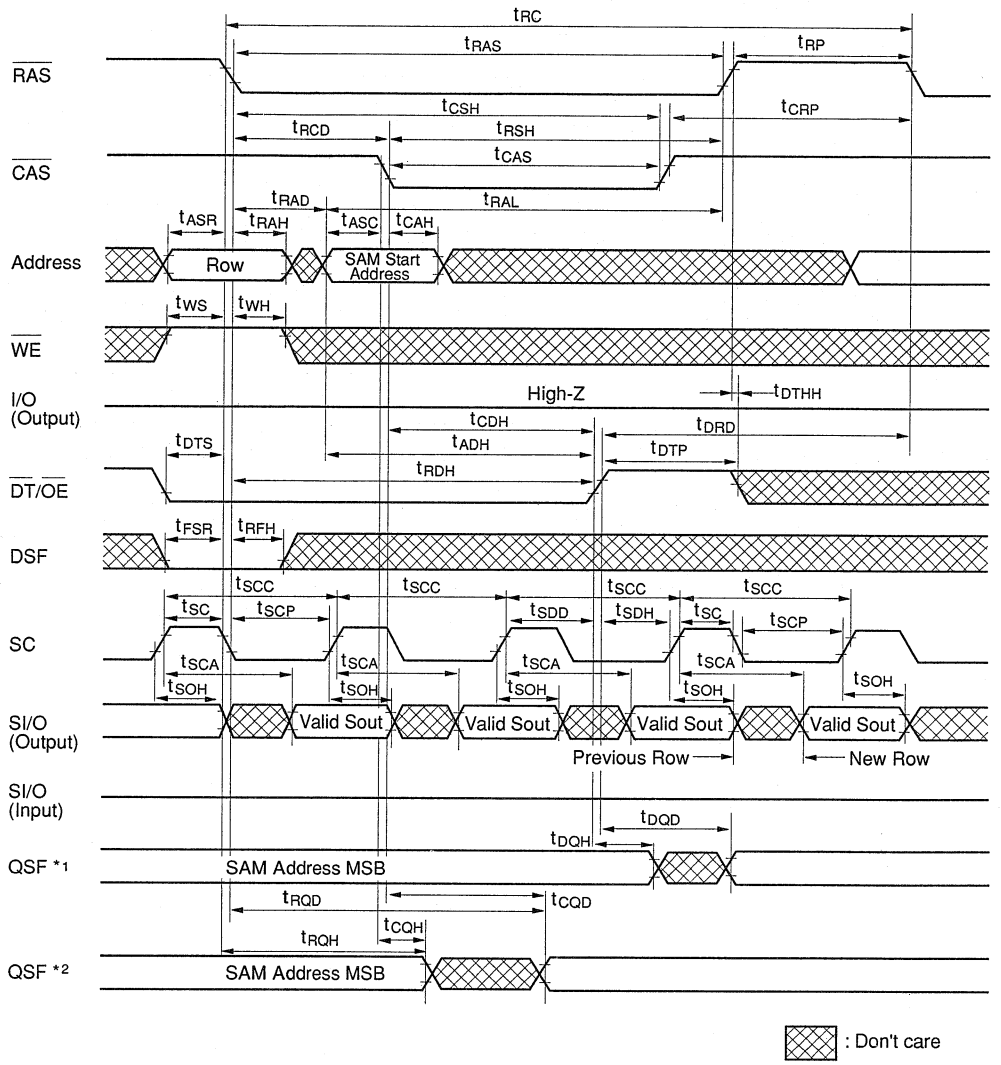
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Page Mode Block Write Cycle



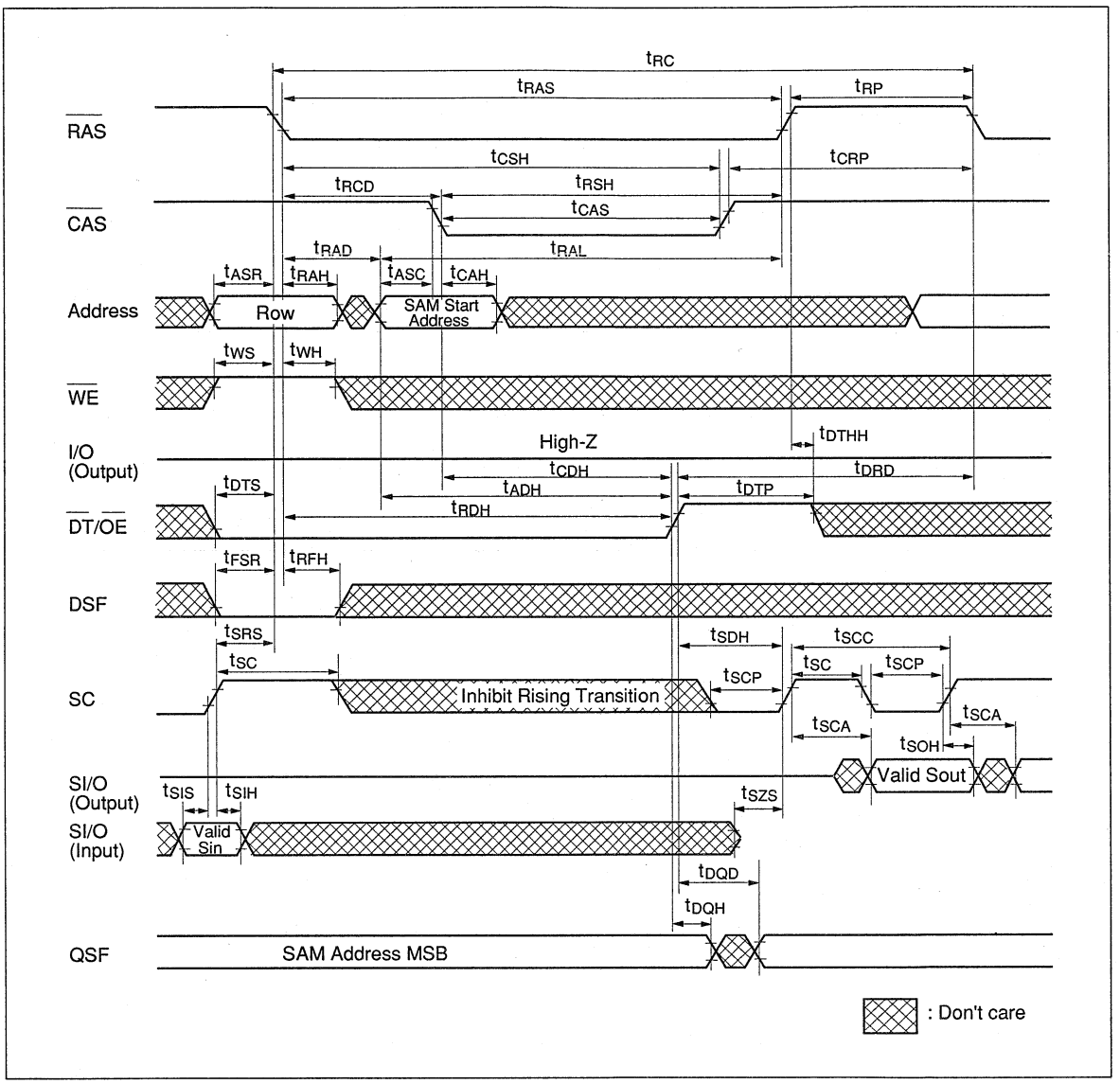
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Read Transfer Cycle (1)

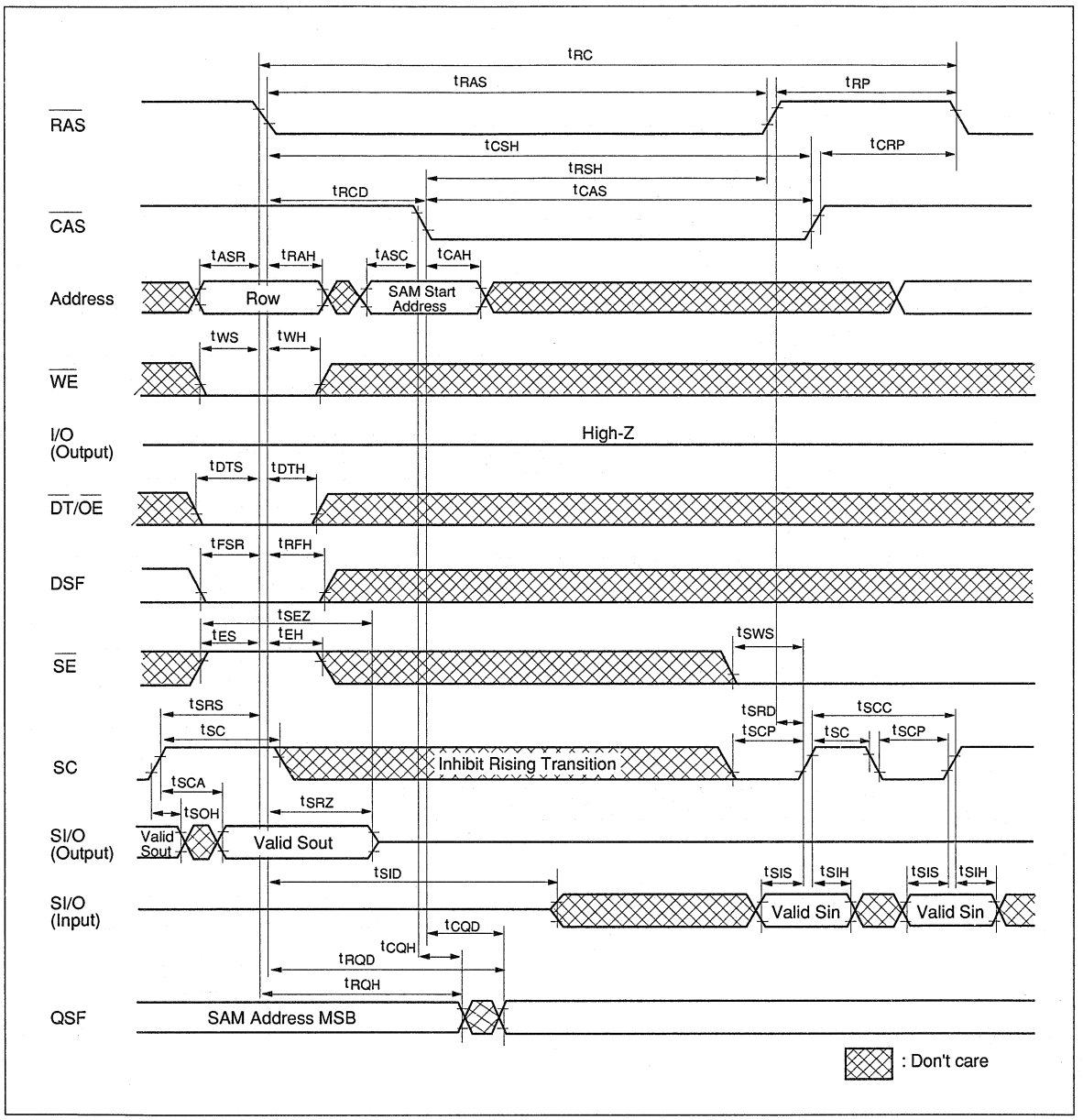


Note:
1. This QSF timing is referred when SC is risen once or more between the previous transfer cycle and $\overline{CAS}$ falling edge of this cycle (QSF is switched by $\overline{DT}$ rising).
2. This QSF timing is referred when SC isn't risen between the previous transfer cycle and $\overline{CAS}$ falling edge of this cycle (QSF is switched by $\overline{RAS}$ or $\overline{CAS}$ falling).

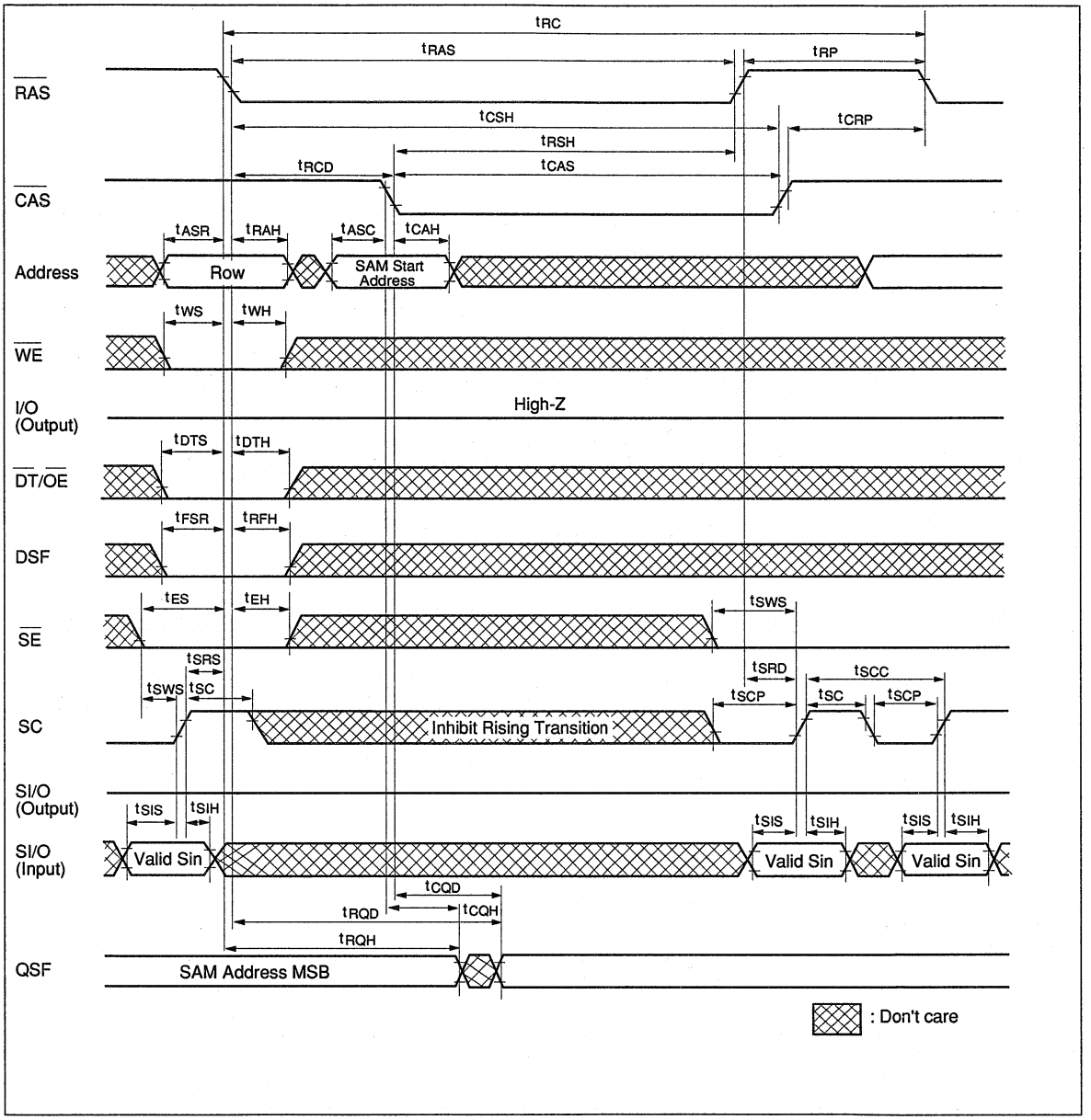
Read Transfer Cycle (2)



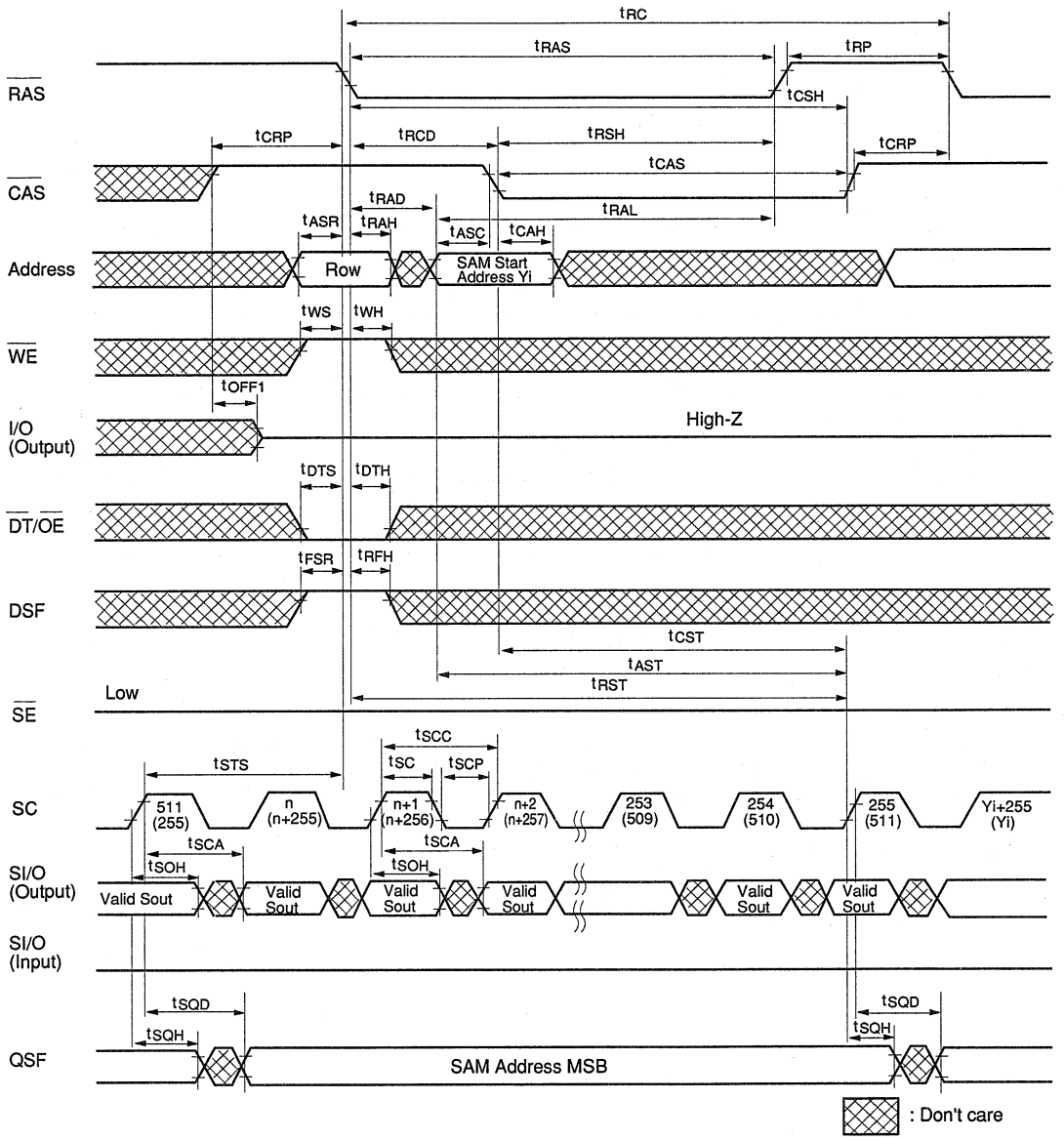
Pseudo Transfer Cycle



Write Transfer Cycle

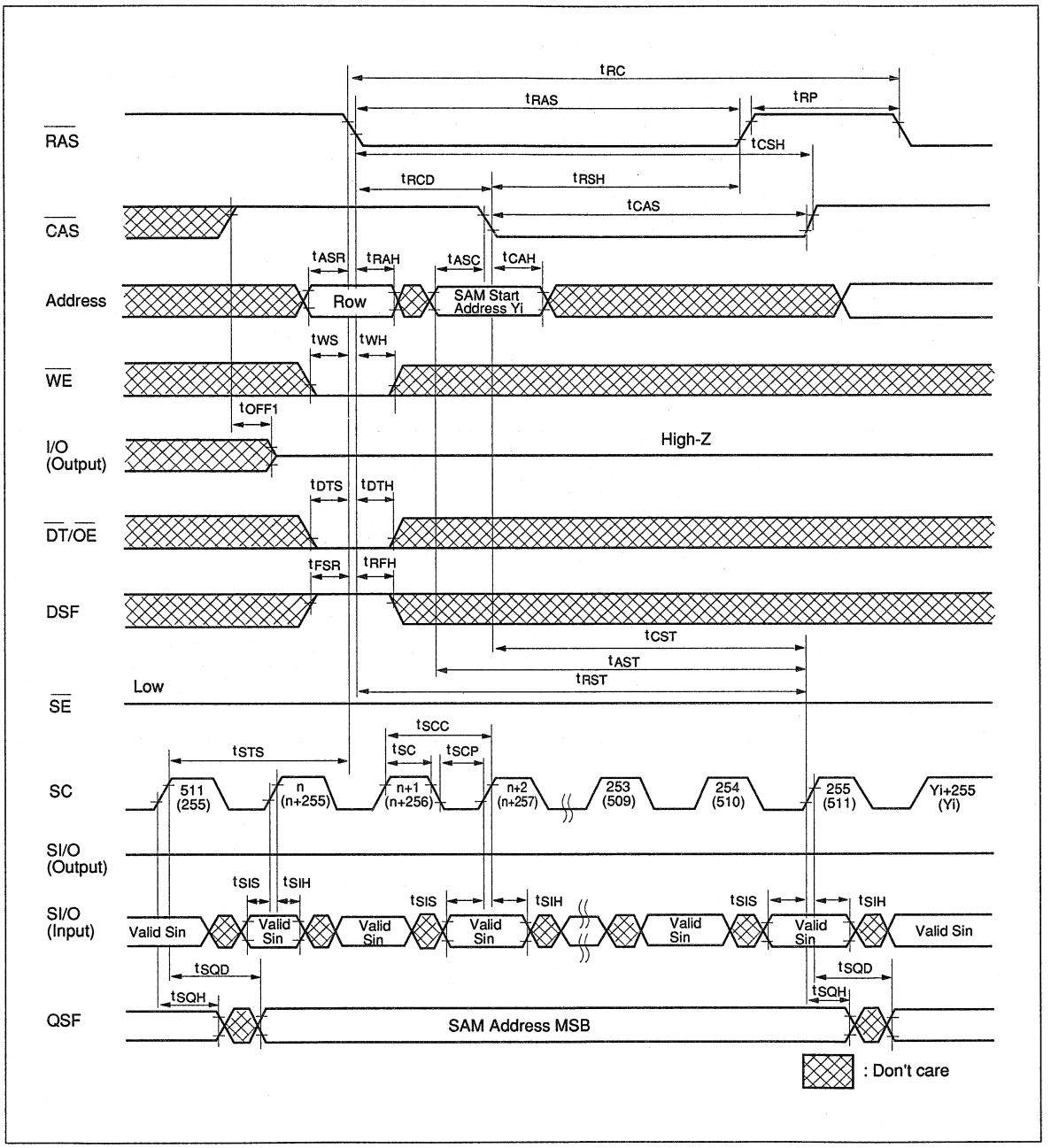


Split Read Transfer Cycle

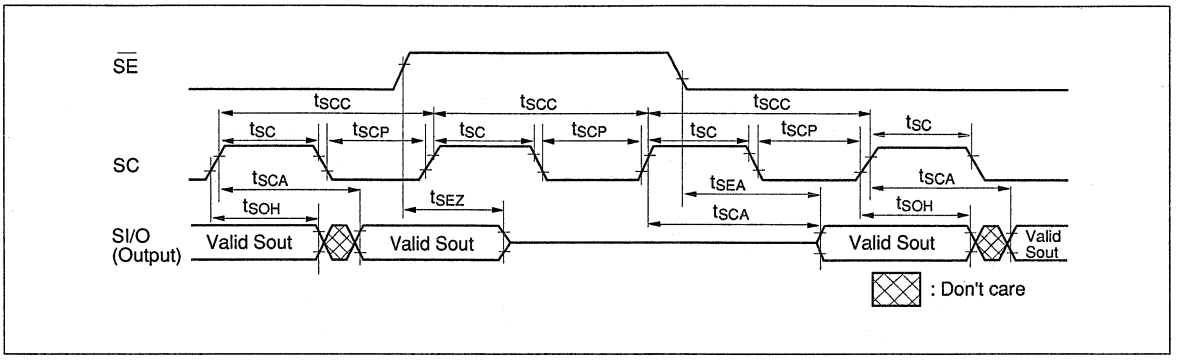


Note: 1. If the next transfer cycle after read transfer cycle is split read transfer cycle, one or more access to SC are required between read transfer cycle and split read transfer cycle.

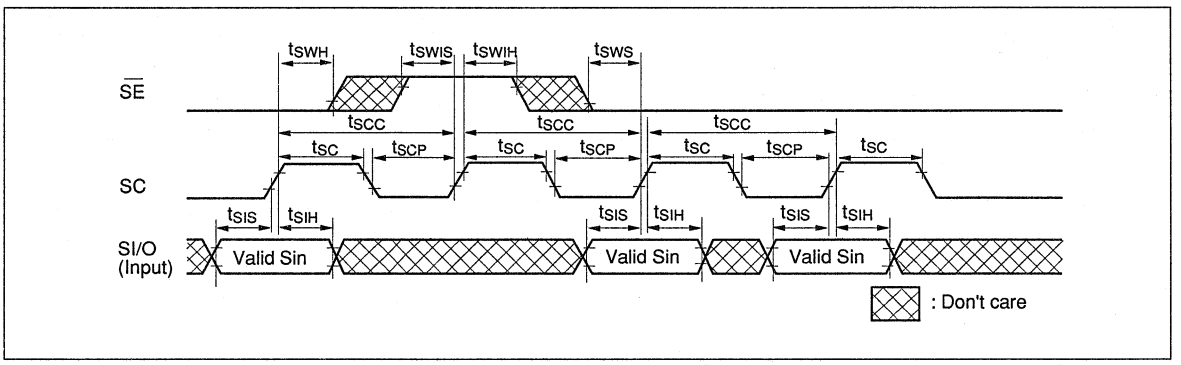
Split Write Transfer Cycle



Serial Read Cycle



Serial Write Cycle



HM538253 Series — Preliminary

262,144-word × 8-bit Multiport CMOS Video RAM

Description

The HM538253 is a 2-Mbit multiport video RAM equipped with a 256-kword × 8-bit dynamic RAM and a 512-word × 8-bit SAM (full-sized SAM). Its RAM and SAM operate independently and asynchronously. The HM538253 is upwardly compatible with the HM534253A/HM538123A except that the pseudo-write-transfer cycle is replaced with masked-write-transfer cycle, with the consent of JEDEC. Furthermore, several new features have been added to the HM538253 which do not conflict with the conventional features. The stopping column feature realizes allows greater flexibility for split SAM register lengths. Persistent mask is also installed according to the TMS34020 features.

Ordering Information

Type No.	Access Time	Package
HM538253J-7	70 ns	400-mil, 40-pin plastic SOJ (CP-40D)
HM538253J-8	80 ns	
HM538253J-10	100 ns	
HM538253TT-7	70 ns	44-pin thin small outline package (TTP-40DA)
HM538253TT-8	80 ns	
HM538253TT-10	100 ns	
HM538253RR-7	70 ns	44-pin thin small outline package (TTP-40DAR)
HM538253RR-8	80 ns	
HM538253RR-10	100 ns	

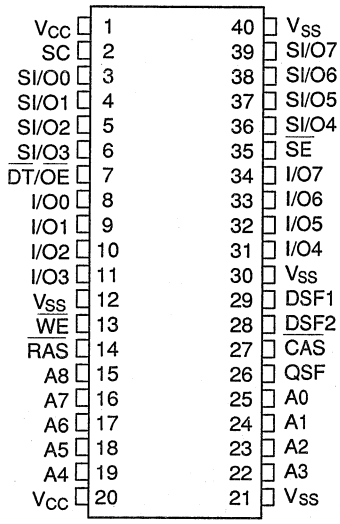
Features

- Multiport organization: RAM and SAM can operate asynchronously and simultaneously:
  - — RAM: 256 kword × 8 bit
  - — SAM: 512 word × 8 bit
- Access time
  - — RAM: 70 ns/80 ns/100 ns max
  - — SAM: 22 ns/25 ns/25 ns max
- Cycle time
  - — RAM: 135 ns/150 ns/180 ns min
  - — SAM: 25 ns/25 ns/30 ns min
- Low power
  - — Active RAM: 715 mW max
    SAM: 468 mW max
  - — Standby 38.5 mW max
- Masked-write-transfer cycle capability
- Stopping column feature capability
- Persistent mask capability
- High-speed page mode capability
- Mask write mode capability
- Bidirectional data transfer cycle between RAM and SAM capability
- Split transfer cycle capability
- Block write mode capability
- Flash write mode capability
- Three types of refresh (8 ms/512 cycles)
  - — $\overline{\text{RAS}}$-only refresh
  - — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - — Hidden refresh
- TTL compatible

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Pin Arrangement

HM538253J Series

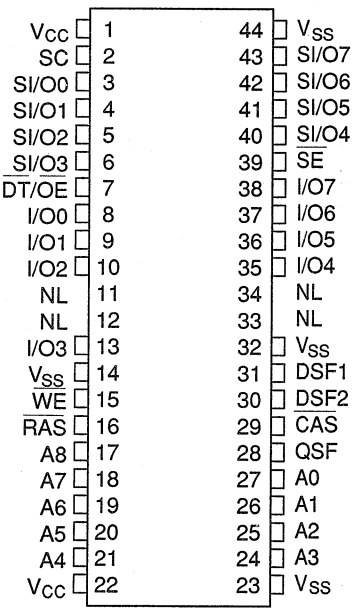


(Top view)

Pin Description

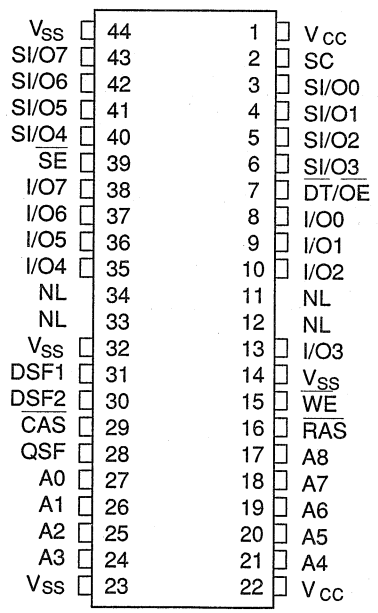
Pin name	Function
A0-A8	Address inputs
I/O0-I/O7	RAM port data inputs/outputs
SI/O0-SI/O7	SAM port data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{DT/OE}$	Data transfer/output enable
SC	Serial clock
$\overline{SE}$	SAM port enable
DSF1, DSF2	Special function input flag
QSF	Special function output flag
V_{CC}	Power supply
V_{SS}	Ground
NL	No lead

HM538253TT Series



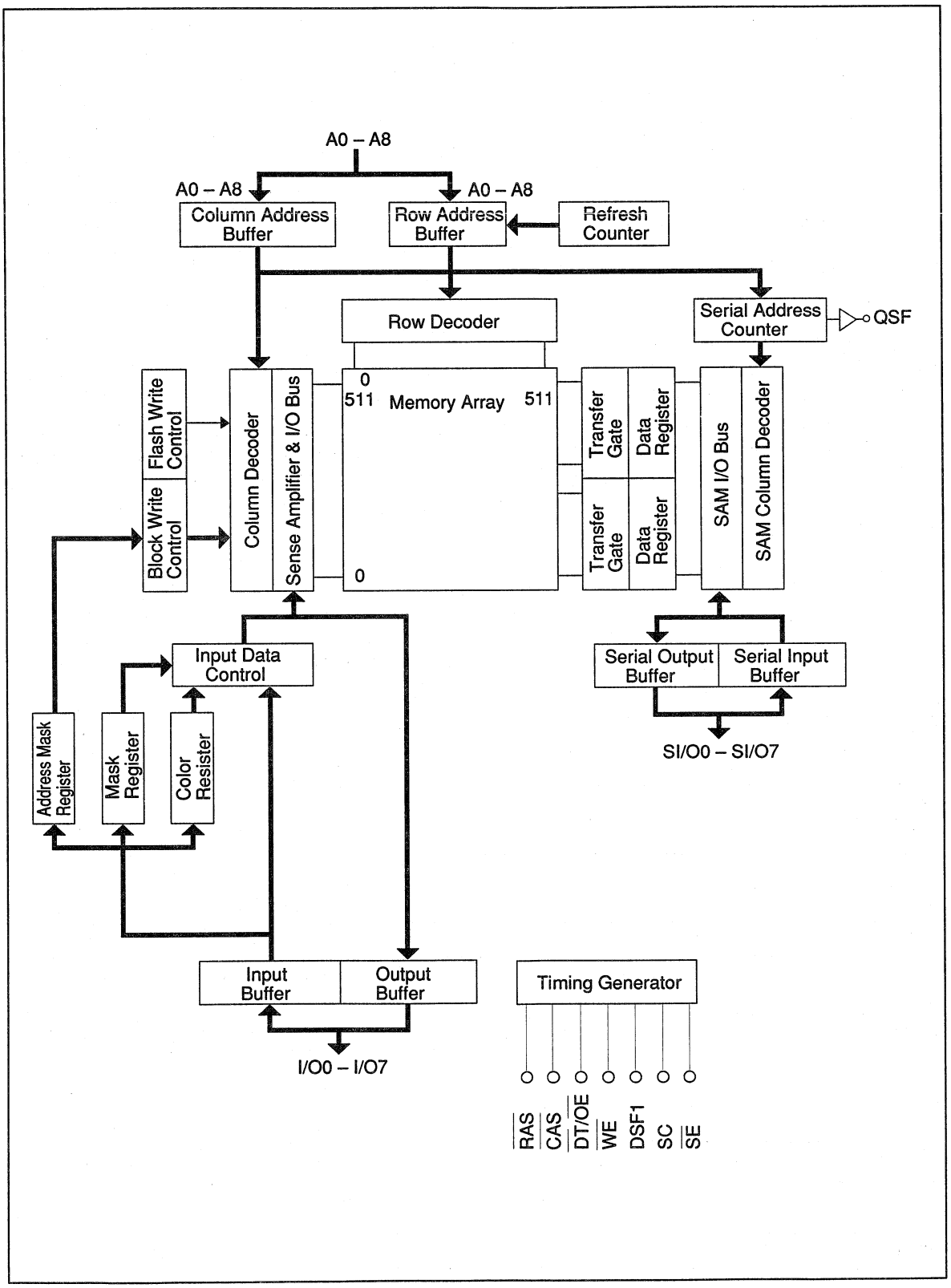
(Top view)

HM538253RR Series



(Top view)

Block Diagram



Pin Functions

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of these signals determines the operation cycle of the HM538253.

$\overline{CAS}$ (input pin): Column address and DSF1 signals are fetched into the chip at the falling edge of $\overline{CAS}$, which determines the operation mode of the HM538253. $\overline{CAS}$ controls output impedance of I/O in RAM.

A0–A8 (input pins): Row address (AX0–AX8) is determined by A0–A8 level at the falling edge of $\overline{RAS}$. Column address (AY0–AY8) is determined by A0–A8 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with the SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$: The $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM538253 turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a no mask write cycle is executed. After that, $\overline{WE}$ switches to read/write cycles. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O0–I/O7 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only to high I/O pins. Data on low I/O pins is masked and internal data is retained. After that, they function as input/output pins as those of a standard DRAM. In block write

Table 1 Operation Cycles of the HM538253

Mnemonic Code	$\overline{RAS}$					$\overline{CAS}$		Address		I/On Input	
	$\overline{CAS}$	DT/$\overline{OE}$	$\overline{WE}$	DSF1	DSF2	DSF1	DSF2	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}$/$\overline{WE}$
CBRS	0	–	0	1	0	–	0	Stop	–	–	–
CBRR	0	–	1	0	0	–	0	–	–	–	–
CBRN	0	–	1	1	0	–	0	–	–	–	–
MWT	1	0	0	0	0	–	0	Row	TAP	WM	–
MSWT	1	0	0	1	0	–	0	Row	TAP	WM	–
RT	1	0	1	0	0	–	0	Row	TAP	–	–
SRT	1	0	1	1	0	–	0	Row	TAP	–	–
RWM	1	1	0	0	0	0	0	Row	Column	WM	Input data
BWM	1	1	0	0	0	1	0	Row	Column	WM	Column Mask
RW (No)	1	1	1	0	0	0	0	Row	Column	–	Input Data
BW (No)	1	1	1	0	0	1	0	Row	Column	–	Column Mask
FWM	1	1	0	1	0	–	0	Row	–	WM	–
LMR and Old Mask Set	1	1	1	1	0	0	0	(Row)	–	–	Mask Data
LCR	1	1	1	1	0	1	0	(Row)	–	–	Color
Option	0	0	0	0	0	–	0	Mode	–	Data	–

cycle, the data functions as address mask data at the falling edges of $\overline{CAS}$ and $\overline{WE}$.

$\overline{DT}/\overline{OE}$ (input pin): The $\overline{DT}/\overline{OE}$ pin functions as a $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as an $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data outputs from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is fetched into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not fetched into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because the internal pointer is incremented at the rising edge of SC.

SI/O0–SI/O7 (input/output pins): SI/Os are SAM input/output pins. I/O direction is determined by the previous transfer cycle. If it was a read transfer cycle, SI/O outputs data. If it was a masked write transfer cycle or write transfer cycle, SI/O inputs data.

Table 1 Operation Cycles of the HM538253 (cont)

Mnemonic Code	Write Mask	Pers W.M.	Register WM	Register Color	No. of Bndry	Function
CBRS	—	—	—	—	Set	CBR refresh with stop register set
CBRR	—	Reset	Reset	—	Reset	CBR refresh with register reset
CBRN	—	—	—	—	—	CBR refresh (no reset)
MWT	Yes	No Yes	Load/use Use	—	—	Masked write transfer (new/old mask)
MSWT	Yes	No Yes	Load/use Use	—	Use	Masked split write transfer (new/old mask)
RT	—	—	—	—	—	Read transfer
SRT	—	—	—	—	Use	Split read transfer
RWM	Yes	No Yes	Load/use Use	—	—	Read/write (new/old mask)
BWM	Yes	No Yes	Load/use Use	Use	—	Block write (new/old mask)
RW (no)	No	No	—	—	—	Read/write (no mask)
BW (no)	No	No	—	Use	—	Block write (no mask)
FWM	Yes	No Yes	Load/use Use	Use	—	Masked flash write (new/old mask)
LMR and Old Mask Set	—	Set	Load	—	—	Load mask register and old mask set
LCR	—	—	—	Load	—	Load color resister set
Option	—	—	—	—	—	—

Notes: 1. With CBRS, all SAM operations use stop register.
2. After LMR, RWM, BWM, FWM, MWT, and MSWT, use old mask which can be reset by CBRR.
3. DSF2 is fixed low in all operation (for the addition of operation modes in future).

DSF1 (input pin): DSF1 is a special function data input flag pin. It is set to high at the falling edge of $\overline{RAS}$ when new functions such as color register and mask register read/write, split transfer, and flash write, are used.

DSF2 (input pin): DSF2 is also a special function data input flag pin. This pin is fixed to low level in all operations of the HM538253.

QSF (output pin): QSF outputs data of address A8 in SAM. QSF is switched from low to high by accessing address 255 in SAM, and from high to low by accessing address 511 in SAM.

RAM Port Operation

RAM Read Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF1 low at the falling edge of $\overline{RAS}$, DSF1 low at the falling edge of $\overline{CAS}$): Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM operation. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data outputs through the I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle (Early Write, Delayed Write, Read-Modify-Write) ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF1 are low at the falling edge of $\overline{RAS}$, and DSF1 is low at the falling edge of $\overline{CAS}$)

No Mask Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$): When $\overline{CAS}$ is set low and $\overline{WE}$ is set low after $\overline{RAS}$ low, a write cycle is executed. If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and all I/O become in high impedance. If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$): If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, two modes of mask write cycle are possible.

In new mask mode, mask data is loaded and used. Whether or not an I/O is written depends on I/O level at the falling edge of $\overline{RAS}$. The data is written in high level I/Os, and the data is masked and retained in low level I/Os. This mask data is effective during the $\overline{RAS}$ cycle. So, in page mode cycles the mask data is retained during the page access.

If a load mask register cycle (LMR) has been performed, the mask data is not loaded from I/O pins and the mask data stored in mask registers persistently are used. This operation is known as persistent write mask, set by LMR cycle and reset by CBRR cycle.

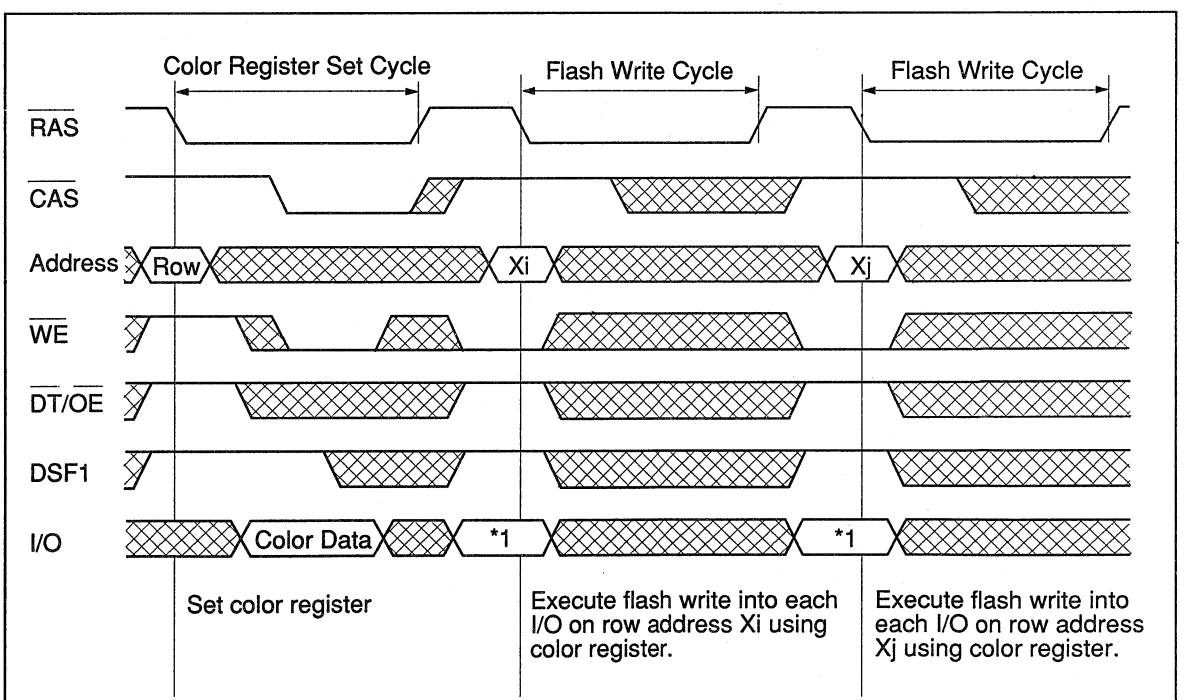
High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF1 low at the falling edge of $\overline{RAS}$): High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle. In this cycle, read, write, and block write cycles can be mixed. Note that address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 512-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 µs).

Color Register Set/Read Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high, $\overline{WE}$ high and DSF1 high at the falling edge of $\overline{RAS}$): In color register set cycle, color data is set to the internal color register used in flash write cycle or block write cycle. 8 bits of internal color register are provided at each I/O. This register is composed of static circuits, so once it is set, it retains the data until reset. Since color register set cycle is the same as the usual read and write cycle, so read, early write, and delayed write cycle can be executed. In this cycle, the HM538253 refreshes the row address fetched at the falling edge of $\overline{RAS}$.

Mask Register Set/Read Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high, $\overline{WE}$ high, and DSF1 low at the falling edge of $\overline{RAS}$): In mask register set cycle, mask data is set to the internal mask register used in mask write cycle, block write cycle, flash write cycle, masked write transfer, and masked split write transfer. 8 bits of internal mask register are provided at each I/O. This mask register is composed of static circuits, so once it is set, it retains the data until reset. Since mask register set cycle is just the same as the usual read and write cycle, so read, early write, and delayed write cycle can be executed.

Flash Write Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high, $\overline{WE}$ low, and DSF1 high at the falling edge of $\overline{RAS}$): In a flash write cycle, a row of data (512 word × 8 bit) is cleared to 0 or 1 at each I/O according to the data in the color register mentioned before. It is also necessary to mask I/O in this cycle. When $\overline{CAS}$ and $\overline{DT}/\overline{OE}$ is set high, $\overline{WE}$ is low, and DSF1 is high at the falling edge of $\overline{RAS}$, this cycle starts. Then, the row address to clear is given to row address. Mask data is the same as that of a RAM write cycle. Cycle time is the same as those of RAM read/write cycles, so all bits can be cleared in 1/512 of the usual cycle time. (See figure 1.)

Block Write Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high and DSF1 low at the falling edge of $\overline{RAS}$, DSF1 high at the falling edge of $\overline{CAS}$ and $\overline{WE}$): In a block write cycle, 4 columns of data (4 word × 8 bit) is cleared to 0 or 1 at each I/O according to the data of color register. Column addresses A0 and A1 are disregarded. The data on I/Os and addresses can be masked. I/O level at the falling edge of $\overline{CAS}$ determines the address to be cleared. (See figure 2.) Block write cycle is as the same as the usual write cycle, so early and delayed write, read-modify-write, and page mode write cycle can be executed.

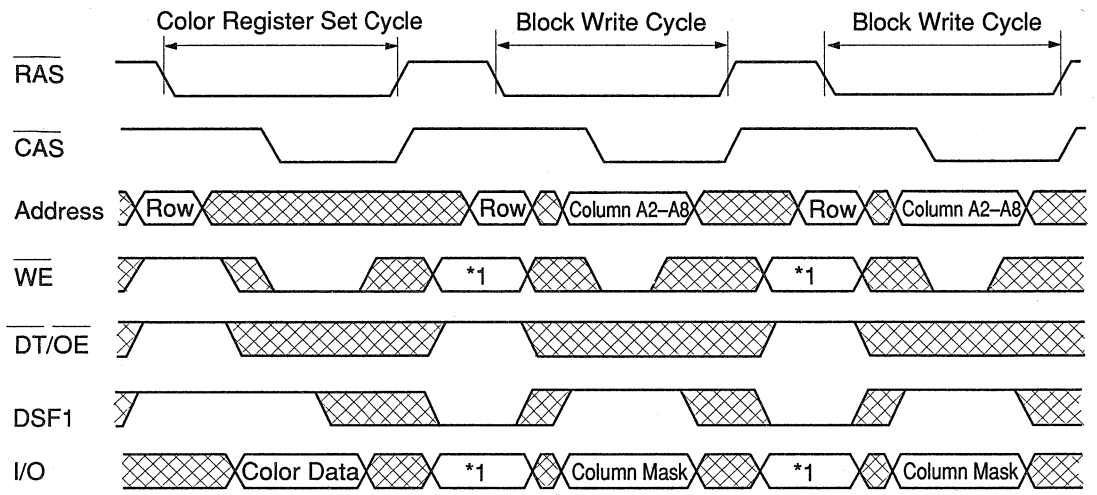


Note: 1. I/O Mask Data (In new mask mode)
Low: Mask
High: Non Mask
In persistent mask mode, I/O don't care

Figure 1 Use of Flash Write

No Mask Mode Block Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$): The data on 8 I/Os are all cleared when $\overline{WE}$ is high at the falling edge of $\overline{RAS}$.

Mask Block Write Cycle ($\overline{WE}$ low at the falling edge of $\overline{RAS}$): When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM538253 starts mask block write cycle to clear the data on an optional I/O. The mask data is the same as that of a RAM write cycle.



*1

$\overline{WE}$	Mode	I/O data/$\overline{RAS}$
Low	New mask mode	Mask
	Persistent mask mode	Don't care (mask register used)
High	No mask	Don't care

I/O Mask Data (In new mask mode)

Low: Mask

High: Non Mask

In persistent mask mode, I/O don't care

Column Mask Data

I/O0	Column0 (A0 = 0, A1 = 0) Mask Data	Low: Mask High: Non Mask
I/O1	Column1 (A0 = 1, A1 = 0) Mask Data	
I/O2	Column2 (A0 = 0, A1 = 1) Mask Data	
I/O3	Column3 (A0 = 1, A1 = 1) Mask Data	

Figure 2 Use of Block Write

Transfer Operation

The HM538253 provides the read transfer cycle, split read transfer cycle, masked write transfer cycle and masked split write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{CAS}$ high and $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:

- Transfer data between row address and SAM data register
  - —Read transfer cycle and split read transfer cycle: RAM to SAM
  - —Masked write transfer cycle and masked split write transfer cycle: SAM to RAM
- Determine SI/O state
  - —Read transfer cycle: SI/O output
  - —Masked write transfer cycle: SI/O input
- Determine first SAM address to access after transferring at column address (SAM start address).
  - —SAM start address must be determined by read transfer cycle or masked write transfer cycle (split transfer cycle isn't available) before SAM access, after power on, and determined for each transfer cycle.
- Use the stopping columns (boundaries) in the serial shift register. If the stopping columns have been set, split transfer cycles use the stopping columns, but any boundaries cannot be set as the start address.
- Load/use mask data in masked write transfer cycle and masked split write transfer cycle.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high and DSF1 low at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by driving $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high and DSF1 low at the falling edge of $\overline{RAS}$. The row address data (512 × 8 bits) determined by this cycle is transferred to SAM data register synchronously at the rising edge of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address determined by column address. In read transfer cycle, $\overline{DT}/\overline{OE}$ must rise to transfer data from RAM to SAM.

This cycle can access SAM even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge and t_{SDH} (min) specified between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge must be satisfied. (See figure 3.)

When read transfer cycle is executed, SI/O becomes output state by first SAM access. Input must be set high impedance before t_{SZS} (min) of the first SAM access to avoid data contention.

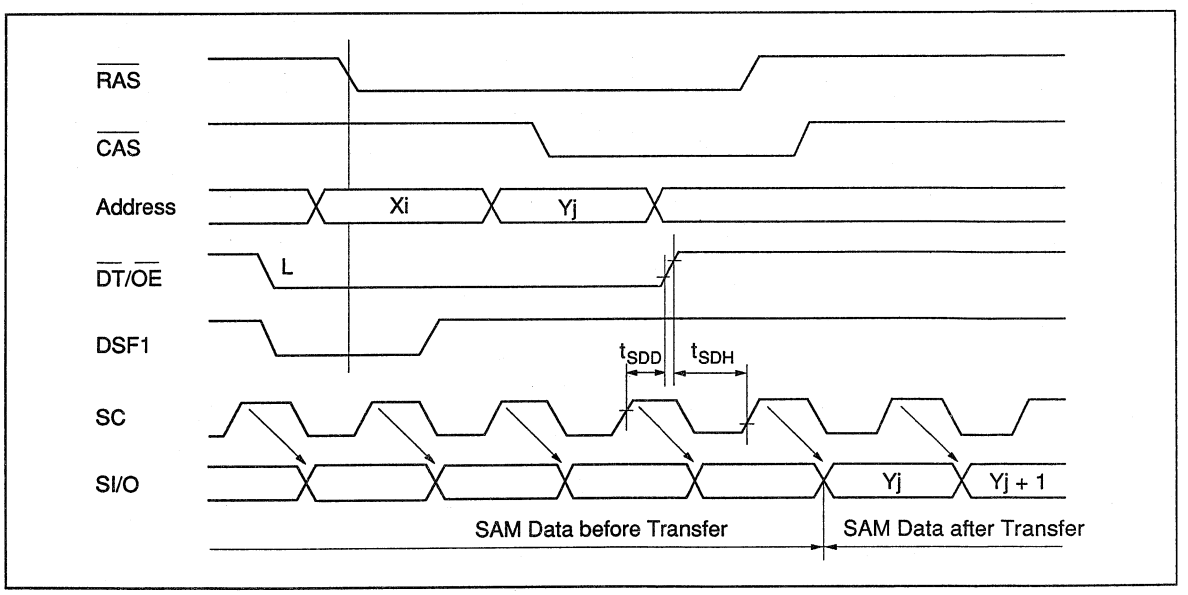


Figure 3 Real Time Read Transfer

Masked Write Transfer cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and DSF1 low at the falling edge of $\overline{RAS}$): Masked write transfer cycle can transfer only selected I/O data in a row of data input by serial write cycle to RAM. Whether I/O data is transferred or not depends on the corresponding I/O level (mask data) at the falling edge of $\overline{RAS}$. This mask transfer operation is the same as a mask write operation in RAM cycles, so the persistent mode can be supported.

The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address for serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC must not be risen.

Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addresses of RAM by write transfer cycle. However, the address to write data must be the same as that of the read transfer cycle or the split read transfer cycle (row address AX8)

Split Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ high and DSF1 high at the falling edge of $\overline{RAS}$): To execute a continuous serial read by real-time read transfer, the HM538253 must satisfy SC and $\overline{DT/OE}$ timings and requires an external circuit to detect SAM last address. Split read transfer cycle makes it possible to execute a continuous serial read without the above timing limitation.

The HM538253 supports two types of split register operation. One is the normal split register operation to split the data register into two halves. Another is the boundary split register operation using stopping columns described later.

Figure 4 shows the block diagram for the normal split register operation. SAM data register (DR) consists of 2 split buffers, whose organizations are 256-word × 8-bit each. Suppose that data is read from upper data register DR1. (The row address AX8 is 0 and SAM address A8 is 1.) When split read transfer is executed setting row address AX8 0 and SAM start addresses A0 to A7, 256-word × 8-bit data is transferred from RAM to the lower data register DR0 (SAM address A8 is 0) automatically. After data is read from data register

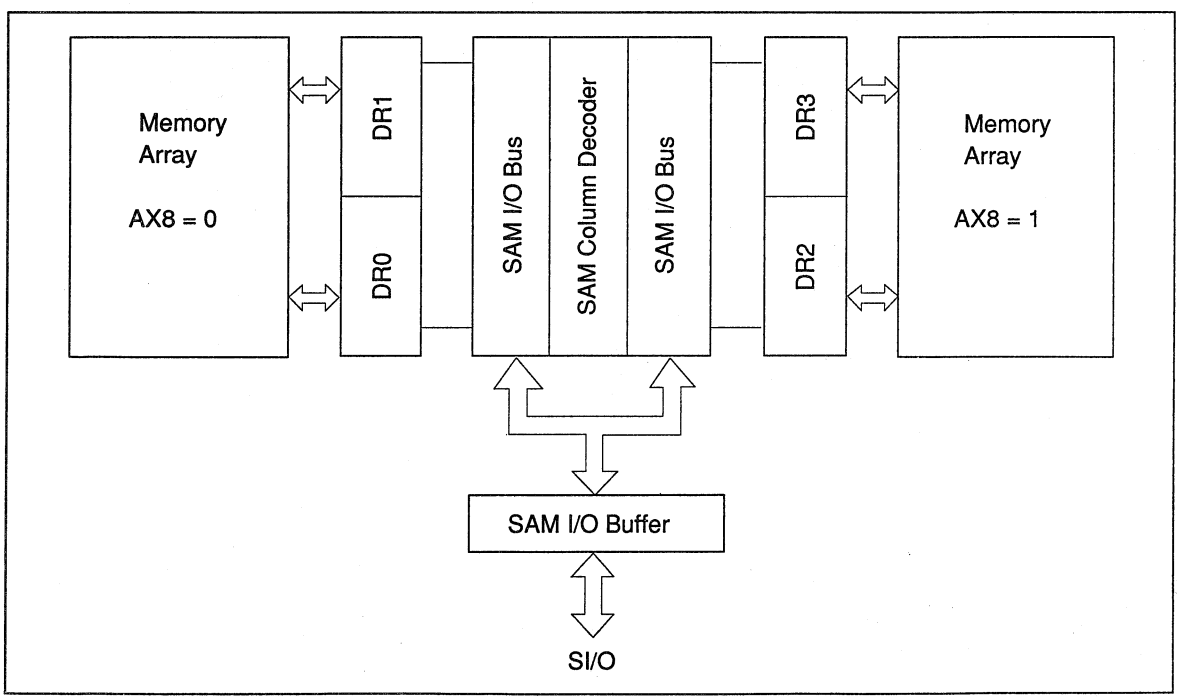


Figure 4 Split Transfer Block Diagram

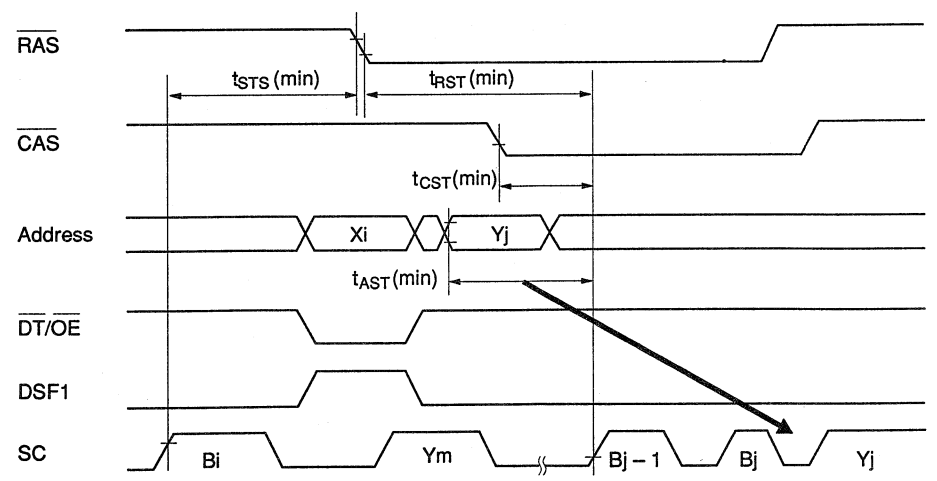
DR1, data read begins from SAM start addresses of data register DR0. If the next split read transfer isn't executed while data is read from data register DR0, data read begins from SAM start address 0 of DR1 after data is read from data register DR0. If split read transfer is executed setting row address AX8 1 and SAM start addresses A0 to A7 while data is read from data register DR1, 256-word × 8-bit data is transferred to data register DR2. After data is read from data register DR1, data read begins from the SAM start addresses of data register DR2. If the next split read transfer isn't executed while data is read from data register DR2, data read begins from SAM start address 0 of data register DR1 after data is read from data register DR2. In split read data transfer, the SAM start address A8 is automatically set in the data register, which isn't used.

The data on SAM address A8, which will be accessed next, outputs to QSF. QSF is switched from low to high by accessing SAM last address 255 and from high to low by accessing address 511.

Split read transfer cycle is set when $\overline{CAS}$ is high, $\overline{DT/OE}$ is low, $\overline{WE}$ is high and DSF1 is high at the falling edge of $\overline{RAS}$. The cycle can be executed asyncronously with SC. However, HM538253 must be satisfied t_{STS} (min) timing specified between SC rising (boundary address) and $\overline{RAS}$ falling. In split transfer cycle, the HM538253 must satisfy t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings specified between $\overline{RAS}$ or $\overline{CAS}$ falling and column address. (See figure 5.)

In split read transfer, SI/O isn't switched to output state. Therefore, read transfer must be executed to switch SI/O to output state when the previous transfer cycle is masked write transfer cycle or masked split write transfer cycle.

Masked Split Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low and DSF1 high at the falling edge of $\overline{RAS}$): A continuous serial write cannot be executed because accessing SAM is inhibited during $\overline{RAS}$ low in write transfer. Masked split write transfer cycle makes it possible. In this cycle, t_{STS} (min), t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings must be satisfied like split read transfer cycle. And it is impossible to switch SI/O to input state in this cycle. If SI/O is in output state, masked write transfer cycle should be executed to switch SI/O into input state. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addresses of RAM by split write transfer cycle. However, in this split write transfer cycle, the MSB of row address (AX8) to write data must be the same as that of the read transfer cycle or the



Note: Ym is the SAM start address in before SRT. Bi and Bj initiate the boundary address.

Figure 5 Split Transfer Limitation

split read transfer cycle. In this cycle, the boundary split register operation using stopping columns is possible as with split read transfer cycle.

Stopping Column in Split Transfer Cycle: The HM538253 has the boundary split register operation using stopping columns. If a CBRS cycle has been performed, split transfer cycle performs the boundary operation. Figure 6 shows an example of boundary split register. (Boundary code is B7.)

First a read data transfer cycle is executed, and SAM start addresses A0 to A8 are set. The RAM data is transferred to the lower SAM, and SAM serial read starts from the start address (Y1) on the lower SAM. After that, a split read transfer cycle is executed, and the next start address (Y2) is set. The RAM data is transferred to the upper SAM. When the serial read arrive at the first boundary after the split read transfer cycle, the next read jumps to the start address (Y2) on the upper SAM (jump 1) and continues. Then the second split read transfer cycle is executed, and another start address

Table 2 Stopping Column Boundary Table

		Stop Address					
Boundary code	**Column size**	**A2**	**A3**	**A4**	**A5**	**A6**	**A7**
B2	4	0	*	*	*	*	*
B3	8	1	0	*	*	*	*
B4	16	1	1	0	*	*	*
B5	32	1	1	1	0	*	*
B6	64	1	1	1	1	0	*
B7	128	1	1	1	1	1	0
B8	256	1	1	1	1	1	1

Notes: 1. A0, A1, and A8: don't care
2. *: don't care

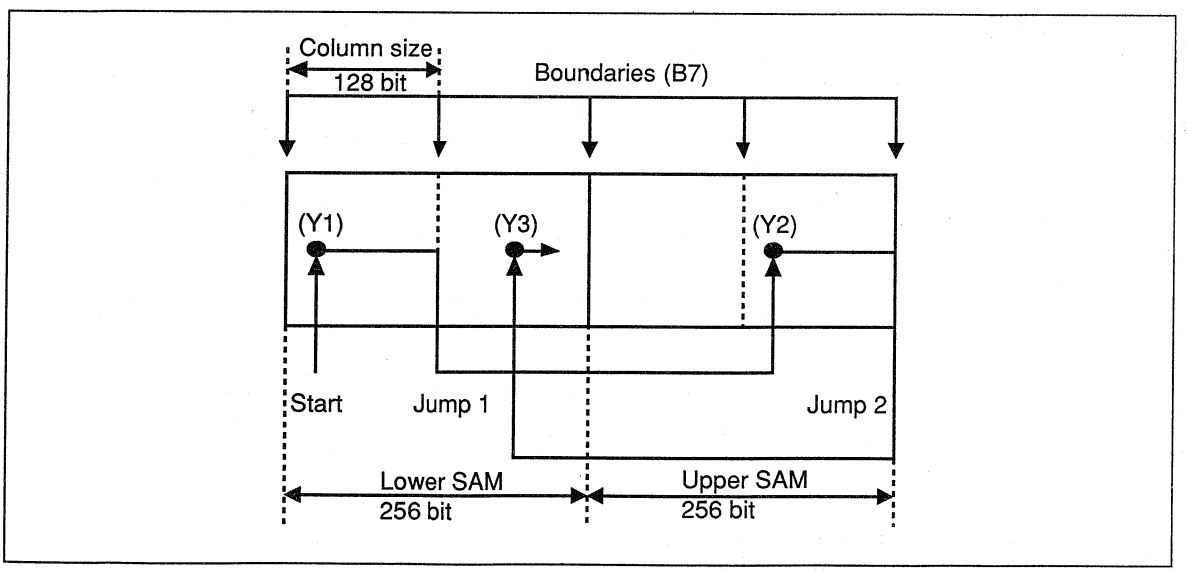


Figure 6 Example of Boundary Split Register

(Y3) is set. The RAM data is transferred to the lower SAM. When the serial read arrive at the other boundary again, the next read jumps to the start address (Y3) on the lower SAM.

Stopping Column Set Cycle (CBRS): Start a stopping column set cycle by driving $\overline{CAS}$ low, $\overline{WE}$ low, and DSF1 high at the falling edge of $\overline{RAS}$. Stopping column data (boundaries) are latched from address inputs on the falling edge of $\overline{RAS}$. To determine the boundary, A2 to A7 can be used, and A0, A1, and A8 are don't care. In the HM538253, 7 types of boundary (B2 to B8) can be set including the default case. (See stopping column boundary table.) If A2 to A6 are set low and A7 is set high, the boundaries (B7) are selected. Figure 6 shows the example. Once a CBRS is executed, the stopping column operation mode continues until CBRR.

Register Reset Cycle (CBRR): Start a register reset cycle (CBRR) by driving $\overline{CAS}$ low, $\overline{WE}$ high, and DSF1 low at the falling edge of $\overline{RAS}$. A CBRR can reset the persistent mask operation and stopping column operation. When a CBRR is executed for stopping column operation reset, it need to satisfy t_{STS} (min) and t_{RST} (min) between $\overline{RAS}$ falling and SC rising.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is a read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When $\overline{SE}$ is set high, SI/O becomes high impedance, and the internal pointer is incremented by the SC rising. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

Serial Write Cycle

If the previous data transfer cycle is a masked write transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is fetched into the data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't fetched into data register. The internal pointer is incremented by the SC rising, so $\overline{SE}$ high can be used as mask data for SAM. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh cycles to retain data. Refresh is executed by accessing all 512 row addresses within 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBRN, CBRS, and CBRR) refresh cycle, and (3) Hidden refresh cycle. The cycles which activate $\overline{RAS}$, such as read/write cycles or transfer cycles, can also refresh the row address. Therefore, no refresh cycle is required when all row addresses are accessed within 8 ms.

$\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is executed by activating only the $\overline{RAS}$ cycle with $\overline{CAS}$ fixed high after inputting the row address (refresh address) from external circuits. To distinguish this cycle from a data transfer cycle, $\overline{DT}/\overline{OE}$ must be high at the falling edge of $\overline{RAS}$.

CBR Refresh Cycle: CBR refresh cycle (CBRN, CBRS and CBRR) are set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, the refresh address need not be input through external circuits because it is input through an internal refresh counter. In this cycle, output is high impedance and power dissipation is low or because $\overline{CAS}$ circuits are not operating.

Hidden Refresh Cycle: Hidden refresh cycle executes CBR refresh with the data output by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift resister and selector), organized as fully static circuitry, require no refresh.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	–0.5*2	—	0.8	V	1

Notes: 1. All voltage referenced to V_{SS}
2 –3.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM538253								
		-7		-8		-10				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	
Operating current	I_{CC1}	—	120	—	105	—	90	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC7}	—	190	—	160	—	140	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Standby current	I_{CC2}	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC8}	—	85	—	70	—	70	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
$\overline{RAS}$-only refresh current	I_{CC3}	—	120	—	105	—	90	mA	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH} t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC9}	—	190	—	160	—	140	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Page mode current	I_{CC4}	—	130	—	115	—	100	mA	$\overline{CAS}$ cycling $\overline{RAS}$ = V_{IL} t_{PC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10}	—	200	—	170	—	150	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	—	95	—	85	—	70	mA	$\overline{RAS}$ cycling t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC11}	—	165	—	140	—	120	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (cont)

		HM538253								
		-7		-8		-10				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	
Data transfer current	I_{CC6}	—	130	—	115	—	100	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC12}	—	200	—	170	—	150	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA		
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA		
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	V	I_{OH} = –1 mA	
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	V	I_{OL} = 2.1 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once while $\overline{RAS}$ is low and $\overline{CAS}$ is high.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%, f = 1 MHz, Bias: Clock, I/O = V_{CC}, address = V_{SS})

Parameter	Symbol	Typ	Max	Unit	Note
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	5	pF	1
Output capacitance (I/O, SI/O, QSF)	$C_{I/O}$	—	7	pF	1

Notes: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) *1, *16

Test Conditions

- Input rise and fall times: 5 ns
- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: RAM 1 TTL + CL (50 pF)
  SAM 1 TTL + CL (30 pF)
  (Including scope and jig)

Common Parameter

		HM538253							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	135	—	150	—	180	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	55	—	60	—	70	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	—	20	—	25	—	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	20	75	ns	2
$\overline{RAS}$ hold time referenced to $\overline{CAS}$	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	
Transition time (rise to fall)	t_T	3	50	3	50	3	50	ns	3
Refresh period	t_{REF}	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ setup time	t_{DTS}	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ hold time	t_{DTH}	10	—	10	—	10	—	ns	
DSF1 to $\overline{RAS}$ setup time	t_{FSR}	0	—	0	—	0	—	ns	
DSF1 to $\overline{RAS}$ hold time	t_{RFH}	10	—	10	—	10	—	ns	
DSF1 to $\overline{CAS}$ setup time	t_{FSC}	0	—	0	—	0	—	ns	
DSF1 to $\overline{CAS}$ hold time	t_{CFH}	15	—	15	—	15	—	ns	
Data-in to $\overline{CAS}$ delay time	t_{DZC}	0	—	0	—	0	—	ns	4
Data-in to $\overline{OE}$ delay time	t_{DZO}	0	—	0	—	0	—	ns	4

Common Parameter (cont)

		HM538253							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Output buffer turn-off delay referenced to $\overline{CAS}$	t_{OFF1}	—	20	—	20	—	20	ns	5
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	—	20	—	20	—	20	ns	5

Read Cycle (RAM), Page Mode Read Cycle

		HM538253							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	40	—	45	ns	7, 9
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns	10
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	10
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	2
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	35	—	40	—	45	—	ns	
Page mode cycle time	t_{PC}	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	7	—	10	—	10	—	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	—	45	—	50	ns	
Page mode $\overline{RAS}$ pulse width	t_{RASP}	70	100000	80	100000	100	100000	ns	

Write Cycle (RAM), Page Mode Write Cycle, Color Register Set Cycle

		HM538253							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	11
Write command hold time	t_{WCH}	15	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	15	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	15	—	15	—	15	—	ns	12
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	10	—	10	—	10	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	10	—	10	—	10	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	20	—	20	—	20	—	ns	
Page mode cycle time	t_{PC}	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	7	—	10	—	10	—	ns	
$\overline{CAS}$ to data-in delay time	t_{CDD}	20	—	20	—	20	—	ns	13
Page mode $\overline{RAS}$ pulse width	t_{RASP}	70	100000	80	100000	100	100000	ns	

Read-Modify-Write Cycle

		HM538253							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	185	—	200	—	230	—	ns	
$\overline{RAS}$ pulse width (read-modify-write cycle)	t_{RWS}	120	10000	130	10000	150	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	45	—	45	—	50	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	60	—	65	—	70	—	ns	14
$\overline{OE}$ to data-in delay time	t_{ODD}	20	—	20	—	20	—	ns	12
Access time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	40	—	45	ns	7, 9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	15	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	15	—	15	—	15	—	ns	12
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	20	—	20	—	20	—	ns	

Refresh Cycle

		HM538253							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	

Flash Write Cycle, Block Write Cycle, and Register Read Cycle

		HM538253							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ to data-in delay time	t_{CDD}	20	—	20	—	20	—	ns	13
$\overline{OE}$ to data-in delay time	t_{ODD}	20	—	20	—	20	—	ns	13

CBR Refresh with Register Reset

		HM538253							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Split transfer setup time	t_{STS}	20	—	20	—	25	—	ns	
Split transfer hold time referenced to $\overline{RAS}$	t_{RST}	70	—	80	—	100	—	ns	

Read Transfer Cycle

		HM538253							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{DT}$ hold time referenced to $\overline{RAS}$	t_{RDH}	60	10000	65	10000	80	10000	ns	
$\overline{DT}$ hold time referenced to $\overline{CAS}$	t_{CDH}	20	—	20	—	25	—	ns	
$\overline{DT}$ hold time referenced to column address	t_{ADH}	25	—	30	—	30	—	ns	
$\overline{DT}$ precharge time	t_{DTP}	20	—	20	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ delay time	t_{DRD}	65	—	70	—	80	—	ns	
SC to $\overline{RAS}$ setup time	t_{SRS}	25	—	30	—	30	—	ns	
1st SC to $\overline{RAS}$ hold time	t_{SRH}	70	—	80	—	100	—	ns	
1st SC to $\overline{CAS}$ hold time	t_{SCH}	25	—	25	—	25	—	ns	
1st SC to column address hold time	t_{SAH}	40	—	45	—	50	—	ns	
Last SC to $\overline{DT}$ delay time	t_{SDD}	5	—	5	—	5	—	ns	
1st SC to $\overline{DT}$ hold time	t_{SDH}	10	—	15	—	15	—	ns	
$\overline{DT}$ to QSF delay time	t_{DQD}	—	35	—	35	—	35	ns	7
QSF hold time referenced to $\overline{DT}$	t_{DQH}	5	—	5	—	5	—	ns	
Serial data-in to 1st SC delay time	t_{SZS}	0	—	0	—	0	—	ns	
Serial clock cycle time	t_{SCC}	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	
$\overline{RAS}$ to QSF delay time	t_{RQD}	—	70	—	75	—	85	ns	
$\overline{CAS}$ to QSF delay time	t_{CQD}	—	35	—	35	—	35	ns	
QSF hold time referenced to $\overline{RAS}$	t_{RQH}	20	—	20	—	25	—	ns	
QSF hold time referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	5	—	ns	

Masked Write Transfer Cycle

Parameter	Symbol	HM538253 -7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Notes
SC setup time referenced to $\overline{RAS}$	t_{SRS}	25	—	30	—	30	—	ns	
$\overline{RAS}$ to SC delay time	t_{SRD}	20	—	25	—	25	—	ns	
Serial output buffer turn-off time referenced to $\overline{RAS}$	t_{SRZ}	10	40	10	45	10	50	ns	
$\overline{RAS}$ to serial data-in delay time	t_{SID}	40	—	45	—	50	—	ns	
$\overline{RAS}$ to QSF delay time	t_{RQD}	—	70	—	75	—	85	ns	7
$\overline{CAS}$ to QSF delay time	t_{CQD}	—	35	—	35	—	35	ns	7
QSF hold time referenced to $\overline{RAS}$	t_{RQH}	20	—	20	—	25	—	ns	
QSF hold time referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	5	—	ns	
Serial clock cycle time	t_{SCC}	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	

Split Read Transfer Cycle, Masked Split Write Transfer Cycle

		HM538253							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Split transfer setup time	t_{STS}	20	—	20	—	25	—	ns	
Split transfer hold time referenced to $\overline{RAS}$	t_{RST}	70	—	80	—	100	—	ns	
Split transfer hold time referenced to $\overline{CAS}$	t_{CST}	20	—	20	—	25	—	ns	
Split transfer hold time referenced to column address	t_{AST}	35	—	40	—	45	—	ns	
SC to QSF delay time	t_{SQD}	—	30	—	30	—	30	ns	7
QSF hold time referenced to SC	t_{SQH}	5	—	5	—	5	—	ns	
Serial clock cycle time	t_{SCC}	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	

Serial Read Cycle, Serial Write Cycle

		HM538253							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Serial clock cycle time	t_{SCC}	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	ns	
Access time from SC	t_{SCA}	—	22	—	25	—	25	ns	15
Access time from $\overline{SE}$	t_{SEA}	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial output buffer turn-off time referenced to $\overline{SE}$	t_{SHZ}	—	20	—	20	—	20	ns	5,17
$\overline{SE}$ to serial output in low-Z	t_{SLZ}	0	—	0	—	0	—	ns	5,17
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	

Serial Read Cycle, Serial Write Cycle (cont)

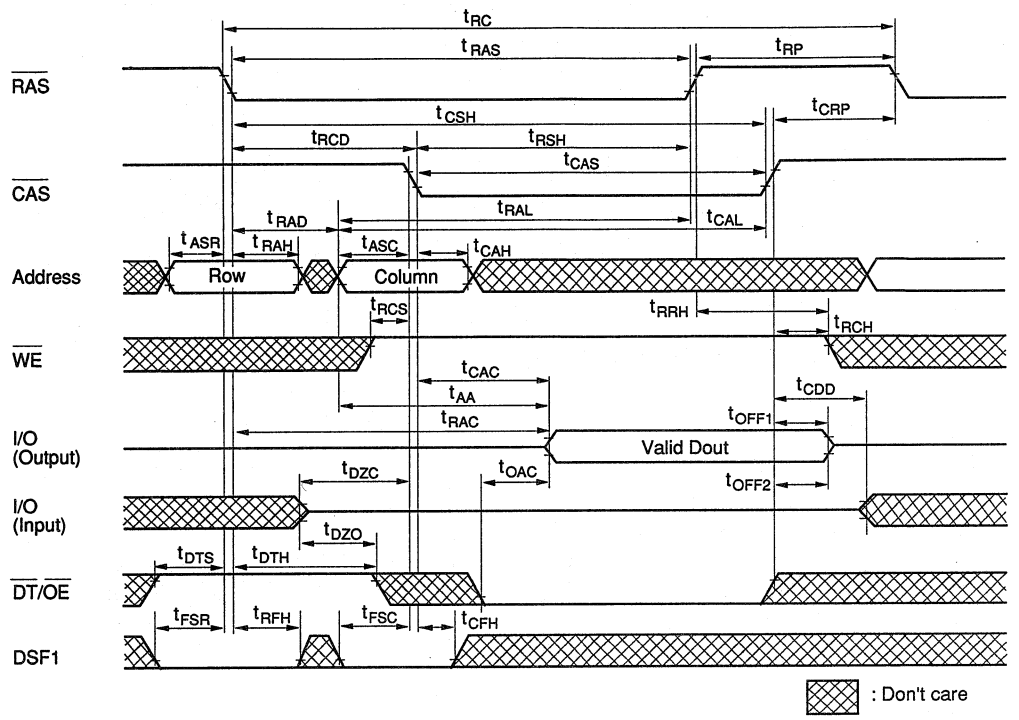
		HM538253							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	
Serial write enable setup time	t_{SWS}	0	—	0	—	0	—	ns	
Serial wrtie enable hold time	t_{SWH}	15	—	15	—	15	—	ns	
Serial write disable setup time	t_{SWIS}	0	—	0	—	0	—	ns	
Serial write disable hold time	t_{SWIH}	15	—	15	—	15	—	ns	

Notes: 1. AC measurements assume t_T = 5 ns.

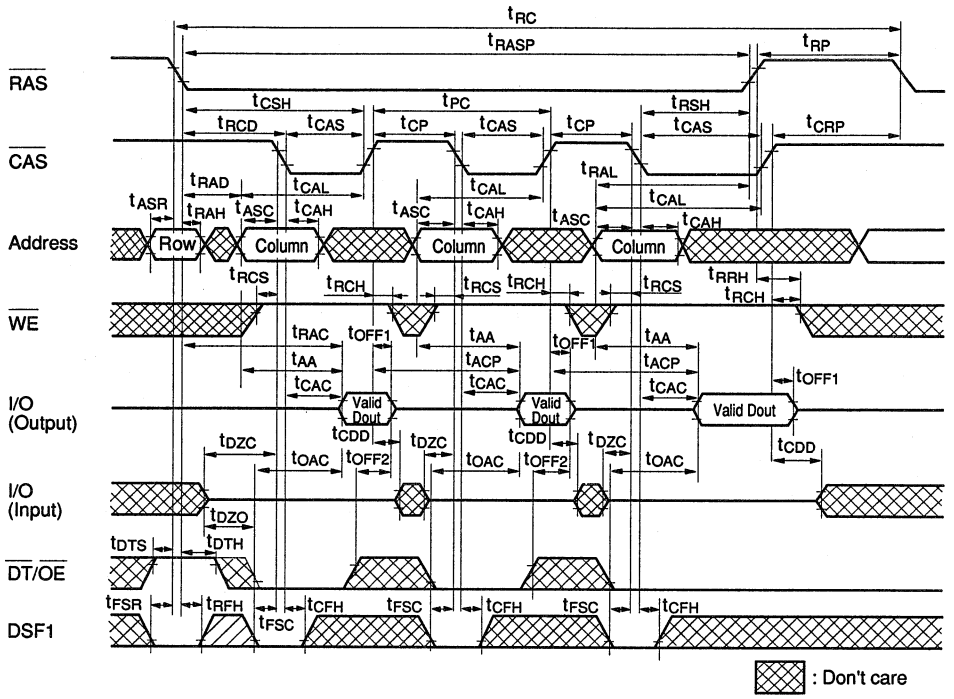
2. When $t_{RCD} > t_{RCD}$ (max) and $t_{RAD} > t_{RAD}$ (max), access time is specified by t_{CAC} or t_{AA}.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition time t_T is measured between V_{IH} and V_{IL}.
4. Data input must be floating before output buffer is turned on. In read cycle, read-modify-write cycle and delayed write cycle, either t_{DZC} (min) or t_{DZO} (min) must be satisfied.
5. t_{OFF1} (max), t_{OFF2} (max), t_{SHZ} (max) and t_{SLZ} (min) are defined as the time at which the output acheives the open circuit condition (V_{OH} – 100 mV, V_{OL} + 100 mV). This parameter is sampled and not 100% tested.
6. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 1 TTL loads and 50 pF.
8. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
9. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
10. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.
11. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
12. These parameters are specified by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
13. Either t_{CDD} (min) or t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{CAS}$ or $\overline{OE}$ prior to applying data to the device when output buffer is on.
14. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min) in read-modify-write cycle, the data of the selected address outputs to an I/O pin and input data is written into the selected address. t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{OE}$ prior to applying data to the device.
15. Measured with a load circuit equivalent to 1 TTL loads and 30 pF.
16. After power-up, pause for 100 µs or more and execute at least 8 initialization cycle (normal memory cycle or refresh cycle), then start operation. Hitachi recommends that 8 initialization cycle is CBRR for internal register reset.
17. When t_{SHZ} and t_{SLZ} are measured in the same V_{CC} and Ta condition and tr and tf of $\overline{SE}$ are less than 5 ns, $t_{SHZ} < t_{SLZ} + 5$ ns.

Timing Waveforms

Read Cycle



Page Mode Read Cycle



Write Cycle

Table 3 below applies to early write, delayed write, page mode write, and read-modify write.

Table 3 Write Cycle State

Menu	Cycle	$\overline{RAS}$ DSF1 W1	$\overline{CAS}$ DSF1 W2	$\overline{RAS}$ $\overline{WE}$ W3	$\overline{RAS}$ I/O W4	$\overline{CAS}$ I/O W5
RWM	Write mask (new/old) Write DQs to I/Os	0	0	0	Write mask*1	Valid data
BWM	Write mask (new/old) Block write	0	1	0	Write mask*2	Column mask*2
RW	Normal write (no mask)	0	0	1	Don't care*1	Valid data
BW	Block write (no mask)	0	1	1	Don't care*2	Column mask*2
LMR	Load write mask resister	1	0	1	Don't care	Write mask data*3
LCR	Load color resister	1	1	1	Don't care	Color data

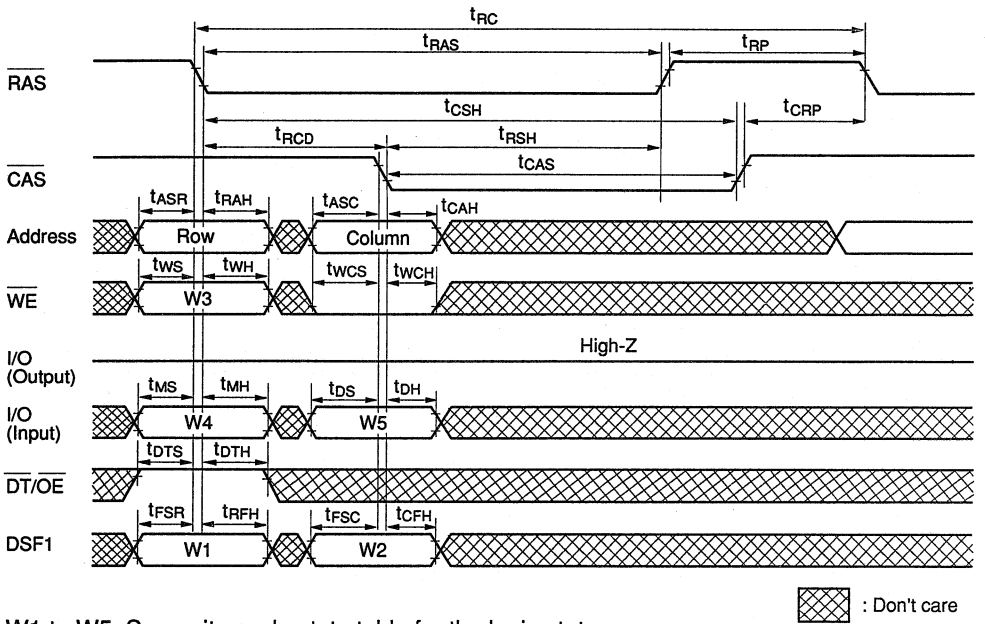
Notes: 1.

$\overline{WE}$	Mode	I/O data/$\overline{RAS}$
Low	New mask mode	Mask
	Persistent mask mode	Don't care (mask register used)
High	No mask	Don't care

I/O Mask data (In new mask mode)
Low: Mask
High: Non mask
In persistent mask mode, I/O don't care

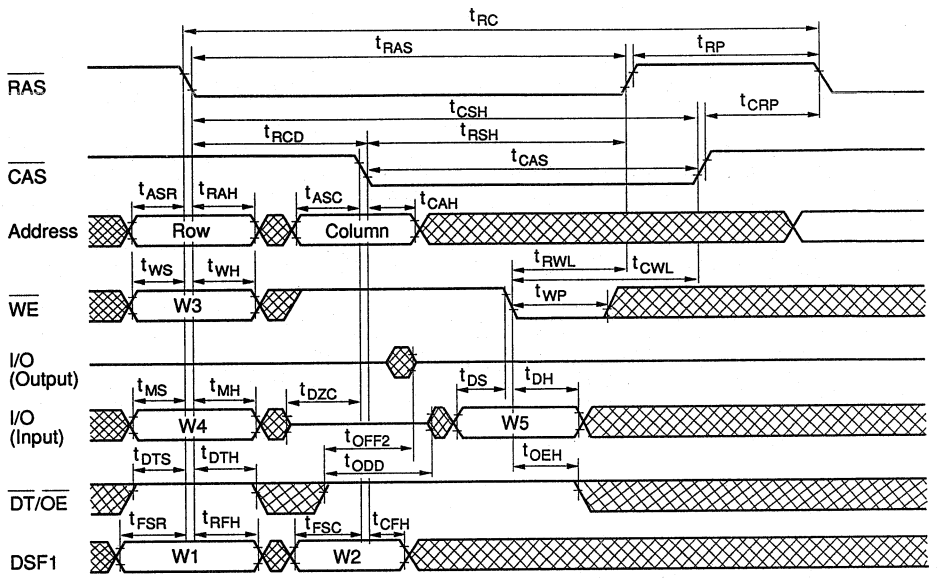
2. Reference Figure 2 use of block write.
3. I/O write mask data
Low: Mask
High: Non mask

Early Write Cycle



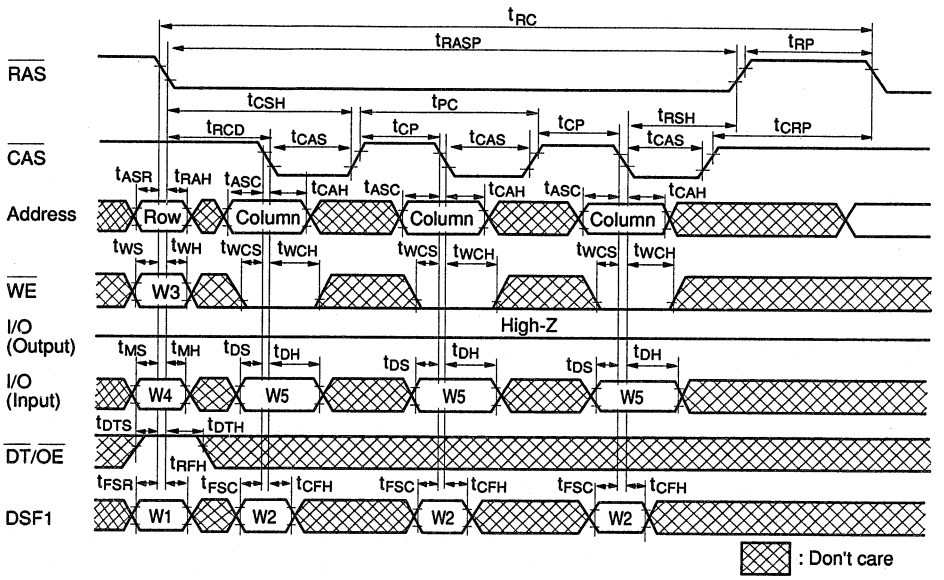
W1 to W5: See write cycle state table for the logic states.

Delayed Write Cycle



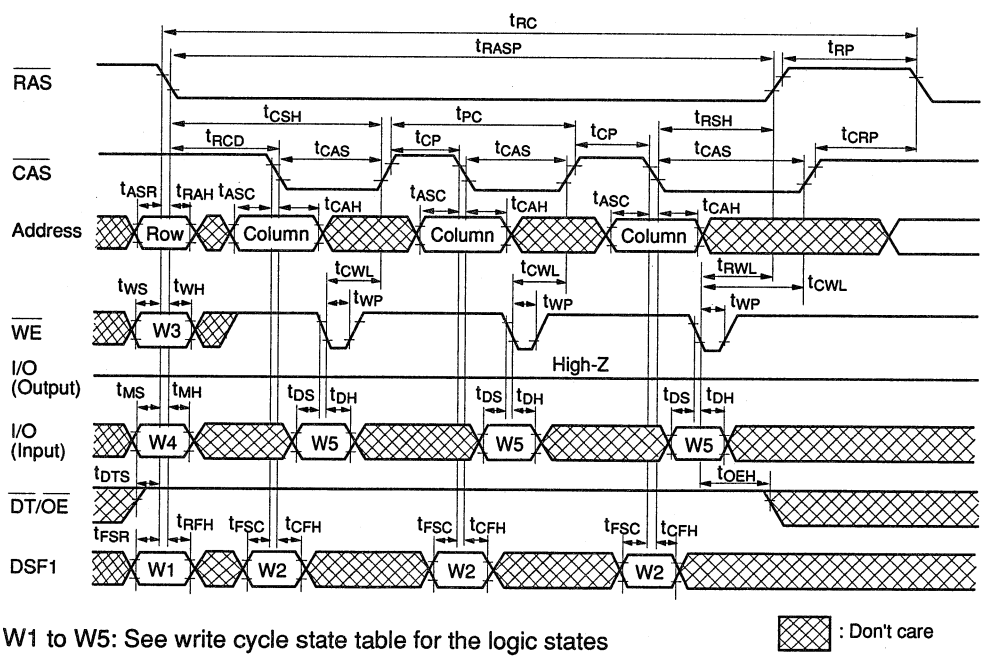
W1 to W5: See write cycle state table for the logic states

Page Mode Write Cycle (Early Write)



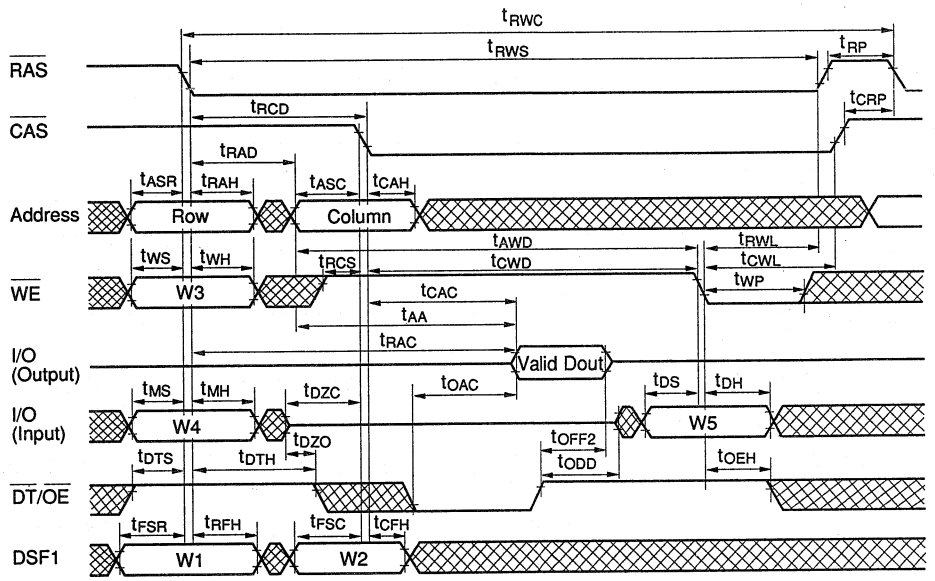
W1 to W5: See write cycle state table for the logic states

Page Mode Write Cycle (Delayed Write)



W1 to W5: See write cycle state table for the logic states

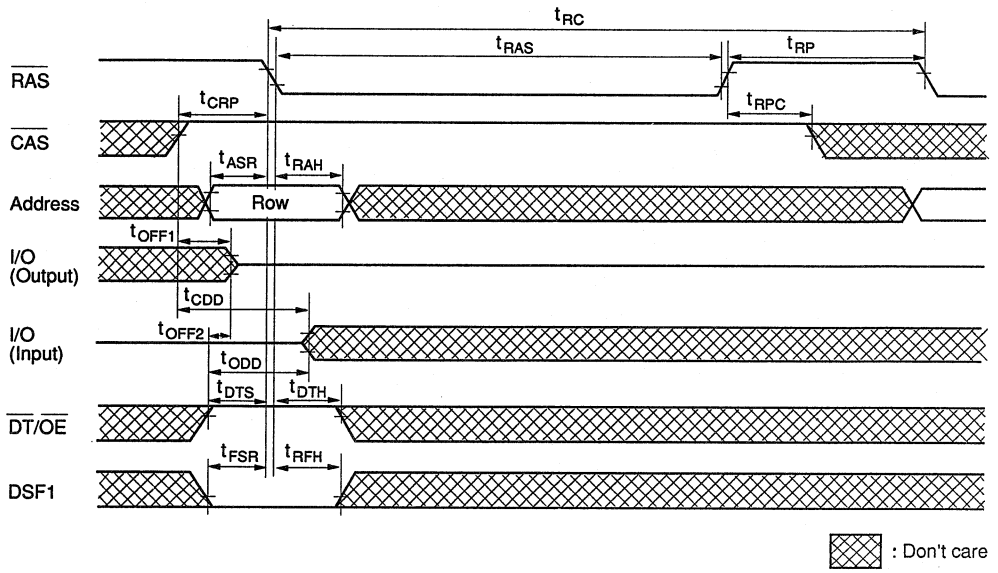
Read-Modify-Write Cycle



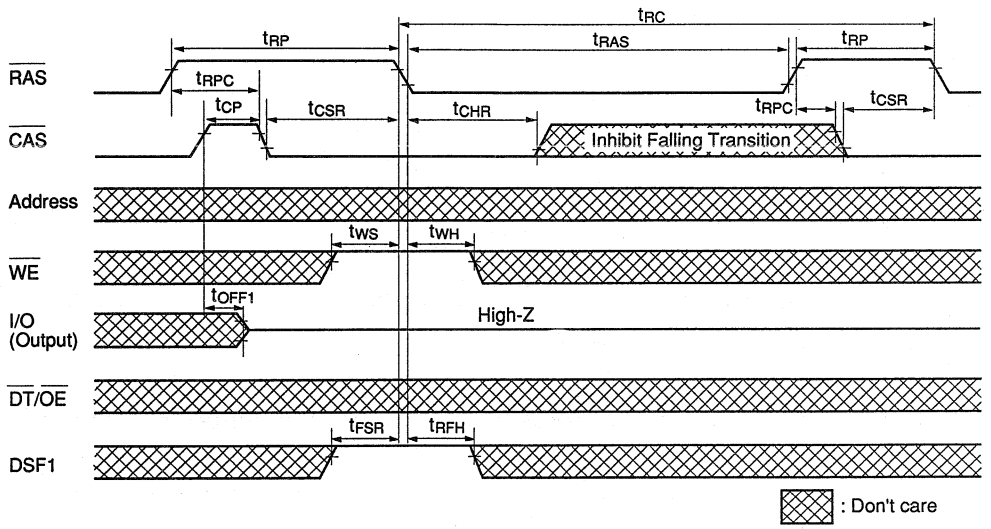
W1 to W5: See write cycle state table for the logic states

: Don't care

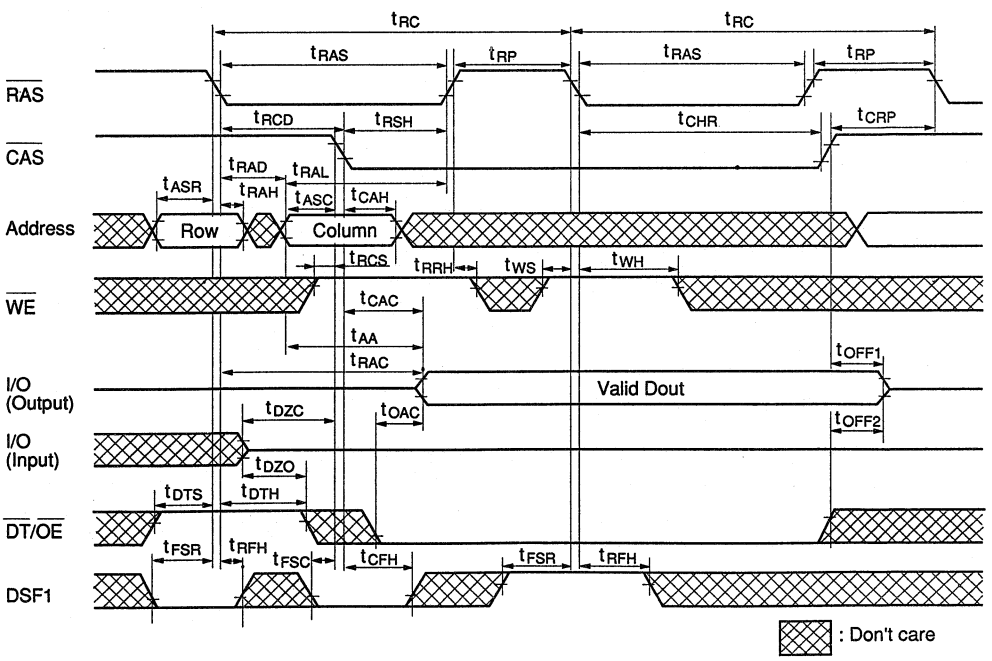
$\overline{\text{RAS}}$-Only Refresh Cycle



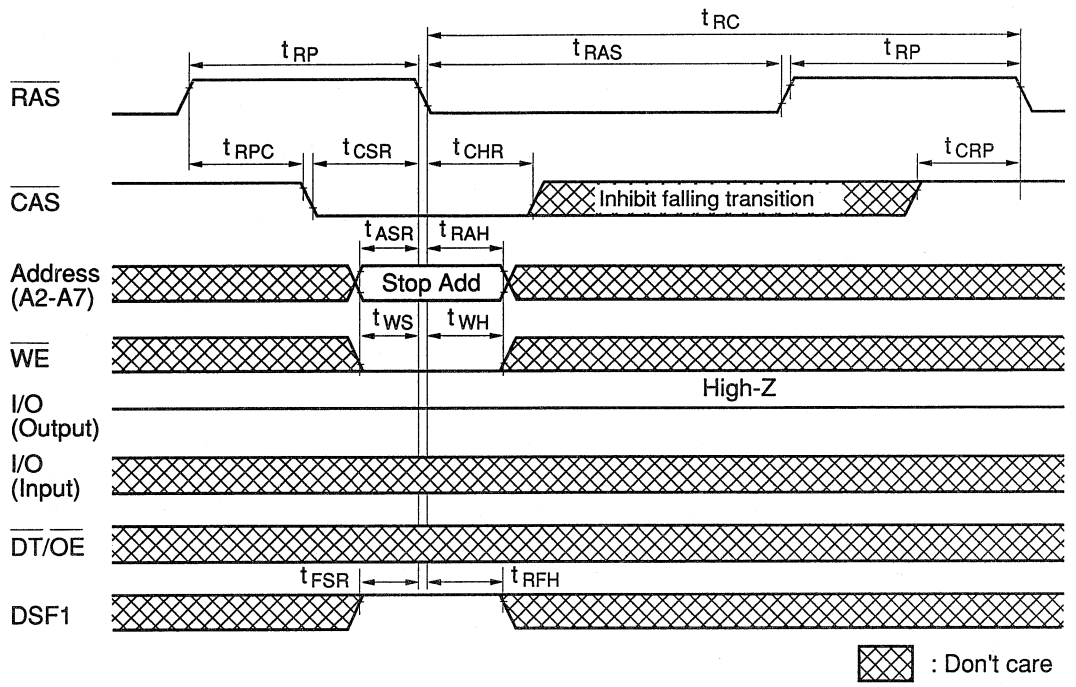
CAS-Before-RAS Refresh Cycle (CBRN)



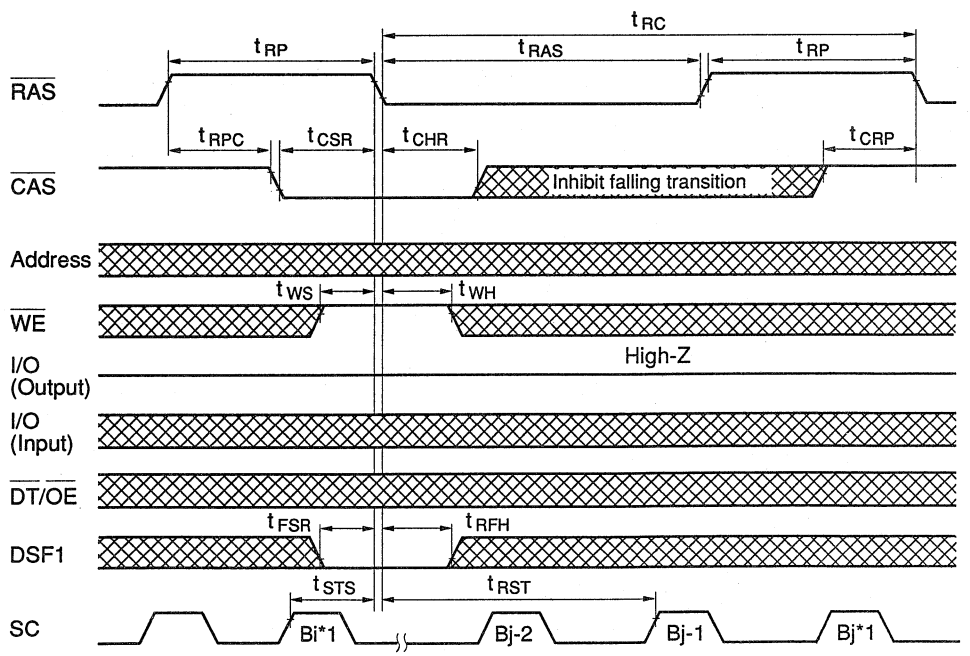
Hidden Refresh Cycle



CAS-Before-RAS Set Cycle (CBRS)

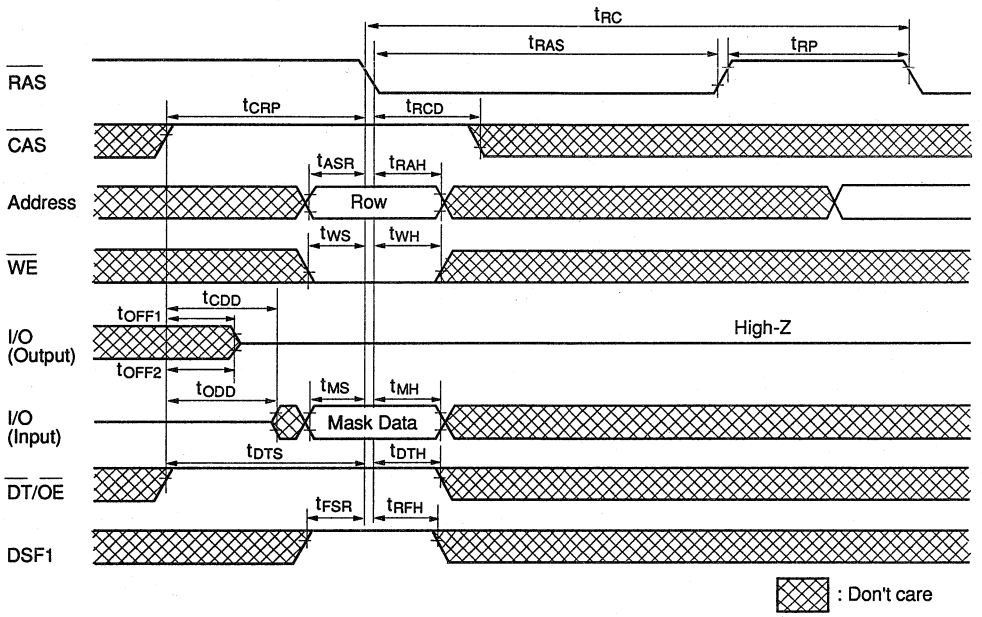


CAS-Before-RAS Reset Cycle (CBRR)

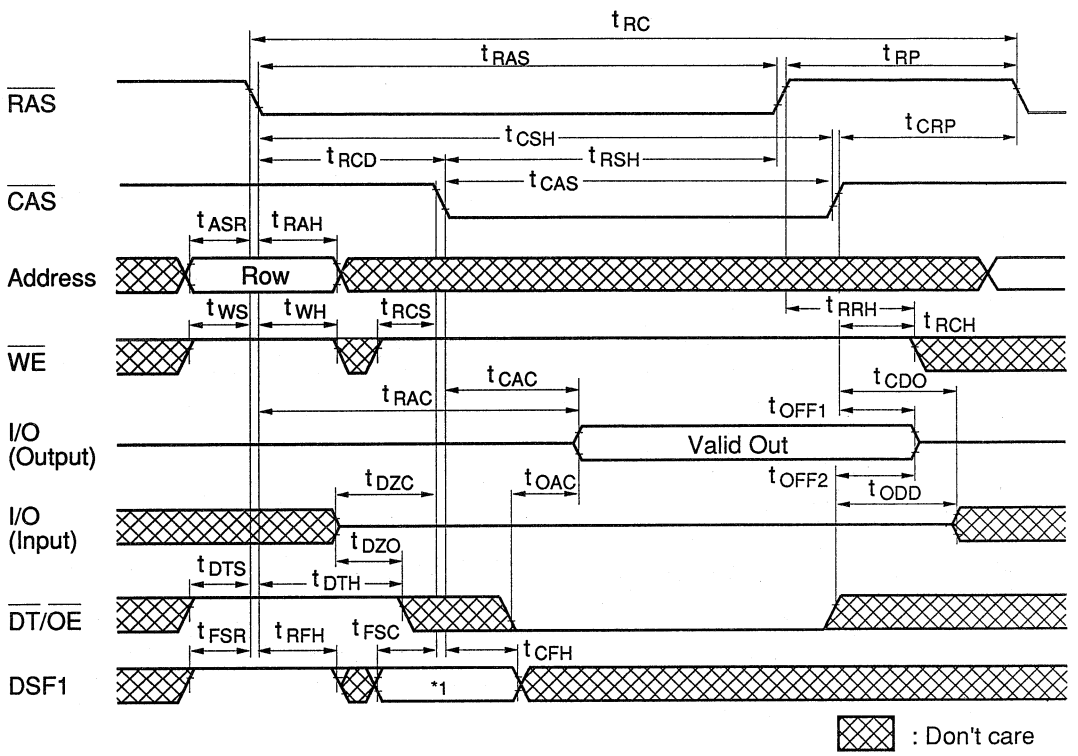


Note: 1. Bi, Bj initiate the boundary addresses.

Flash Write Cycle



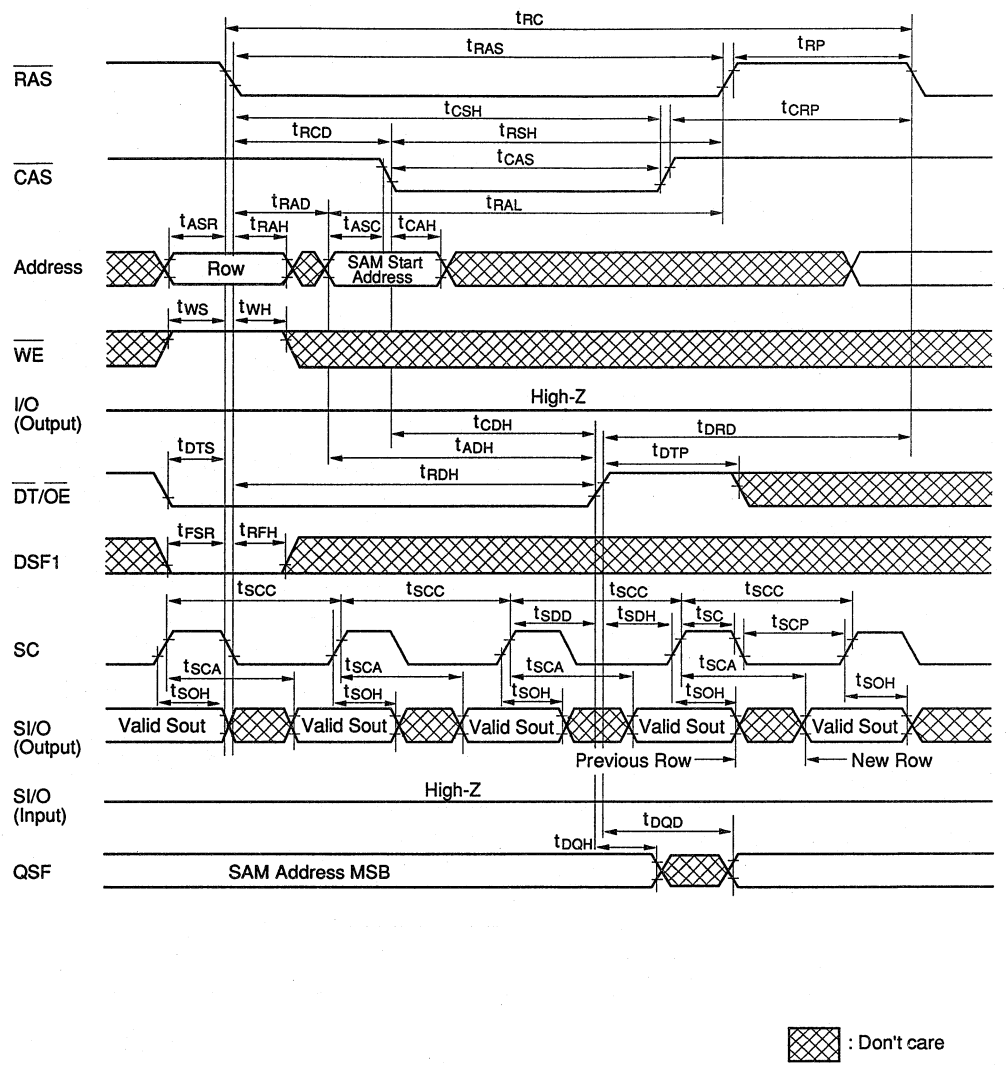
Register Read Cycle (Mask data, Color data)



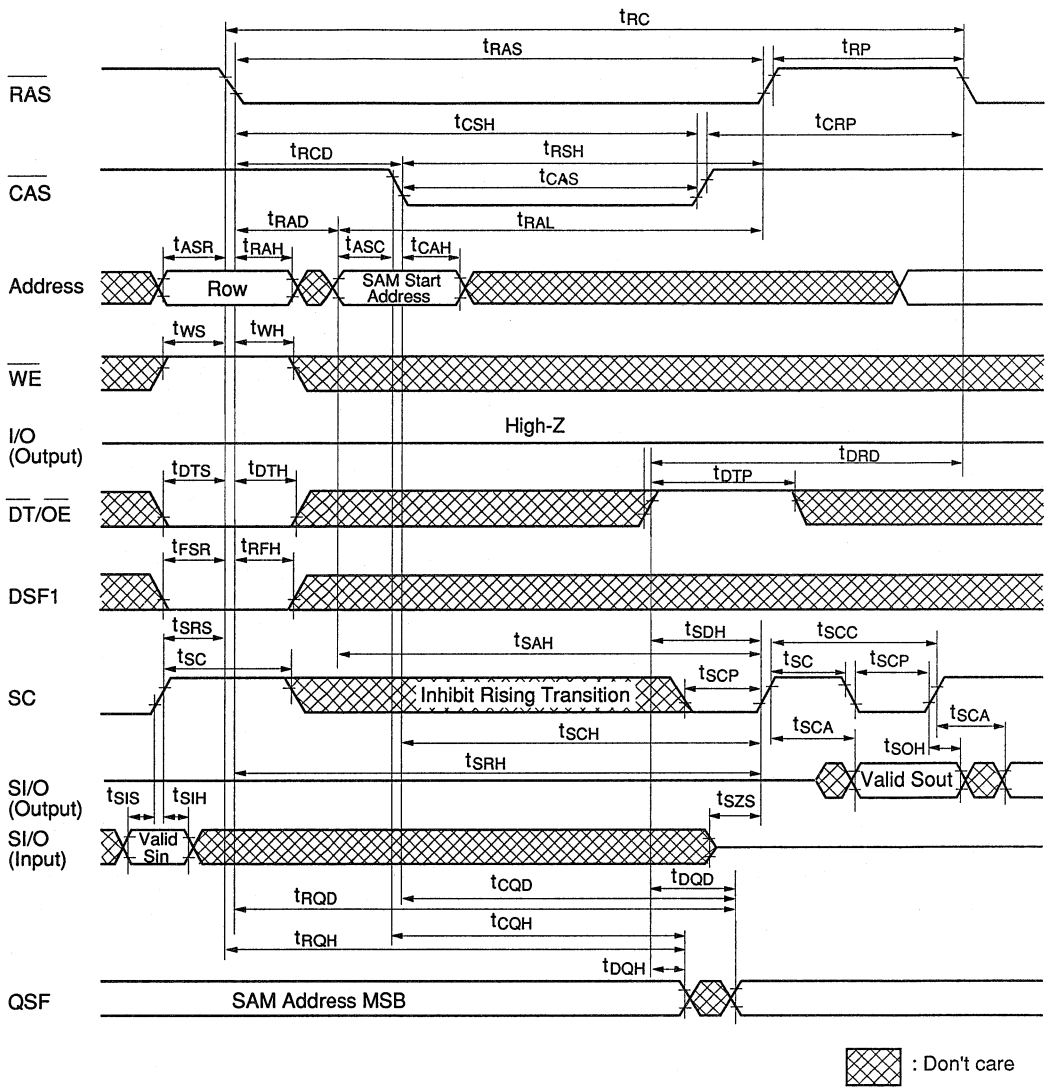
Note: 1. State of DSF1 at falling edge of $\overline{CAS}$

State	0	1
Accessed data	Mask data (LMR)	Color data (LCR)

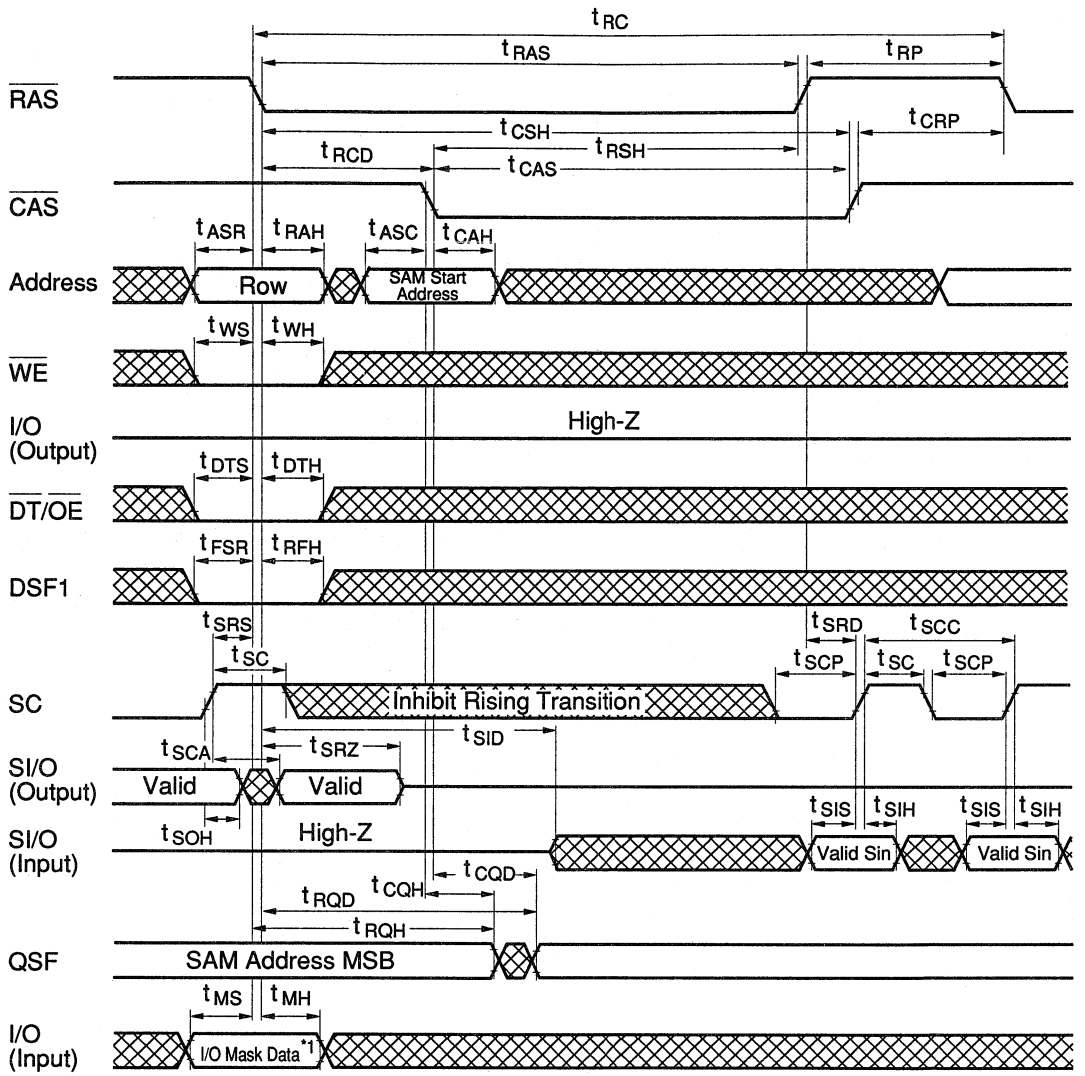
Read Transfer Cycle 1



Read Transfer Cycle 2



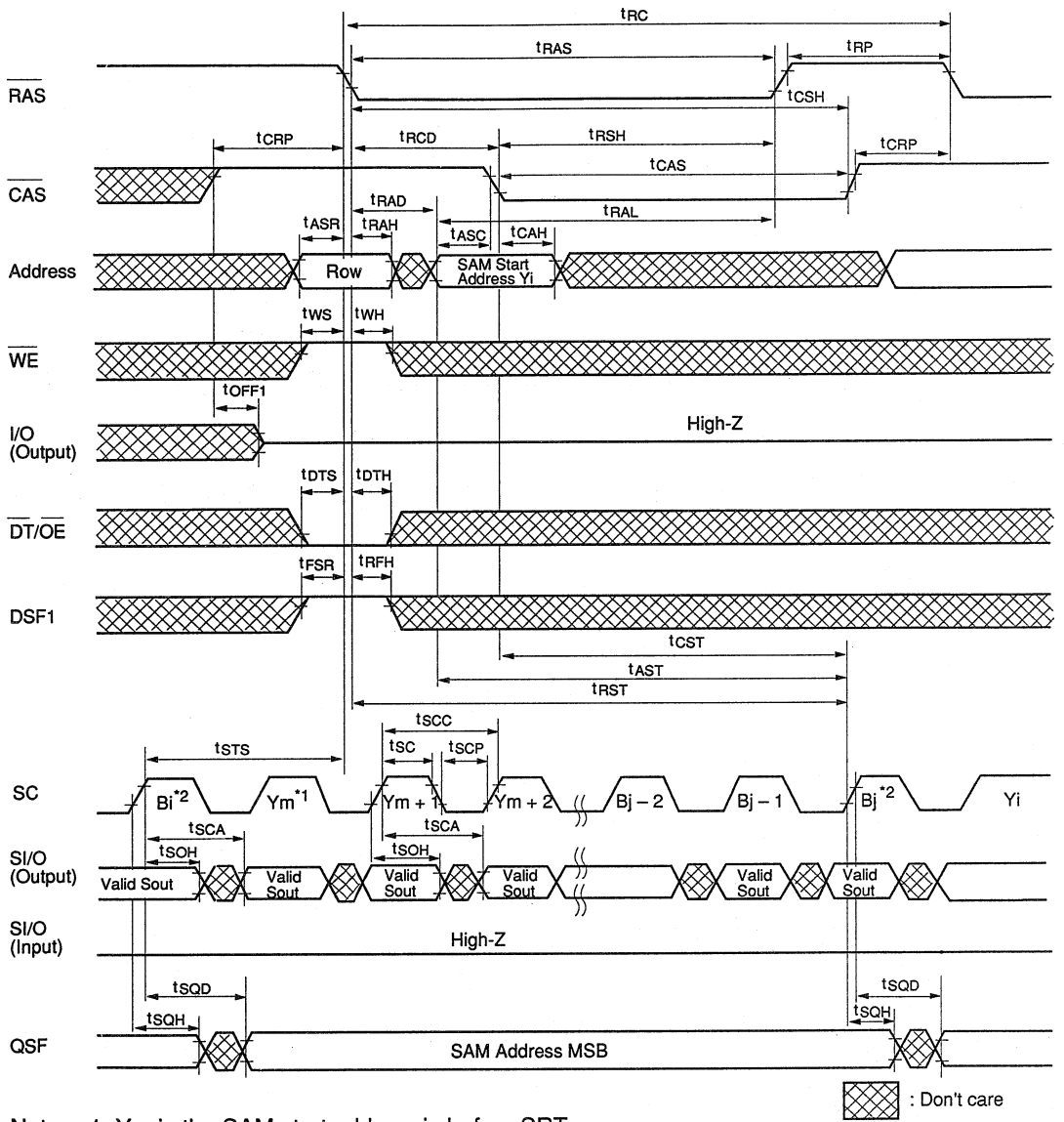
Masked Write Transfer Cycle



Note: 1. I/O mask data (In new mask mode)
Low: Mask
High: Non mask
I/O: Don't care in persistent mask mode.

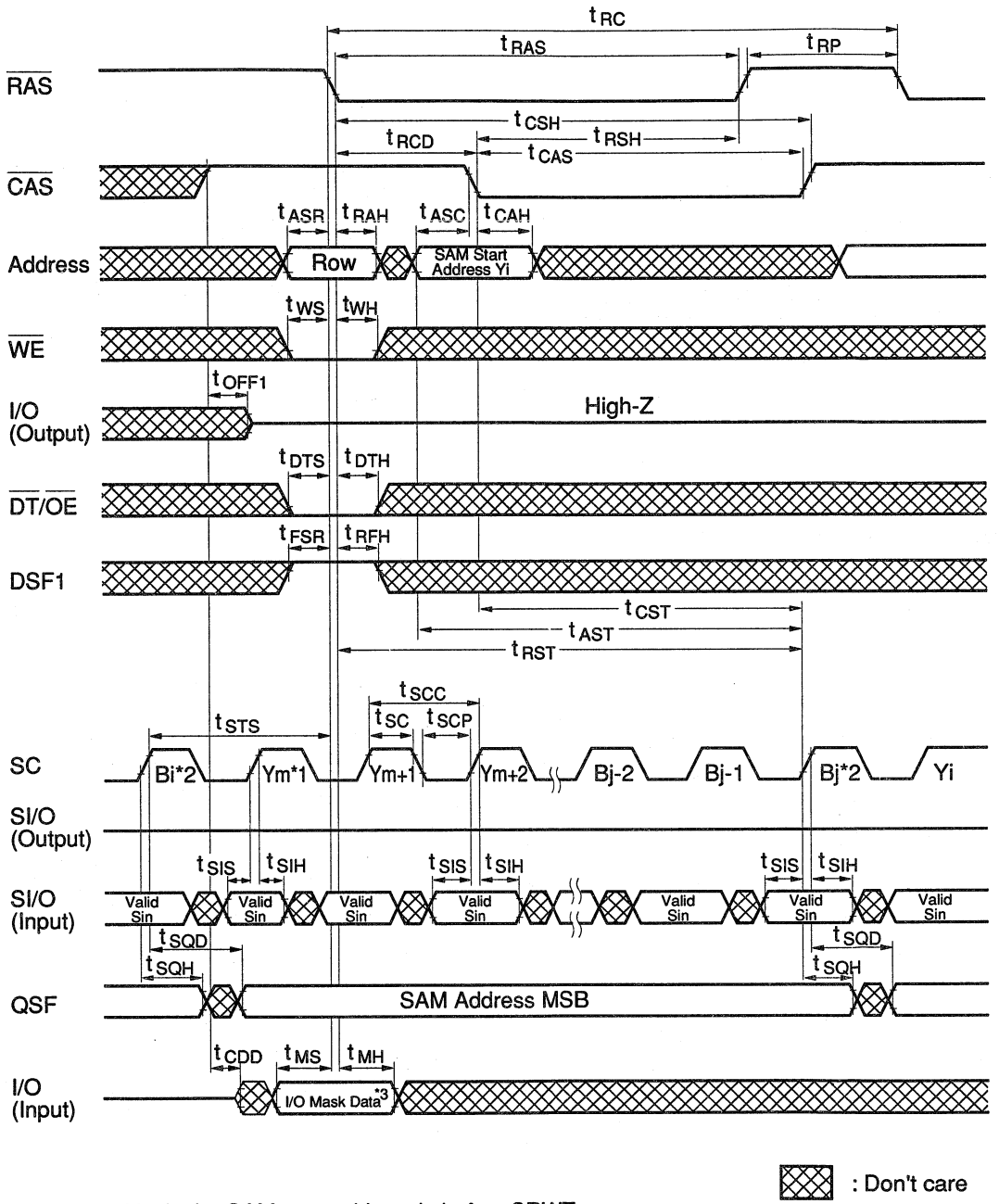
: Don't care

Split Read Transfer Cycle



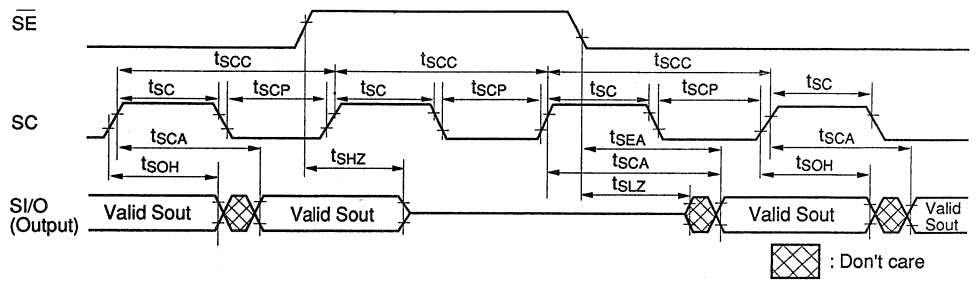
Notes: 1. Ym is the SAM start address in before SRT.
2. Bi, Bj initiate the boundary address.

Masked Split Write Transfer Cycle

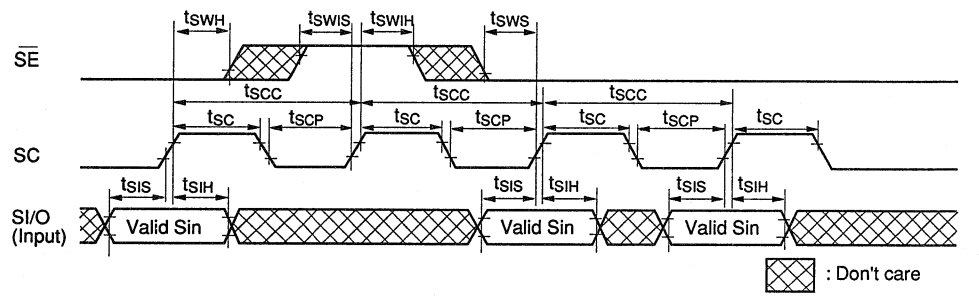


Notes: 1. Ym is the SAM start address in before SRWT.
2. Bi, Bj initiate the boundary address.
3. I/O Mask data (In new mask mode)
Low: Mask
High: Non mask
I/O: Don't care in persistent mask mode.

Serial Read Cycle



Serial Write Cycle



HM5316123 Series — Preliminary

131,072-word × 16-bit Multiport CMOS Video RAM

The HM5316123 is a 2-Mbit multiport video RAM equipped with a 128-kword × 16-bit dynamic RAM and a 256-word × 16-bit SAM (full-sized SAM). Its RAM and SAM operate independently and asynchronously. The HM5316123 is basically upward-compatible with the HM534253A/ HM538123A. However, the pseudo-write-transfer cycle is replaced with masked-write-transfer cycle, which is approved by JEDEC.

Furthermore, several new features are added to the HM5316123 without conflict with the conventional features. The stopping column feature adds flexibility to the length of the split SAM register. The HM5316123 also has a persistent mask feature, according to the TMS34020. Byte-write-control is useful for connecting × 16 organization memory to 8-bit bus systems.

Ordering Information

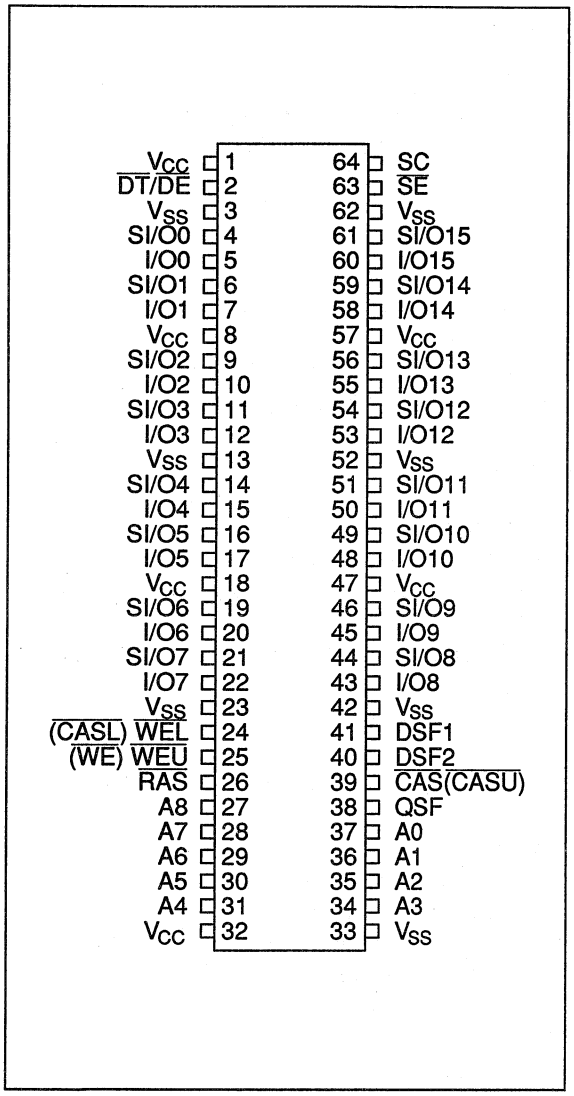
Type No.	Access Time	Package
HM5316123F-7	70 ns	64-pin plastic shrink SOP (FP-64DS)
HM5316123F-8	80 ns	
HM5316123F-10	100 ns	

Features

- Multiport organization
  - — Asynchronous and simultaneous operation of RAM and SAM capability
    - RAM: 128 kword × 16 bit
    - SAM: 256 word × 16 bit
- Access time
  - — RAM: 70 ns/80 ns/100 ns max
  - — SAM: 22 ns/25 ns/25 ns max
- Cycle time
  - — RAM: 135 ns/150 ns/180 ns min
  - — SAM: 25 ns/30 ns/30 ns min
- Low power
  - — Active RAM: 715 mW max
    SAM: 468 mW max
  - — Standby 38.5 mW max
- Masked-write-transfer cycle capability
- Stopping column feature capability
- Persistent mask capability
- Byte write control capability: 2 $\overline{WE}$ control (2 $\overline{CAS}$ control)
- High-speed page mode capability
- Mask write mode capability
- Bidirectional data transfer cycle between RAM and SAM capability
- Split transfer cycle capability
- Block write mode capability
- Flash write mode capability
- 3 veriations of refresh (8 ms/512 cycles)
  - — $\overline{RAS}$-only refresh
  - — $\overline{CAS}$-before-$\overline{RAS}$ refresh
  - — Hidden refresh
- TTL compatible

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

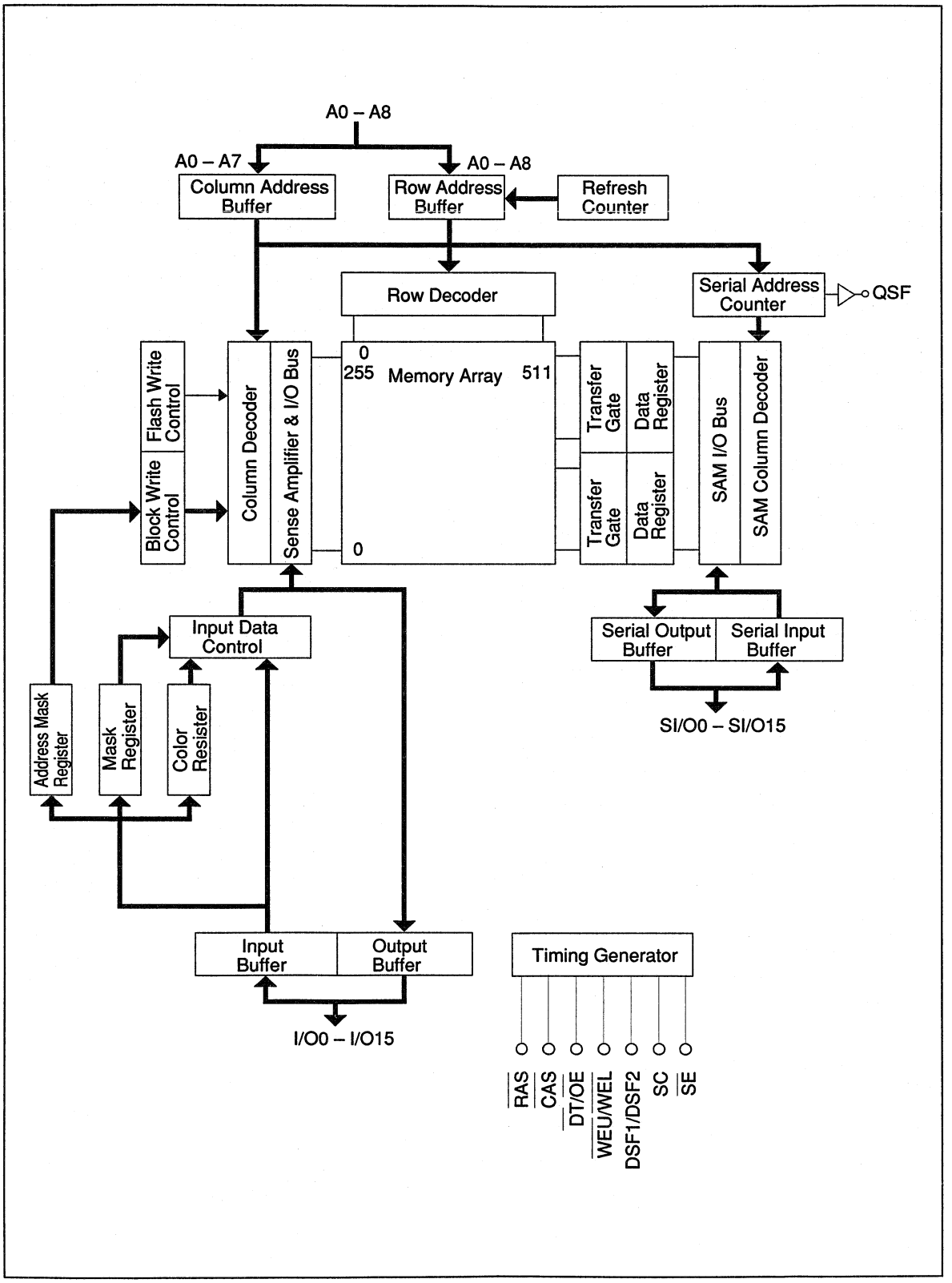
Pin Arrangement



Pin Description

Pin name	Function
A0–A8	Address inputs
I/O0–I/O15	RAM port data inputs/outputs
SI/O0–SI/O15	SAM port data inputs/outputs
RAS	Row address strobe
CAS (CASL, CASU)	Column address strobe
WEU, WEL (WE)	Write enable
DT/OE	Data transfer/output enable
SC	Serial clock
SE	SAM port enable
DSF1, DSF2	Special function input flag
QSF	Special function output flag
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Pin Functions

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active low and high in standby mode. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of these signals determine the operation cycle of the HM5316123.

$\overline{CAS}$ (input pin): Column address and DSF1 signals are fetched into the chip at the falling edge of $\overline{CAS}$, which determines the operation mode of the HM5316123. $\overline{CAS}$ controls output impedance of I/O in RAM.

A0–A8 (input pins): Row address (AX0–AX8) is determined by A0–A8 level at the falling edge of $\overline{RAS}$. Column address (AY0–AY7) is determined by A0–A7 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line that transfers data with SAM data register. Column address is the SAM start address after transfer.

$\overline{WEU}$ and $\overline{WEL}$ (input pins): $\overline{WEU}$ and $\overline{WEL}$ pins have two functions, at the falling edge of $\overline{RAS}$ and after. When either $\overline{WEU}$ or $\overline{WEL}$ is low at the falling edge of $\overline{RAS}$, the HM5316123 goes into mask write mode. Depending on the I/O level at the time, write on each I/O can be masked. ($\overline{WEU}$ and $\overline{WEL}$ levels at the falling edge of $\overline{RAS}$ are don't care in read cycle.) When both $\overline{WEU}$ and $\overline{WEL}$ are high at the falling edge of $\overline{RAS}$, a no-mask write cycle is executed. After that, $\overline{WEU}$ and $\overline{WEL}$ switch read/write cycles. Both $\overline{WEU}$ and

Table 1 Operation Cycles of the HM5316123

Mnemonic	$\overline{RAS}$					$\overline{CAS}$		Address		I/On Input	
Code	$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WE}$	DSF1	DSF2	DSF1	DSF2	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS/WE}$
CBRS	0	–	0	1	0	–	0	Stop	–	–	–
CBRR	0	–	1	0	0	–	0	–	–	–	–
CBRN	0	–	1	1	0	–	0	–	–	–	–
MWT	1	0	0	0	0	–	0	Row	TAP	WM	–
MSWT	1	0	0	1	0	–	0	Row	TAP	WM	–
RT	1	0	1	0	0	–	0	Row	TAP	–	–
SRT	1	0	1	1	0	–	0	Row	TAP	–	–
RWM	1	1	0	0	0	0	0	Row	Column	WM	Input data
BWM	1	1	0	0	0	1	0	Row	Column	WM	Column Mask
RW (No)	1	1	1	0	0	0	0	Row	Column	–	Input Data
BW (No)	1	1	1	0	0	1	0	Row	Column	–	Column Mask
FWM	1	1	0	1	0	–	0	Row	–	WM	–
LMR and Old Mask Set	1	1	1	1	0	0	0	(Row)	–	–	Mask Data
LCR	1	1	1	1	0	1	0	(Row)	–	–	Color
Option	0	0	0	0	0	–	0	Mode	–	Data	–

$\overline{WEL}$ must be held high in a read cycle. In a transfer cycle, the direction of transfer is determined by $\overline{WEU}$ and $\overline{WEL}$ levels at the falling edge of $\overline{RAS}$. When either $\overline{WEU}$ or $\overline{WEL}$ is low, data is transferred from SAM to RAM (data is written into RAM). When both $\overline{WEU}$ and $\overline{WEL}$ are high, data is transferred from RAM to SAM (data is read from RAM).

I/O0–I/O15 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only to high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM. In block write cycle, they function as address mask data at the falling edges of $\overline{CAS}$, and $\overline{WEU}$ or $\overline{WEL}$.

$\overline{DT}$/$\overline{OE}$ (input pin): $\overline{DT}$/$\overline{OE}$ functions as $\overline{DT}$ (data transfer) at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data is output from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is fetched into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle. Data on SI/O is not fetched into the SAM data register in serial write cycle. $\overline{SE}$ can be

Mnemonic Code	Write Mask	Pers W.M.	Register WM	Register Color	No.of Bndry	Function
CBRS	–	–	–	–	Set	CBR refresh with stop resister set
CBRR	–	Reset	Reset	–	Reset	CBR refresh with register reset
CBRN	–	–	–	–	–	CBR refresh (no reset)
MWT	Yes	No Yes	Load/use Use	–	–	Masked write transfer (new/old mask)
MSWT	Yes	No Yes	Load/use Use	–	Use	Masked split write transfer (new/old mask)
RT	–	–	–	–	–	Read transfer
SRT	–	–	–	–	Use	Split read transfer
RWM	Yes	No Yes	Load/use Use	–	–	Read/write (new/old mask)
BWM	Yes	No Yes	Load/use Use	Use	–	Block write (new/old mask)
RW (No)	No	No	–	–	–	Read/write (no mask)
BW (No)	No	No	–	Use	–	Block write (no mask)
FWM	Yes	No Yes	Load/use Use	Use	–	Masked flash write (new/old mask)
LMR and Old Mask Set	–	Set	Load	–	–	Load mask register and old mask set
LCR	–	–	–	Load	–	Load color resister set
Option	–	–	–	–	–	–

Notes: 1. With CBRS, all SAM operations use stop register.
2. After LMR, RWM, BWM, FWM, MWT, and MSWT, use old mask which can be reset by CBRR.
3. DSF2 is fixed low in all operations (for the future addition of operation modes)

used as a mask for serial write because the internal pointer is incremented at the rising edge of SC.

SI/O0–SI/O15 (input/output pins): SI/Os are input/output pins of the SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a masked write transfer cycle or write transfer cycle, SI/O inputs data.

DSF1 (input pin): DSF1 is a special function data input flag pin. It is set to high at the falling edge of $\overline{RAS}$ when new functions such as color register and mask register read/write, split transfer, and flash write, are used.

DSF2 (input pin): DSF2 is also a special function data input flag pin. This pin is fixed low in all operations of the HM5316123.

QSF (output pin): QSF outputs data of address A7 in SAM. QSF is switched from low to high by accessing address 127 in SAM and from high to low by accessing 255 address in SAM.

RAM Port Operation

RAM Read Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF1 low at the falling edge of $\overline{RAS}$, DSF1 low at the falling edge of $\overline{CAS}$): Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WEU}$ or $\overline{WEL}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data outputs through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle (Early Write, Delayed Write, Read-Modify-Write) ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF1 low at the falling edge of $\overline{RAS}$, DSF1 low at the falling edge of $\overline{CAS}$)

No-Mask Write Cycle ($\overline{WEU}$ and $\overline{WEL}$ high at the falling edge of $\overline{RAS}$): When $\overline{CAS}$ is set low and either $\overline{WEU}$ or $\overline{WEL}$ is set low after $\overline{RAS}$ low, a write cycle is executed.

If either $\overline{WEU}$ or $\overline{WEL}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and all I/O become in high impedance. All 16 data signals are latched on the falling edge of $\overline{CAS}$. If only one of $\overline{WEU}$ and $\overline{WEL}$ is low when $\overline{CAS}$ falls, the write will affect only those corresponding 8 bits. If the other of $\overline{WEU}$ and $\overline{WEL}$ falls at the same time in the cycle, those 8 bits will then be written with the latched data.

If both $\overline{WEU}$ and $\overline{WEL}$ are set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle and all 16 data bits are latched on the falling edge of $\overline{WEU}$ or $\overline{WEL}$. Byte write occurs if only one of $\overline{WEU}$ or $\overline{WEL}$ falls during the cycle. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

Mask Write Mode ($\overline{WEU}$ or $\overline{WEL}$ low at the falling edge of $\overline{RAS}$): If $\overline{WEU}$ or $\overline{WEL}$ is set low at the falling edge of $\overline{RAS}$, two modes of mask write cycle are possible.

In new mask mode, mask data is loaded and used. Whether or not an I/O is written depends on the I/O level at the falling edge of $\overline{RAS}$. The data is written to high level I/Os, and the data is masked and retained in low level I/Os. This mask data is effective during the $\overline{RAS}$ cycle. So in page mode cycles, the mask data is retained during the page access.

If a load mask register cycle (LMR) has been performed, the mask data is not loaded from I/O pins. The persistent mask data stored in the mask registers are used. This operation, known as persistent write mask, set by LMR cycle and reset by CBRR cycle.

High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF1 low at the falling edge of $\overline{RAS}$): High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle. In this cycle, read, write, and block write cycles can be mixed. Note that address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 256-word memory cells with the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 µs).

Color Register Set/Read Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ high, $\overline{WEU}$ and $\overline{WEL}$ high and DSF1 high at the falling edge of $\overline{RAS}$): In a color register set cycle, color data is set to the internal color register used in flash write cycle or block write cycle. 16 bits of internal color register are provided at each I/O. This register is composed of static circuits, so once it is set, it retains the data until reset. Since a color register set cycle is just as same as the usual read and write cycle, so read, early write and delayed write cycles can be executed. In this cycle, the HM5316123 refreshes the row address fetched at the falling edge of $\overline{RAS}$.

Mask Register Set/Read Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ high, $\overline{WEU}$ and $\overline{WEL}$ high, and DSF1 low at the falling edge of $\overline{RAS}$): In mask register set cycle, mask data is set to the internal mask register used in mask write cycle, block write cycle, flash write cycle, masked write transfer, and masked split write transfer. 16 bits of internal mask register are provided at each I/O. This mask register is composed of static circuits, so once it is set, it retains the data until reset. Since the mask register set cycle is just as same as the usual read and write cycle, read, so early and delayed write cycles, and read cycles can be executed.

Flash Write Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ high, $\overline{WEU}$ or $\overline{WEL}$ low, and DSF1 high at the falling edge of $\overline{RAS}$): In a flash write cycle, a row of data (256 word × 16 bit) is cleared to 0 or 1 at each I/O according to the data of color register mentioned previously. It is also necessary to mask I/O in this cycle. This cycle starts when $\overline{CAS}$ and $\overline{DT/OE}$ are set high, $\overline{WEU}$ or $\overline{WEL}$ is low, and DSF1 is high at the falling edge of $\overline{RAS}$. Then, the row address to be cleared is set for the row address. Mask data is as same as that of a RAM write cycle. Cycle time is the same as those of RAM read/write cycles, so all bits can be cleared in 1/256 of the usual cycle time. (See figure 1.)

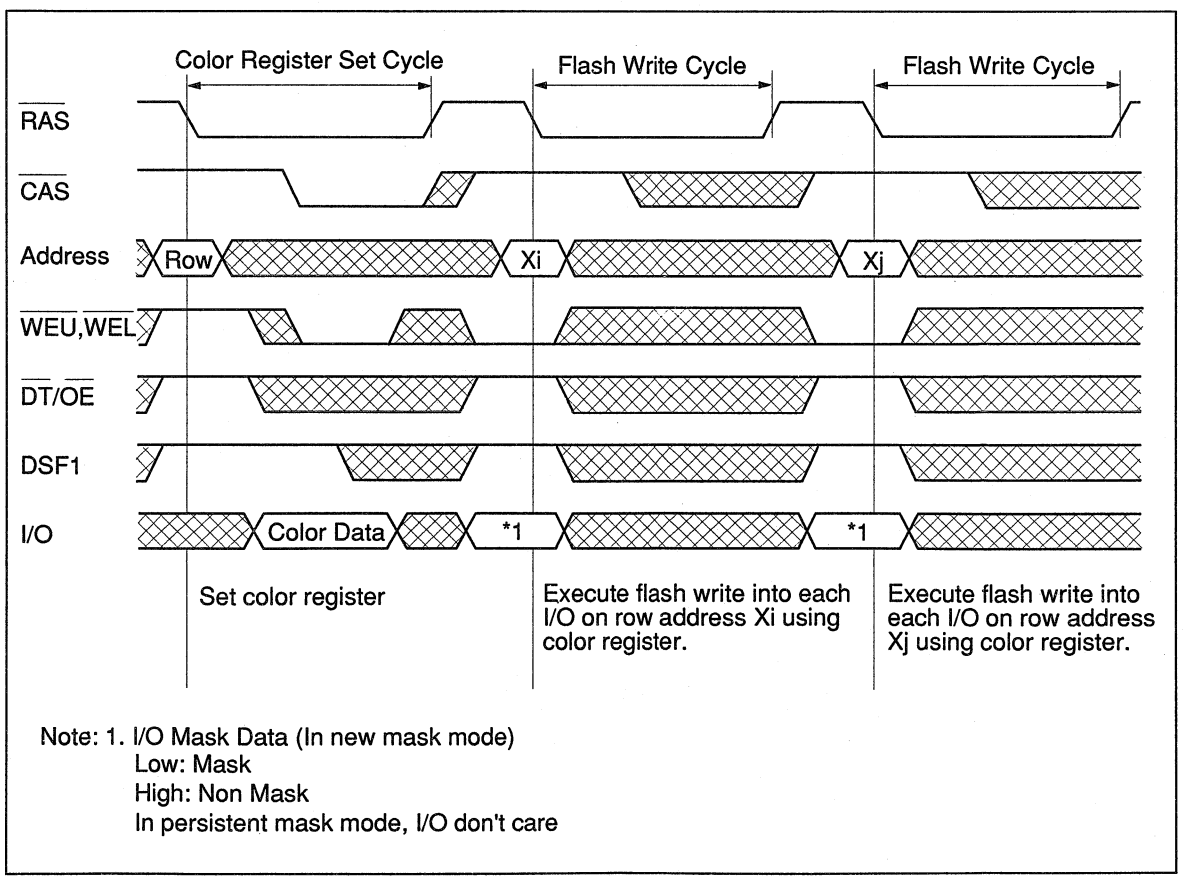
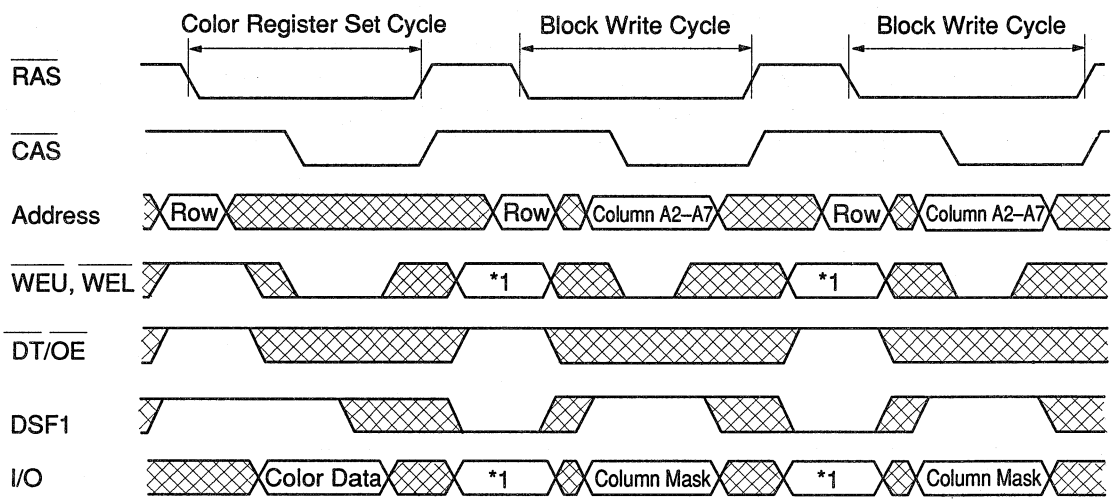


Figure 1 Use of Flash Write

Block Write Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ high and DSF1 low at the falling edge of $\overline{RAS}$, DSF1 high at the falling edge of $\overline{CAS}$ and $\overline{WEU}$, $\overline{WEL}$): In a block write cycle, 4 columns of data (4 word × 16 bit) are cleared to 0 or 1 at each I/O according to the data of color register. Column addresses A0 and A1 are disregarded. The data on I/Os and addresses can be masked. I/O level at the falling edge of $\overline{CAS}$ determines the address to be cleared. (See figure 2.) The block write cycle is the same as the usual write cycle, so early and delayed write, read-modify-write, and page mode write cycles can be executed.

No-Mask Mode Block Write Cycle ($\overline{WEU}$ and $\overline{WEL}$ high at the falling edge of $\overline{RAS}$): The data on all 16 I/Os are cleared when $\overline{WEU}$ and $\overline{WEL}$ are high at the falling edge of $\overline{RAS}$.

Mask Block Write Cycle ($\overline{WEU}$ or $\overline{WEL}$ low at the falling edge of $\overline{RAS}$): When either $\overline{WEU}$ or $\overline{WEL}$ is low at the falling edge of $\overline{RAS}$, the HM5316123 starts mask block write cycle to clear the data on an optional I/O. The mask data is the same as that of a RAM write cycle.



*1

WEU, WEL	Mode	I/O data/RAS
Low	New mask mode	Mask
	Persistent mask mode	Don't care (mask register used)
High	No mask	Don't care

I/O Mask Data (In new mask mode)

Low: Mask

High: Non Mask

In persistent mask mode, I/O don't care

Column Mask Data

I/O0	Column0 (A0 = 0, A1 = 0) Mask Data	Low: Mask
I/O1	Column1 (A0 = 1, A1 = 0) Mask Data	
I/O2	Column2 (A0 = 0, A1 = 1) Mask Data	
I/O3	Column3 (A0 = 1, A1 = 1) Mask Data	High: Non Mask

Figure 2 Use of Block Write

Transfer Operation

The HM5316123 provides the read transfer cycle, split read transfer cycle, masked write transfer cycle and masked split write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{CAS}$ high and $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:

- Transfer data between row address and SAM data register
  - —Read transfer cycle and split read transfer cycle: RAM to SAM
  - —Masked write transfer cycle and masked split write transfer cycle: SAM to RAM
- Determine SI/O state
  - —Read transfer cycle: SI/O output
  - —Masked write transfer cycle: SI/O input
- Determine first SAM address to access after transferring at column address (SAM start address).
  - —SAM start address must be determined by read transfer cycle or masked write transfer cycle (split transfer cycle isn't available) before SAM access, after power on, and for each transfer cycle.
- Use the stopping columns (boundaries) in the serial shift register. If the stopping columns have been set, split transfer cycles use the stopping columns, but no boundaries can be set as the start address.
- Load/use mask data in masked write transfer cycle and masked split write transfer cycle.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WEU}$ and $\overline{WEL}$ high and DSF1 low at the falling edge of $\overline{RAS}$): Start read transfer cycle by driving $\overline{DT}/\overline{OE}$ low, $\overline{WEU}$ and $\overline{WEL}$ high and DSF1 low at the falling edge of $\overline{RAS}$. The row address data (256 × 16 bits) determined by this cycle is transferred to the SAM data register synchronously at the rising edge of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from the SAM start address determined by the column address. In a read transfer cycle, $\overline{DT}/\overline{OE}$ must be high to transfer data from RAM to SAM.

This cycle can access SAM even during transfer (real-time read transfer). In this case, the timing t_{SDD} (min) specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge, and t_{SDH} (min) specified between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge must be satisfied. (See figure 3.)

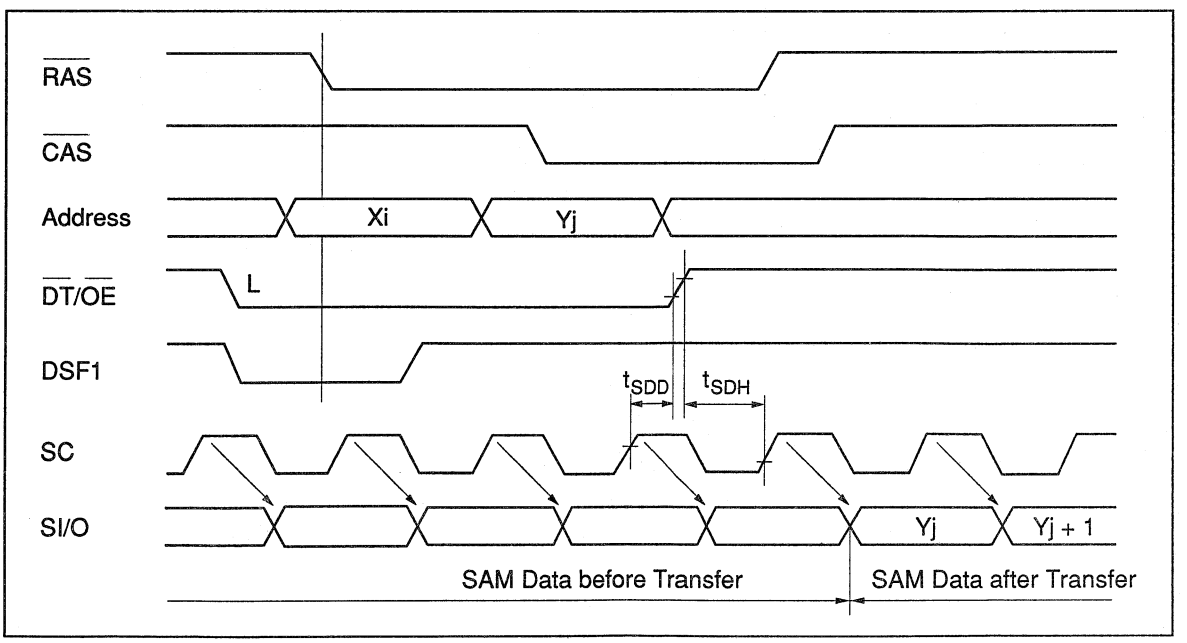


Figure 3 Real-Time Read Transfer

When a read transfer cycle is executed, SI/O reaches output state by first SAM access. Input must be set high impedance before t_{SZS} (min) of the first SAM access to avoid data contention.

Masked Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WEU}$ or $\overline{WEL}$ low, and DSF1 low at the falling edge of $\overline{RAS}$): Masked write transfer cycle can transfer only selected I/O data in a row of data input by a serial write cycle to RAM. Whether an I/O data is transferred or not depends on the corresponding I/O level (mask data) at the falling edge of $\overline{RAS}$. This mask transfer operation is the same as the mask write operation in RAM cycles, so the persistent mode is supported.

The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address for serial write after terminating this cycle.

In this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC must not rise. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addreses in RAM by a write transfer cycle. However, the data write adddress must be the same as that of the read transfer cycle or the split read transfer cycle (row address AX8)

Split Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WEU}$ and $\overline{WEL}$ high and DSF1 high at the falling edge of $\overline{RAS}$): To execute a continuous serial read by real-time read transfer, the HM5316123 must satisfy SC and $\overline{DT/OE}$ timing. It requires an external circuit to detect the last SAM address. The split read transfer cycle makes it possible to execute a continuous serial read without the above timing limitation.

The HM5316123 supports two types of split register operation. One is the normal split register operation, which splits the data register into two halves. The other is the boundary split register operation using stopping columns described later.

Figure 4 shows the block diagram for the normal split register operation. The SAM data register (DR) consists of 2 split buffers, whose organizations are 128 words × 16 bits each. Suppose that data is read from upper data register DR1. (The row address AX8 is 0 and SAM address A7 is 1.) When a split read transfer is executed setting row address AX8 to 0 and SAM start addresses A0 to A6, 128-word × 16-bit data are

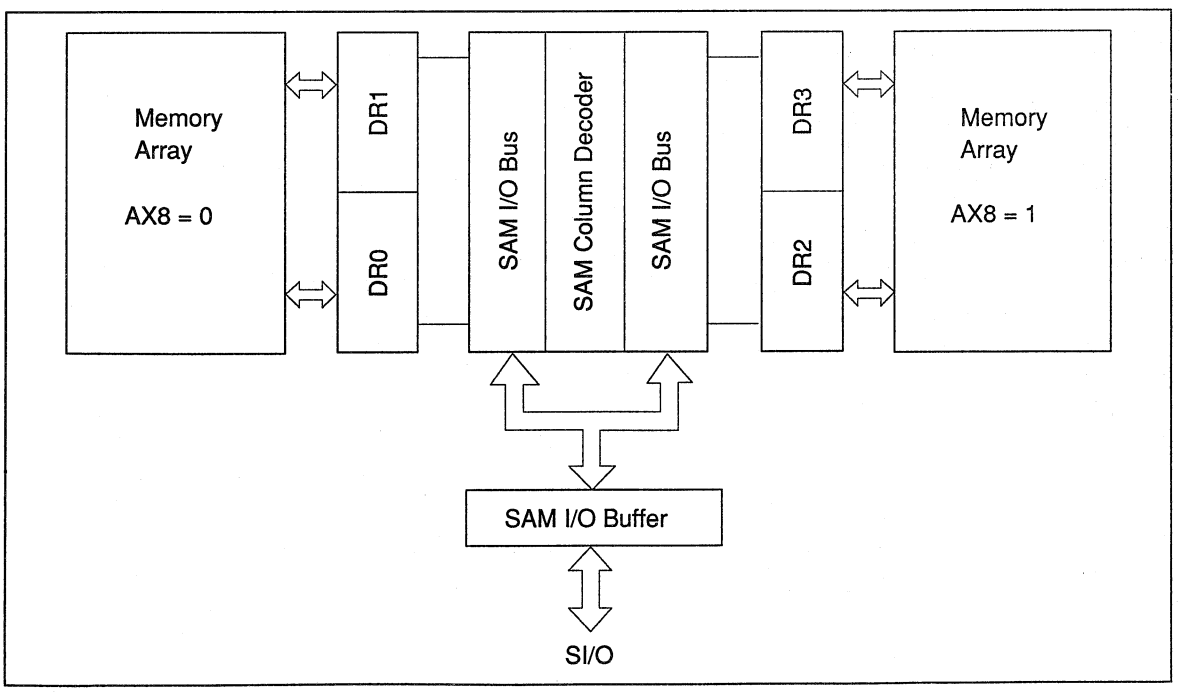


Figure 4 Split Transfer Block Diagram

transferred from RAM to the lower data register DR0 (SAM address A7 is 0) automatically. After data is read from data register DR1, data read begins from SAM start addresses of data register DR0. If the next split read transfer isn't executed while data is being read from data register DR0, data start to be read from SAM start address 0 of DR1 after data is read from data register DR0.

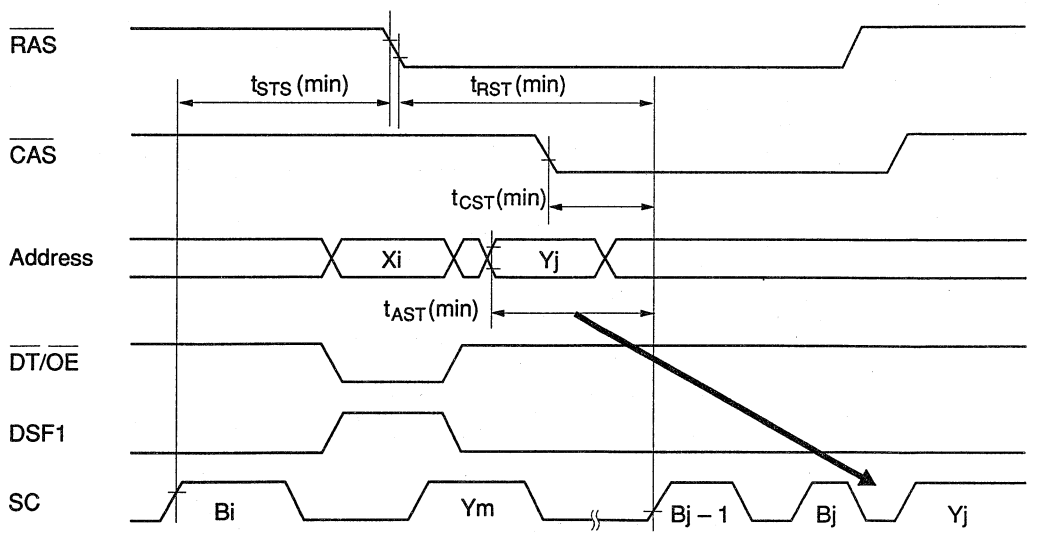
If split read transfer is executed with row address AX8 set to 1 and SAM start addresses A0 to A6 while data are read from data register DR1, 128-word × 16-bit data are transferred to data register DR2. After data are read from data register DR1, data read begins from SAM start addresses of data register DR2. If the next split read transfer isn't executed while data is read from data register DR2, data read begins from SAM start address 0 of data register DR1 after data are read from data register DR2. In split read data transfer, the SAM start address A7 is automatically set in the data register which isn't used.

The data on SAM address A7, which will be accessed next, is output to QSF. QSF is switched from low to high by accessing the last SAM address, 127, and from high to low by accessing address 255.

Split read transfer cycle is set when $\overline{CAS}$ is high, $\overline{DT/OE}$ is low, $\overline{WEU}$ and $\overline{WEL}$ is high and DSF1 is high at the falling edge of $\overline{RAS}$. The cycle can be executed asyncronously with SC. However, HM5316123 must satisfy t_{STS} (min) timing specified between SC rising (boundary address) and $\overline{RAS}$ falling. In split transfer cycle, the HM5316123 must satisfy t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings specified between $\overline{RAS}$ or $\overline{CAS}$ falling and column address. (See figure 5.)

In split read transfer, SI/O isn't switched to output state. Therefore, read transfer must be executed to switch SI/O to output state when the previous transfer cycle is masked write transfer cycle or masked split write transfer cycle.

Masked Split Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WEU}$ or $\overline{WEL}$ low and DSF1 high at the falling edge of $\overline{RAS}$): A continuous serial write cannot be executed because accessing SAM is inhibited during $\overline{RAS}$ low in write transfer. Masked split write transfer cycle makes it possible. In this cycle, t_{STS} (min), t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings must be satisfied as in split read transfer cycle. It is impossible to switch SI/O to input state in this cycle. If SI/O is in output



Note: Ym is the SAM start address in before SRT. Bi and Bj initiate the boundary address.

Figure 5 Split Transfer Limitation

state, masked write transfer cycle should be executed to switch SI/O into input state. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addresses of RAM by split write transfer cycle. However, in this split write transfer cycle, the MSB of the row address (AX8) for write data must be the same as that of the read transfer cycle or the split read transfer cycle. In this cycle, the boundary split register operation using stopping columns is possible as split read transfer cycle.

Stopping Column in Split Transfer Cycle: The HM5316123 boundary split register operation uses stopping columns. If a CBRS cycle has been performed, split transfer cycle performs the boundary operation. Figure 6 shows an example of boundary split register. (Boundary code is B6.)

First, a read data transfer cycle is executed, and SAM start addresses A0 to A7 are set. The RAM data are transferred to the lower SAM, and SAM serial read starts from the start address (Y1) on the lower SAM. After that, a split read transfer cycle is executed, and the next start address (Y2) is set. The RAM data are transferred to the upper SAM. When the serial read data arrive at the first boundary after the split read transfer cycle, the next read jumps to the start address (Y2) on the upper SAM (jump 1) and continues. Then the second split read transfer cycle is executed, and another start address (Y3) is set. The RAM data are transferred to the lower SAM. When the serial read arrive at the other boundary again, the next read jumps to the start address (Y3) on the lower SAM.

Stopping Column Set Cycle (CBRS): Start a stopping column set cycle by driving $\overline{CAS}$ low, $\overline{WEU}$ or $\overline{WEL}$ low, DSF1 high at the falling edge of $\overline{RAS}$. Stopping column data (boundaries) are latched from address inputs on the falling edge of $\overline{RAS}$. Use A2 to A6 to determine the boundary. A0, A1, and A7 are don't care. In the HM5316123, six types of boundary (B2 to B7) can be set including the default case. (See table 1.) If A2 to A5 are set to low and A6 is set to high, the boundaries (B6) are selected. Figure 6 shows the example. Once a CBRS is executed, the stopping column operation mode continues until CBRR.

Register Reset Cycle (CBRR): Start a register reset cycle (CBRR) by driving $\overline{CAS}$ low, $\overline{WEU}$ and $\overline{WEL}$ high, and DSF1 low at the falling edge of $\overline{RAS}$. A CBRR can reset the persistent mask operation and stopping column operation. When a CBRR is executed for stopping column operation reset, it must safisfy t_{STS} (min) and t_{RST} (min) between $\overline{RAS}$ falling and SC rising.

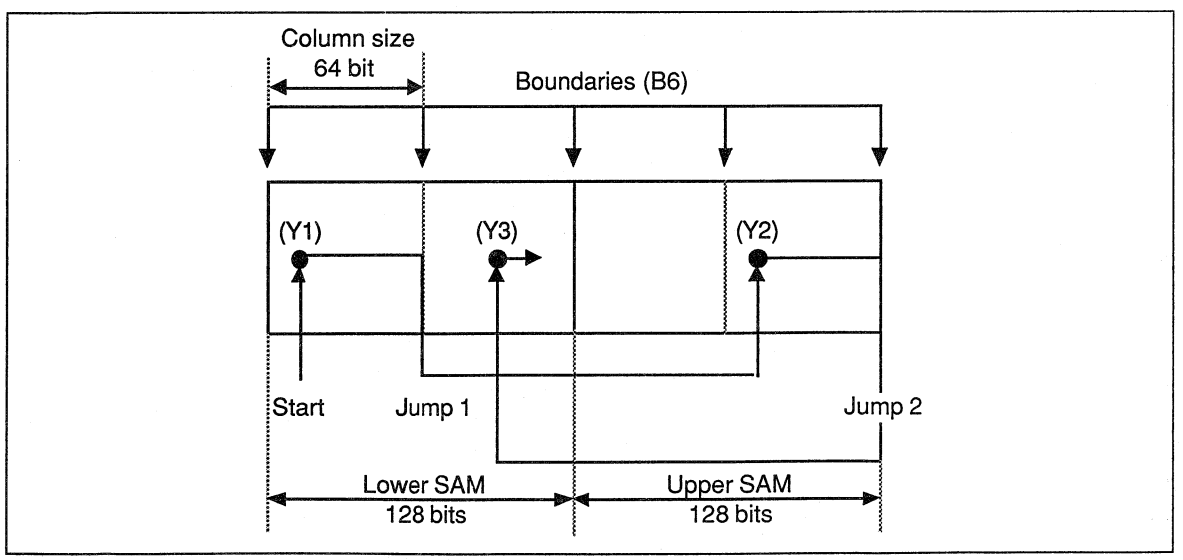


Figure 6 Boundary Split Register Example

Table 1 Stopping Column Boundary Table

Boundary Code	Column Size	Stop Address				
		A2	A3	A4	A5	A6
B2	4	0	*	*	*	*
B3	8	1	0	*	*	*
B4	16	1	1	0	*	*
B5	32	1	1	1	0	*
B6	64	1	1	1	1	0
B7	128	1	1	1	1	1

Notes: 1. A0, A1, and A7: Don't care
2. *: Don't care

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is a read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When $\overline{SE}$ is set high, SI/O becomes high impedance, and the internal pointer is incremented by the SC rising edge. After indicating the last address (address 255), the internal pointer indicates address 0 at the next access.

Serial Write Cycle

If the previous data transfer cycle is a masked write transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is fetched into data register at the SC rising edge as in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't fetched into the data register. The internal pointer is incremented by the SC rising edge, so $\overline{SE}$ high can be used as mask data for SAM. After indicating the last address (address 255), the internal pointer indicates address 0 at the next access.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is executed by accessing all 512 row addresses within 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBRN, CBRS, and CBRR) refresh, and (3) Hidden refresh. Besides these, cycles that activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required when all row addresses are accessed within 8 ms.

$\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is executed by activating a $\overline{RAS}$ cycle only with $\overline{CAS}$ fixed high after inputting the row address (= refresh address) from external circuits. To distinguish this cycle from data transfer cycle, $\overline{DT/OE}$ must be high at the falling edge of $\overline{RAS}$.

CBR Refresh Cycle: CBR refresh cycle (CBRN, CBRS, and CBRR) are set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, the refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate.

Hidden Refresh Cycle: Hidden refresh cycle executes CBR refresh with the data output by reactivating $\overline{RAS}$ when $\overline{DT/OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift resister and selector), are organized as fully static circuitry, require no refresh.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	–0.5 (Note 2)	—	0.8	V	1

Notes: 1. All voltages referenced to V_{SS}
2. –3.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM5316123								
		-7		-8		-10				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	
Operating current	I_{CC1}	—	120	—	105	—	90	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC7}	—	190	—	160	—	140	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Standby current	I_{CC2}	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC8}	—	85	—	70	—	70	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
$\overline{RAS}$-only refresh current	I_{CC3}	—	120	—	105	—	90	mA	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH} t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC9}	—	190	—	160	—	140	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Page mode current	I_{CC4}	—	130	—	115	—	100	mA	$\overline{CAS}$ cycling $\overline{RAS}$ = V_{IL} t_{PC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10}	—	200	—	170	—	150	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	—	95	—	85	—	70	mA	$\overline{RAS}$ cycling t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC11}	—	165	—	140	—	120	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Data transfer current	I_{CC6}	—	130	—	115	—	100	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC12}	—	200	—	170	—	150	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA		
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA		
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	V	I_{OH} = –1 mA	
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	V	I_{OL} = 2.1 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once while $\overline{RAS}$ is low and $\overline{CAS}$ is high.

Capacitance (Ta = 25°C, V_{CC} = 5 ±10%, f = 1 MHz, Bias: Clock, I/O = V_{CC}, Address = V_{SS})

Parameter	Symbol	Typ	Max	Unit	Note
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	5	pF	1
Output capacitance (I/O, SI/O, QSF)	$C_{I/O}$	—	7	pF	1

Notes: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) *1, *16

Test Conditions

- Input rise and fall times: 5 ns
- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load:
  - —RAM: 1 TTL + C_L (50 pF)
  - —SAM: 1 TTL + C_L (30 pF)
  (Including scope and jig)

Common ParameterHM5316123

		HM5316123							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	135	—	150	—	180	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	55	—	60	—	70	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	—	20	—	25	—	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	20	75	ns	2
$\overline{RAS}$ hold time referenced to $\overline{CAS}$	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	
Transition time (rise to fall)	t_T	3	50	3	50	3	50	ns	3
Refresh period	t_{REF}	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ setup time	t_{DTS}	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ hold time	t_{DTH}	10	—	10	—	10	—	ns	

Parameter	Symbol	HM5316123 -7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Notes
DSF1to $\overline{RAS}$ setup time	t_{FSR}	0	—	0	—	0	—	ns	

Common Parameters (cont)

Parameter	Symbol	HM5316123 -7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Notes
DSF1 to $\overline{RAS}$ setup time	t_{FSR}	0	—	0	—	0	—	ns	
DSF1 to $\overline{RAS}$ hold time	t_{RFH}	10	—	10	—	10	—	ns	
DSF1 to $\overline{CAS}$ setup time	t_{FSC}	0	—	0	—	0	—	ns	
DSF1 to $\overline{CAS}$ hold time	t_{CFH}	15	—	15	—	15	—	ns	
Data-in to $\overline{CAS}$ delay time	t_{DZC}	0	—	0	—	0	—	ns	4
Data-in to $\overline{OE}$ delay time	t_{DZO}	0	—	0	—	0	—	ns	4
Output buffer turn-off delay referenced to $\overline{CAS}$	t_{OFF1}	—	20	—	20	—	20	ns	5
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	—	20	—	20	—	20	ns	5

Read Cycle (RAM), Page Mode Read Cycle

Parameter	Symbol	HM5316123 -7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	40	—	45	ns	7, 9
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns	10
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	10
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	2
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	35	—	40	—	45	—	ns	
Page mode cycle time	t_{PC}	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	7	—	10	—	10	—	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	—	45	—	50	ns	
Page mode $\overline{RAS}$ pulse width	t_{RASP}	70	100000	80	100000	100	100000	ns	

Write Cycle (RAM), Page Mode Write Cycle, Color Register Set Cycle

		HM5316123							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	11
Write command hold time	t_{WCH}	15	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	15	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	15	—	15	—	15	—	ns	12
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	10	—	10	—	10	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	10	—	10	—	10	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	20	—	20	—	20	—	ns	
Page mode cycle time	t_{PC}	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	7	—	10	—	10	—	ns	
$\overline{CAS}$ to data-in delay time	t_{CDD}	20	—	20	—	20	—	ns	13
Page mode $\overline{RAS}$ pulse width	t_{RASP}	70	100000	80	100000	100	100000	ns	

Read-Modify-Write Cycle

		HM5316123							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	185	—	200	—	230	—	ns	
$\overline{RAS}$ pulse width (read-modify-write cycle)	t_{RWS}	120	10000	130	10000	150	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	45	—	45	—	50	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	60	—	65	—	70	—	ns	14
$\overline{OE}$ to data-in delay time	t_{CDD}	20	—	20	—	20	—	ns	12
Access time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	40	—	45	ns	7, 9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	15	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	15	—	15	—	15	—	ns	12
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	20	—	20	—	20	—	ns	

Refresh Cycle

		HM5316123							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	

Flash Write Cycle, Block Write Cycle, and Register Read Cycle

		HM5316123							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ to data-in delay time	t_{CDD}	20	—	20	—	20	—	ns	13
$\overline{OE}$ to data-in delay time	t_{ODD}	20	—	20	—	20	—	ns	13

CBR Refresh with Register Reset

		HM5316123							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Split transfer setup time	t_{STS}	20	—	20	—	25	—	ns	
Split transfer hold time referenced to $\overline{RAS}$	t_{RST}	70	—	80	—	100	—	ns	

Read Transfer Cycle

		HM5316123							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{DT}$ hold time referenced to $\overline{RAS}$	t_{RDH}	60	10000	65	10000	80	10000	ns	
$\overline{DT}$ hold time referenced to $\overline{CAS}$	t_{CDH}	20	—	20	—	25	—	ns	
$\overline{DT}$ hold time referenced to column address	t_{ADH}	25	—	30	—	30	—	ns	
$\overline{DT}$ precharge time	t_{DTP}	20	—	20	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ delay time	t_{DRD}	65	—	70	—	80	—	ns	
SC to $\overline{RAS}$ setup time	t_{SRS}	25	—	30	—	30	—	ns	
1st SC to $\overline{RAS}$ hold time	t_{SRH}	70	—	80	—	100	—	ns	
1st SC to $\overline{CAS}$ hold time	t_{SCH}	25	—	25	—	25	—	ns	
1st SC to column address hold time	t_{SAH}	40	—	45	—	50	—	ns	
Last SC to $\overline{DT}$ delay time	t_{SDD}	5	—	5	—	5	—	ns	
1st SC to $\overline{DT}$ hold time	t_{SDH}	10	—	15	—	15	—	ns	
$\overline{DT}$ to QSF delay time	t_{DQD}	—	35	—	35	—	35	ns	7
QSF hold time referenced to $\overline{DT}$	t_{DQH}	5	—	5	—	5	—	ns	
Serial data-in to 1st SC delay time	t_{SZS}	0	—	0	—	0	—	ns	
Serial clock cycle time	t_{SCC}	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	
$\overline{RAS}$ to QSF delay time	t_{RQD}	—	70	—	75	—	85	ns	
$\overline{CAS}$ to QSF delay time	t_{CQD}	—	35	—	35	—	35	ns	
QSF hold time referenced to$\overline{RAS}$	t_{RQH}	20	—	20	—	25	—	ns	
QSF hold time referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	5	—	ns	

Masked Write Transfer Cycle

		HM5316123							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
SC setup time referenced to $\overline{RAS}$	t_{SRS}	25	—	30	—	30	—	ns	
$\overline{RAS}$ to SC delay time	t_{SRD}	20	—	25	—	25	—	ns	
Serial output buffer turn-off time referenced to $\overline{RAS}$	t_{SRZ}	10	40	10	45	10	50	ns	
$\overline{RAS}$ to serial data-in delay time	t_{SID}	40	—	45	—	50	—	ns	
$\overline{RAS}$ to QSF delay time	t_{RQD}	—	70	—	75	—	85	ns	7
$\overline{CAS}$ to QSF delay time	t_{CQD}	—	35	—	35	—	35	ns	7
QSF hold time referenced to $\overline{RAS}$	t_{RQH}	20	—	20	—	25	—	ns	
QSF hold time referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	5	—	ns	
Serial clock cycle time	t_{SCC}	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	

Split Read Transfer Cycle, Masked Split Write Transfer Cycle

		HM5316123							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Split transfer setup time	t_{STS}	20	—	20	—	25	—	ns	
Split transfer hold time referenced to $\overline{RAS}$	t_{RST}	70	—	80	—	100	—	ns	
Split transfer hold time referenced to $\overline{CAS}$	t_{CST}	20	—	20	—	25	—	ns	
Split transfer hold time referenced to column address	t_{AST}	35	—	40	—	45	—	ns	
SC to QSF delay time	t_{SQD}	—	30	—	30	—	30	ns	7
QSF hold time referenced to SC	t_{SQH}	5	—	5	—	5	—	ns	
Serial clock cycle time	t_{SCC}	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	

Serial Read Cycle, Serial Write Cycle

		HM5316123							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Serial clock cycle time	t_{SCC}	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	ns	
Access time from SC	t_{SCA}	—	22	—	25	—	25	ns	15
Access time from $\overline{SE}$	t_{SEA}	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	ns	
Serial output buffer turn-off time referenced to $\overline{SE}$	t_{SHZ}	—	20	—	20	—	20	ns	5
$\overline{SE}$ to serial output in low-Z	t_{SLZ}	0	—	0	—	0	—	ns	5
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	ns	

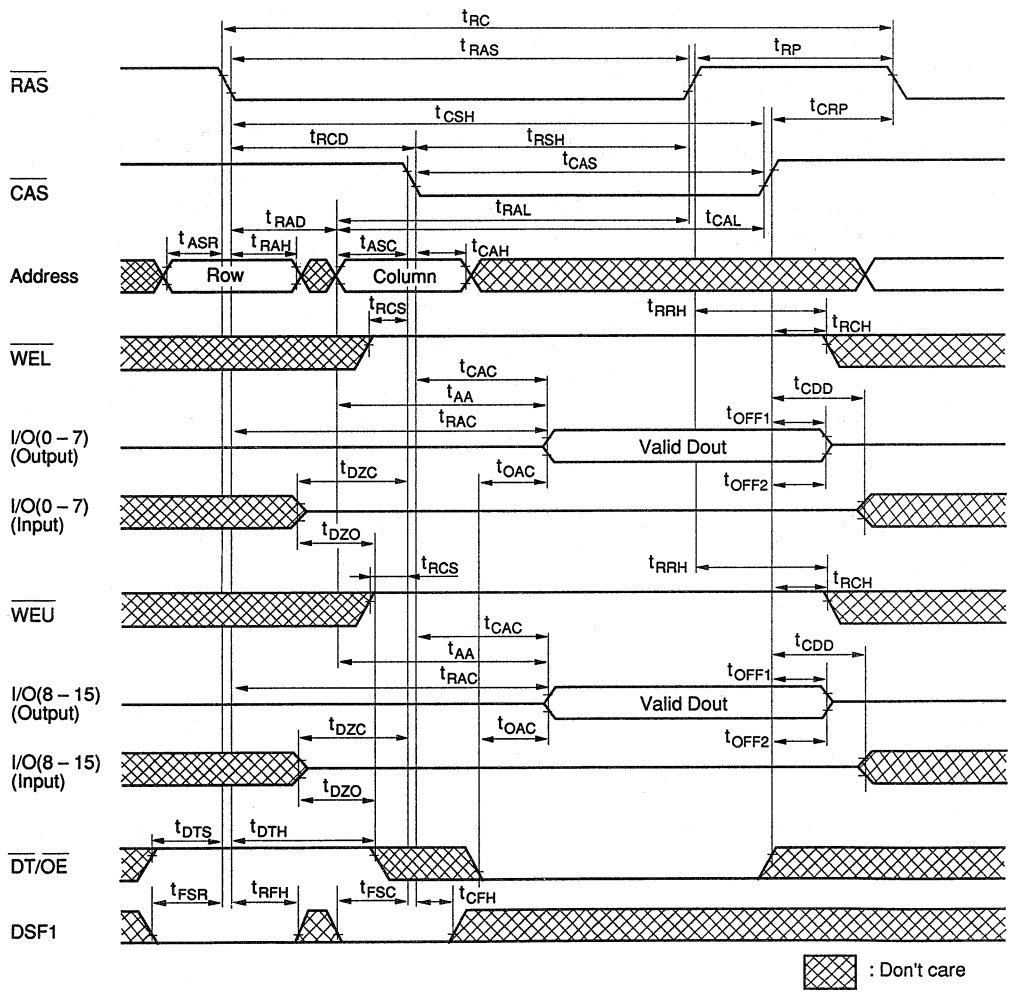
Serial Read Cycle, Serial Write Cycle (cont)

		HM5316123							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Serial write enable setup time	t_{SWS}	0	—	0	—	0	—	ns	
Serial wrtie enable hold time	t_{SWH}	15	—	15	—	15	—	ns	
Serial write disable setup time	t_{SWIS}	0	—	0	—	0	—	ns	
Serial write disable hold time	t_{SWIH}	15	—	15	—	15	—	ns	

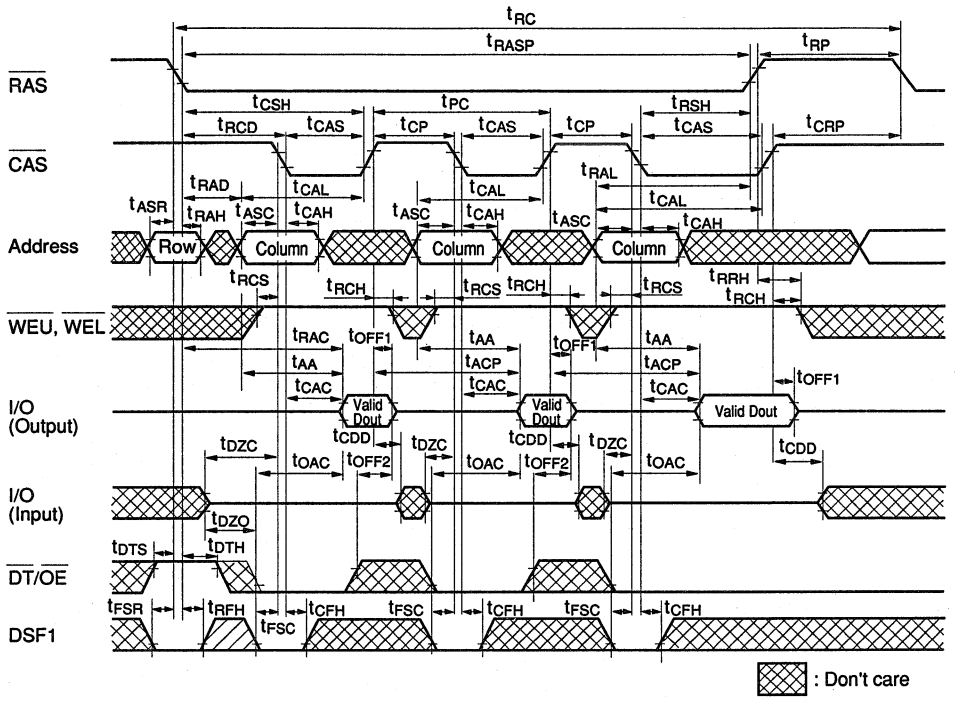
Notes:
1. AC measurements assume t_T = 5 ns.
2. When $t_{RCD} > t_{RCD}$ (max) and $t_{RAD} > t_{RAD}$ (max), access time is specified by t_{CAC} or t_{AA}.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition time t_T is measured between V_{IH} and V_{IL}.
4. Data input must be floating before output buffer is turned on. In read cycle, read-modify-write cycle and delayed write cycle, either t_{DZC} (min) or t_{DZO} (min) must be satisfied.
5. t_{OFF1} (max), t_{OFF2} (max), t_{SHZ} (max) and t_{SLZ} (min) are defined as the time at which the output acheives the open circuit condition (V_{OH} – 100 mV, V_{OL} + 100 mV). This parameter is sampled and not 100% tested.
6. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 1 TTL loads and 50 pF.
8. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
9. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
10. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.
11. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
12. These parameters are specified by the later falling edge of $\overline{CAS}$ or $\overline{WEU}$ and $\overline{WEL}$.
13. Either t_{CDD} (min) or t_{ODD} (min) must be satisfied because the output buffer must be turned off by $\overline{CAS}$ or $\overline{OE}$ before data is applied to the device when the output buffer is on.
14. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min) in read-modify-write cycle, the data of the selected address outputs to an I/O pin and input data is written into the selected address. t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{OE}$ prior to applying data to the device.
15. Measured with a load circuit equivalent to 1 TTL loads and 30 pF.
16. After power-up, pause for 100 µs or more and execute at least 8 initialization cycles (normal memory cycle or refresh cycle), then start operation. Hitachi recommends that 8 initialization cycle is CBRR for internal register reset.
17 When t_{SHZ} and t_{SLZ} are measured in the same V_{CC} and Ta conditions and tr and tf of $\overline{SE}$ are less than 5 ns, $t_{SHZ} \leq t_{SLZ} + 5$ ns.
18. When both $\overline{WEU}$ and $\overline{WEL}$ go low at the same time, all 16 bits of data are written into the device. $\overline{WEU}$ and $\overline{WEL}$ cannot be staggered within the same write cycle.

Timing Waveforms

Read Cycle



Page Mode Read Cycle



Write Cycle

Table 2, the write cycle state table, applies to early write, delayed write, page mode write, and read-modify write.

Table 2 Write Cycle State

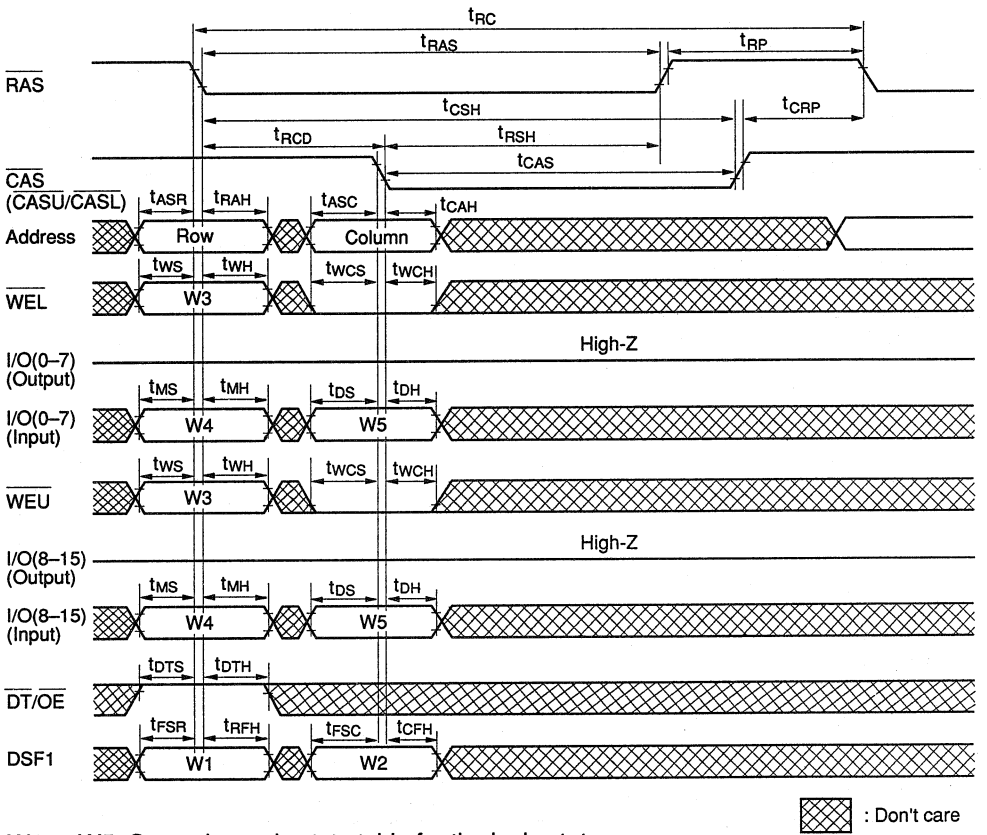
		$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{RAS}$	$\overline{CAS}$
		DSF1	DSF1	$\overline{WEU}$, $\overline{WEL}$	I/O	I/O
MNEU	Cycle	W1	W2	W3	W4	W5
RWM	Write mask (new/old) Write DQs to I/Os	0	0	0	Write mask (Note 1)	Valid data
BWM	Write mask (new/old) Block write	0	1	0	Write mask (Note 2)	Column mask (Note 2)
RW	Normal write (no mask)	0	0	1	Don't care (Note 1)	Valid data
BW	Block write (no mask)	0	1	1	Don't care (Note 2)	Column mask (Note 2)
LMR	Load write mask resister	1	0	1	Don't care	Write mask data (Note 3)
LCR	Load color resister	1	1	1	Don't care	Color data

Notes: 1. I/O mask data (in new mask mode)
Low: Masked
High: Not masked
In persistent mask mode, I/O is don't care.

$\overline{WEU}$, $\overline{WEL}$	Mode	I/O Data/$\overline{RAS}$
Either low	New mask mode	Mask
	Persistent mask mode	Don't care (mask register used)
Both high	No mask	Don't care

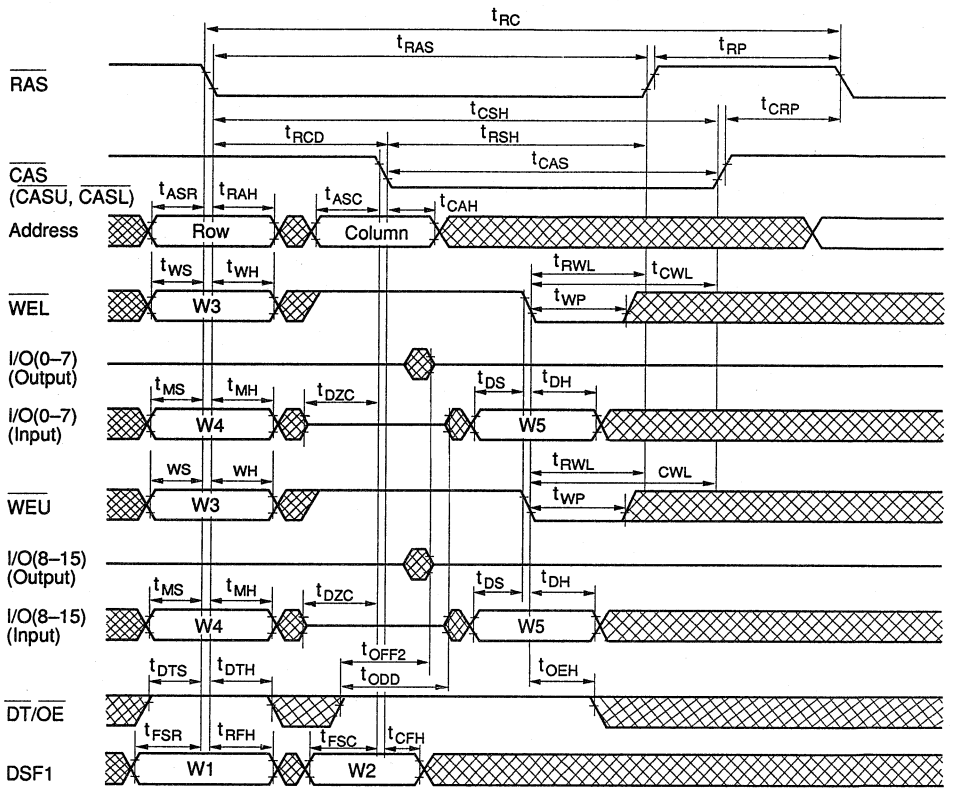
2. See figure 2, use of Block Write
3. I/O write mask data
Low: Masked
High: Not masked

Early Write Cycle



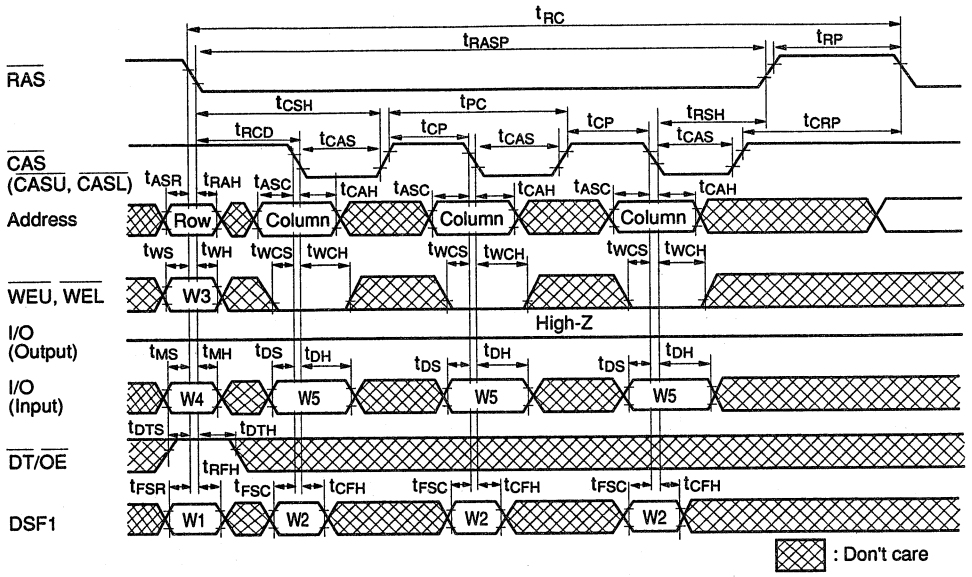
W1 to W5: See write cycle state table for the logic states.

Delayed Write Cycle



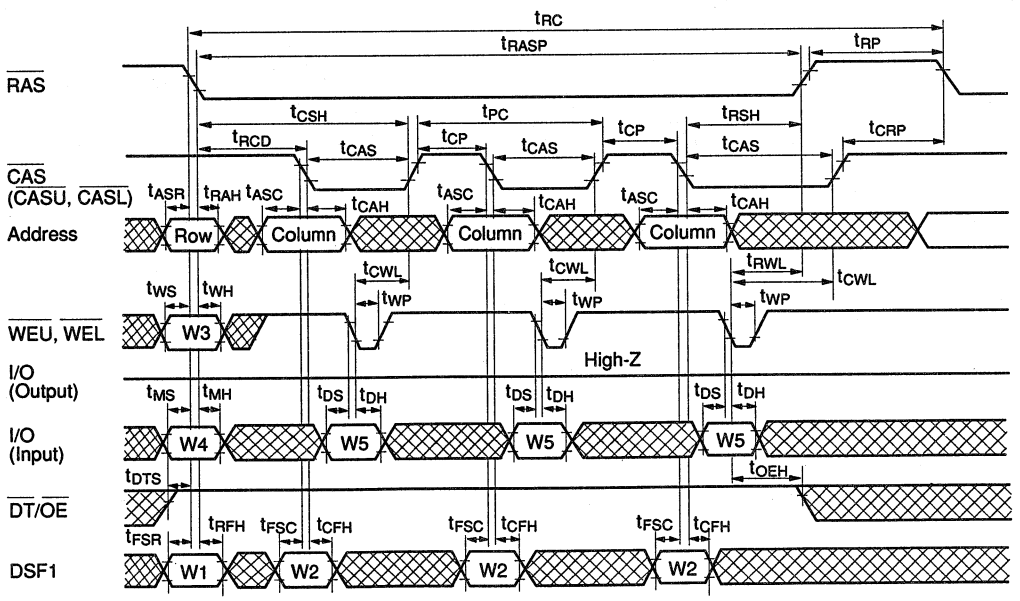
W1 to W5: See write cycle state table for the logic states

Page Mode Write Cycle (Early Write)



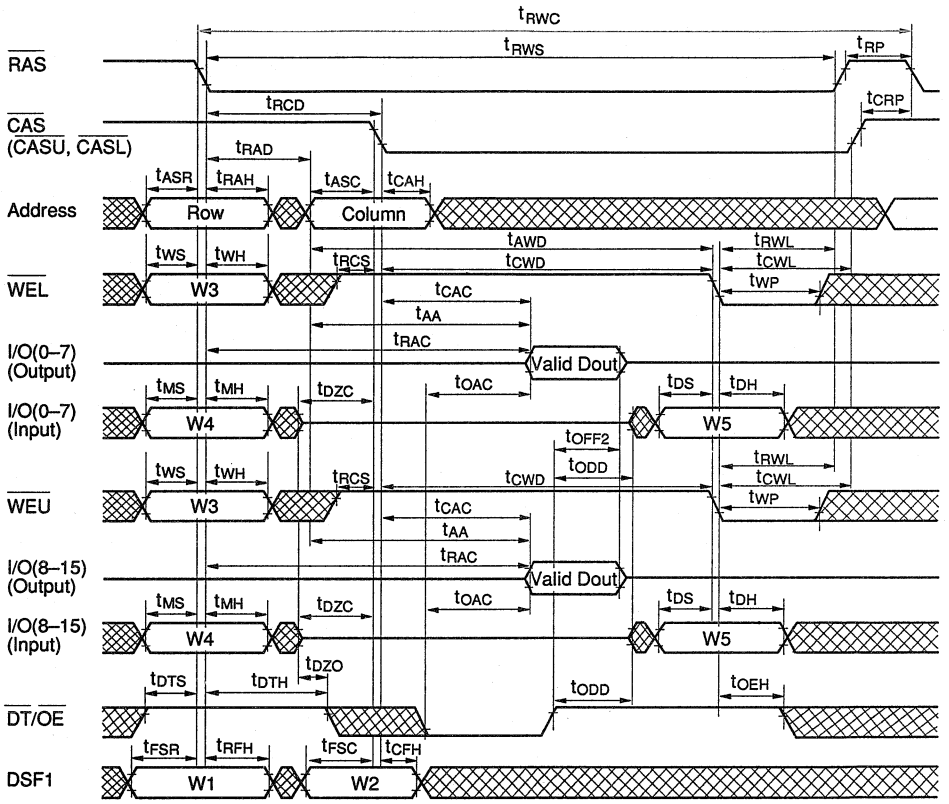
W1 to W5: See write cycle state table for the logic states

Page Mode Write Cycle (Delayed Write)



W1 to W5: See write cycle state table for the logic states

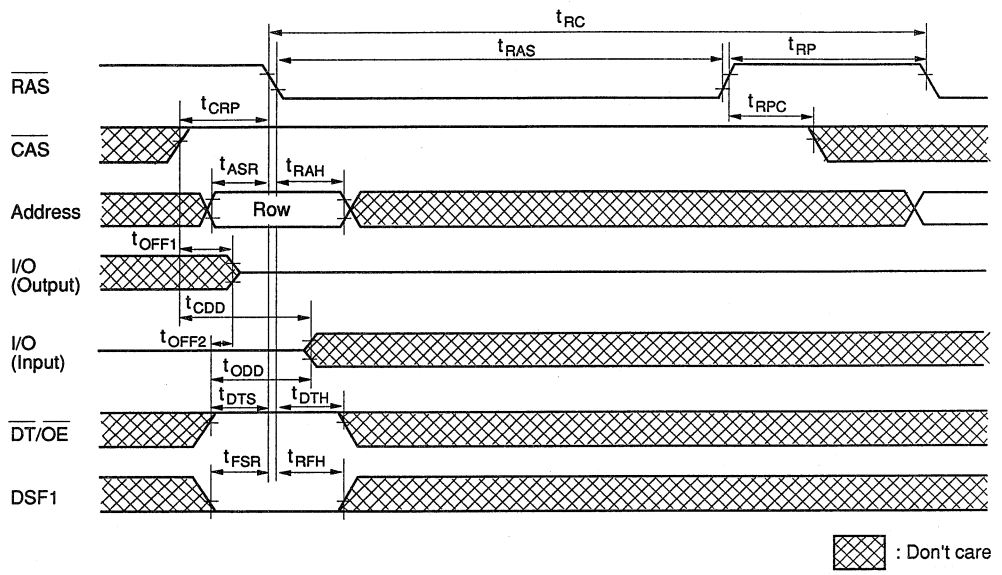
Read-Modify-Write Cycle



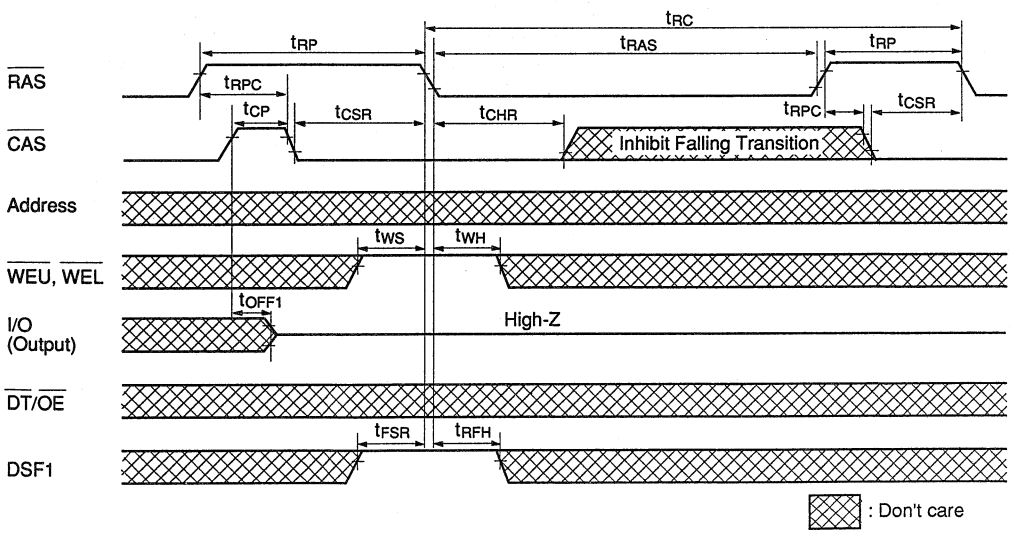
W1 to W5: See write cycle state table for the logic states

: Don't care

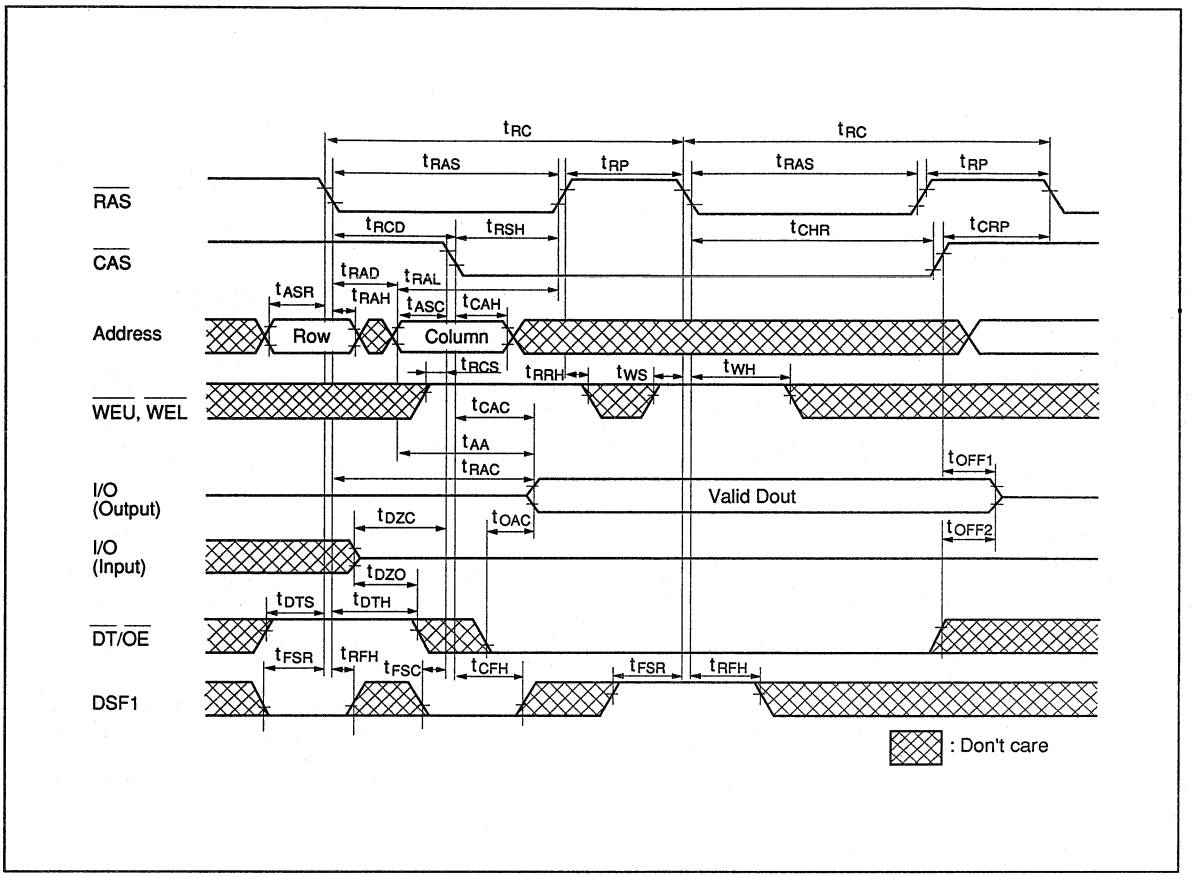
$\overline{\text{RAS}}$-Only Refresh Cycle



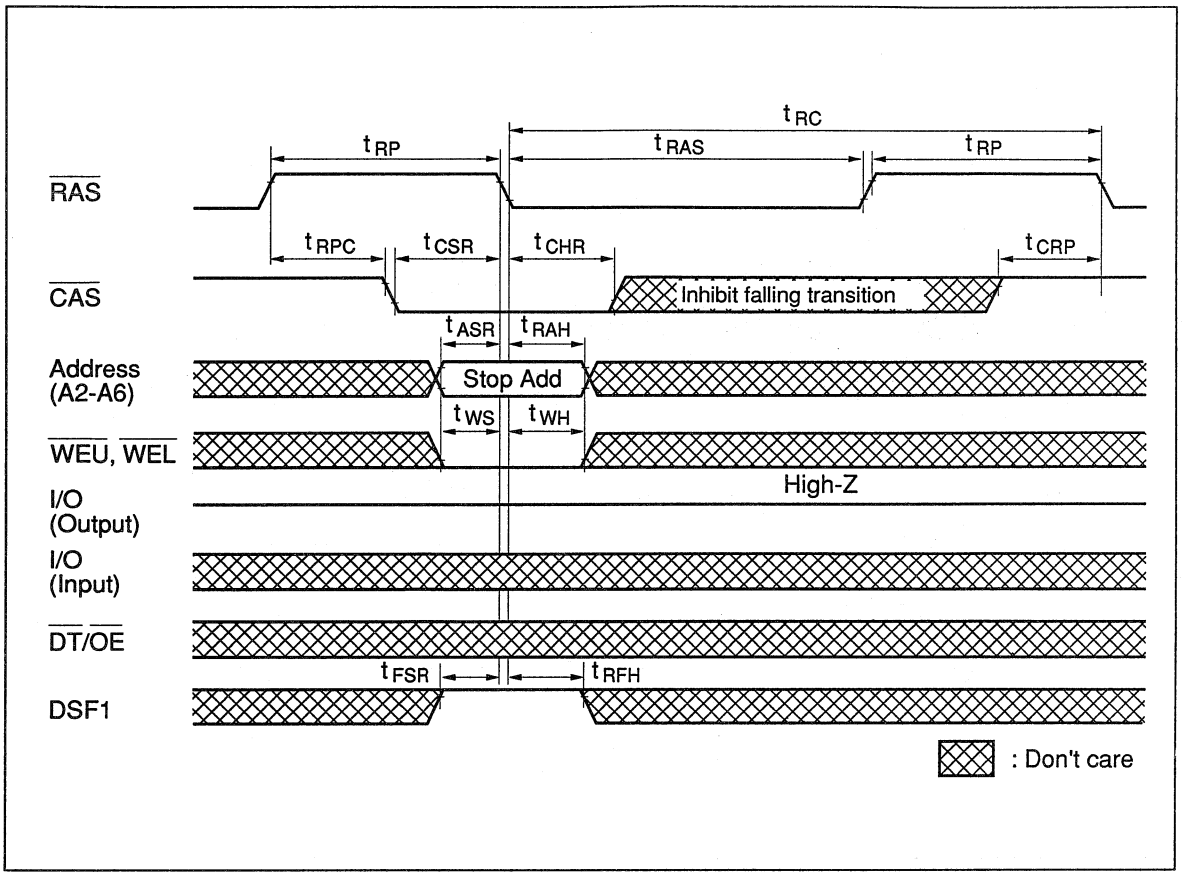
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle (CBRN)



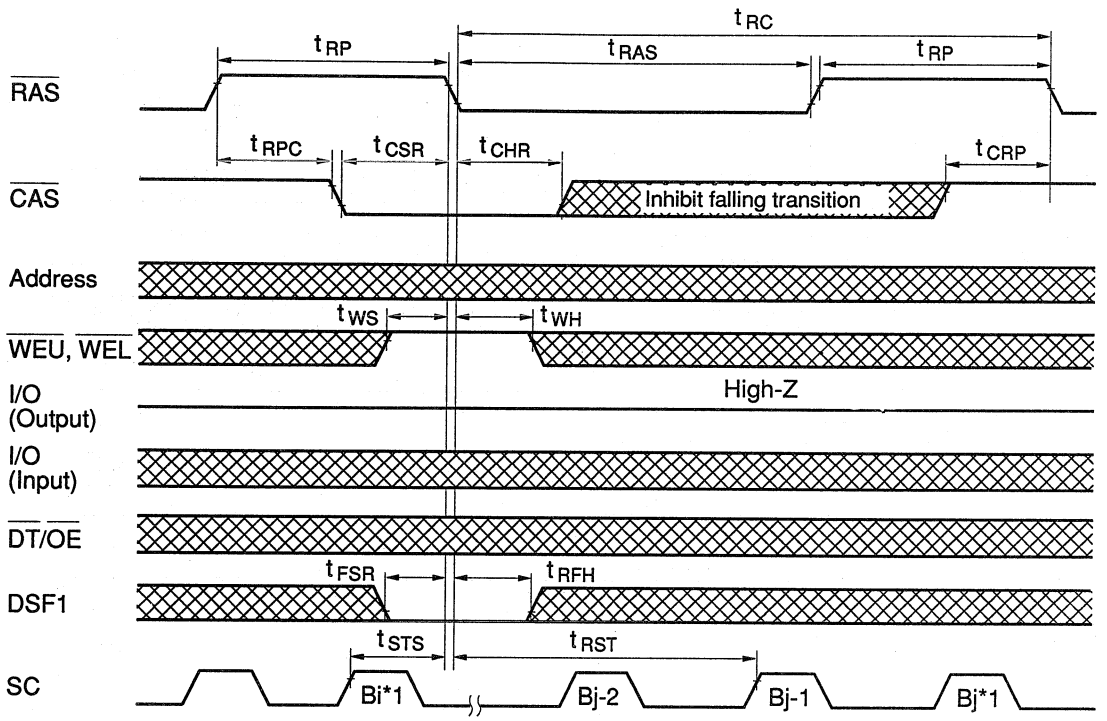
Hidden Refresh Cycle



$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Set Cycle (CBRS)



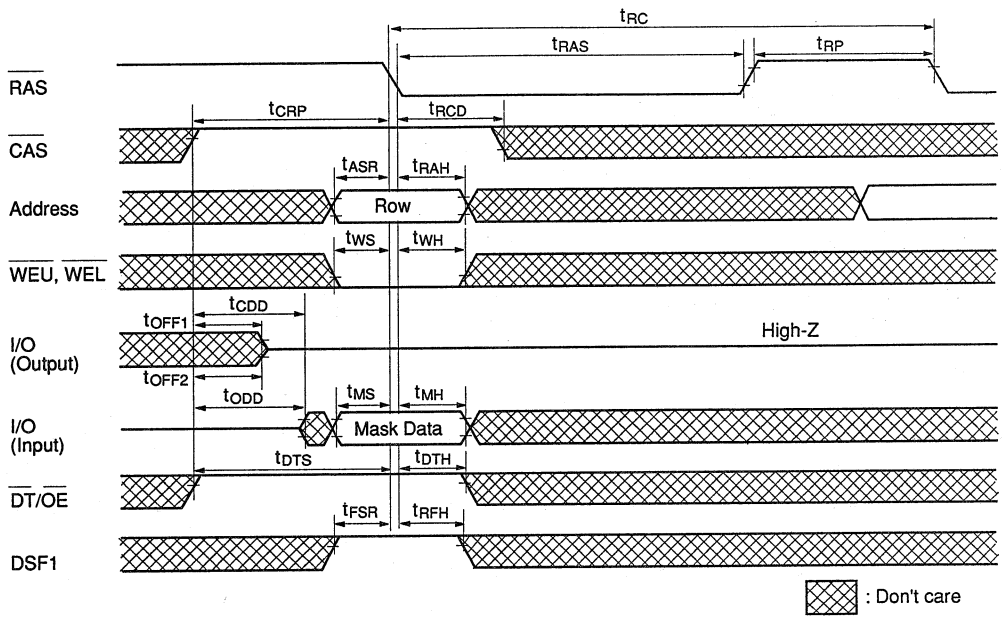
$\overline{CAS}$-Before-$\overline{RAS}$ Reset Cycle (CBRR)



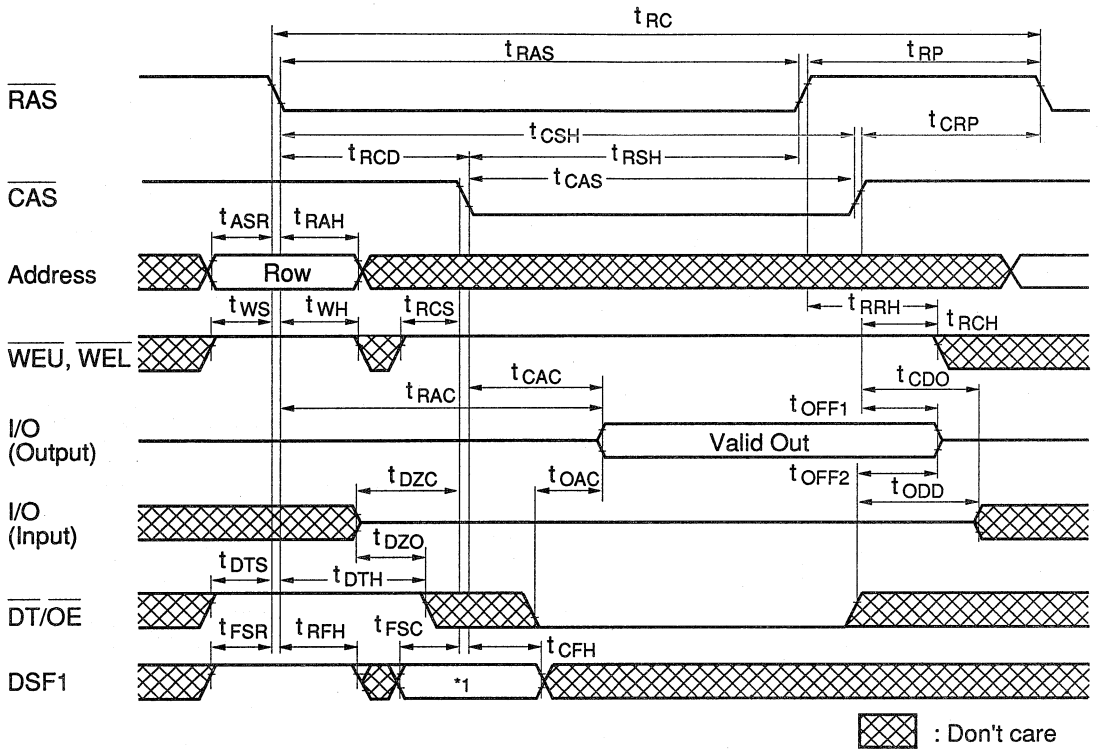
Note: 1. Bi, Bj initiate the boundary addresses.

: Don't care

Flash Write Cycle



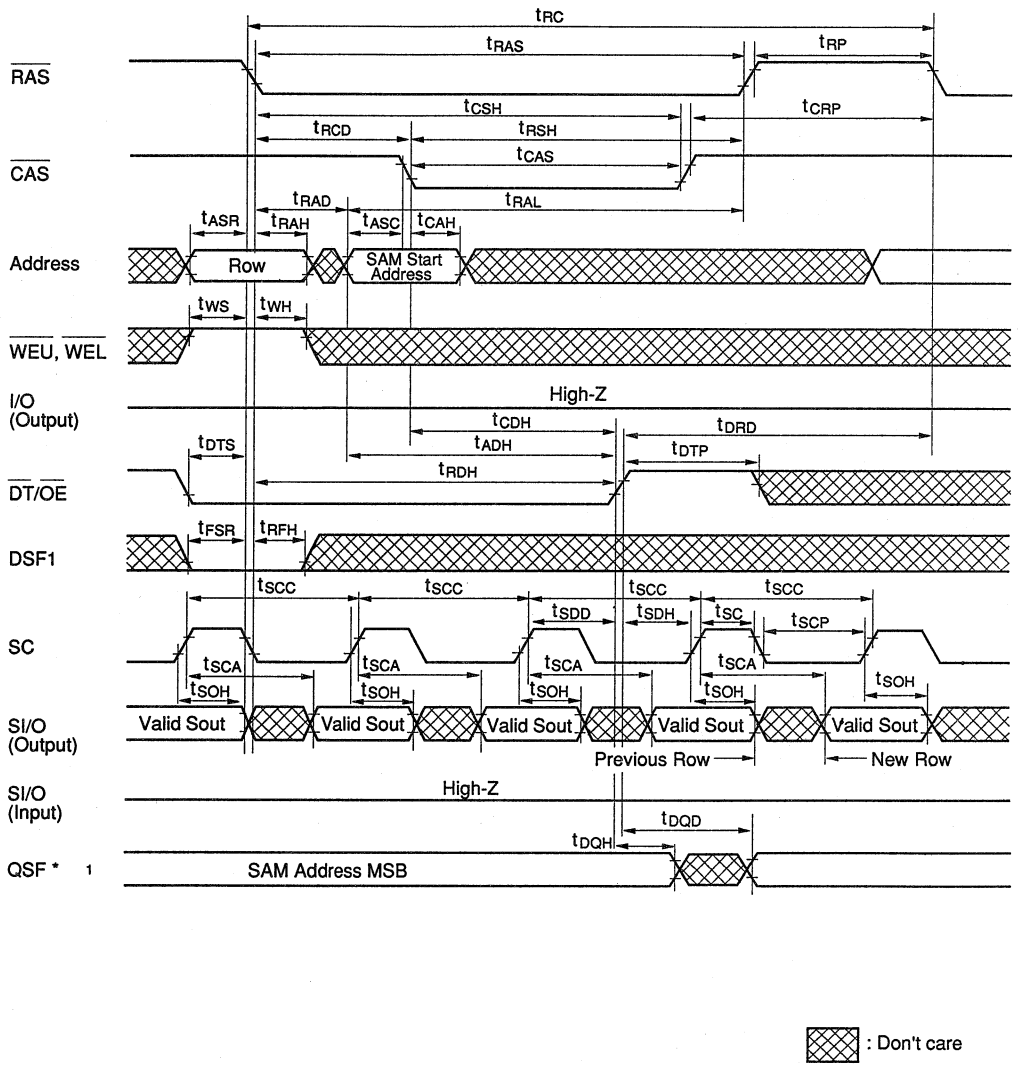
Register Read Cycle (Mask Data, Color Data)



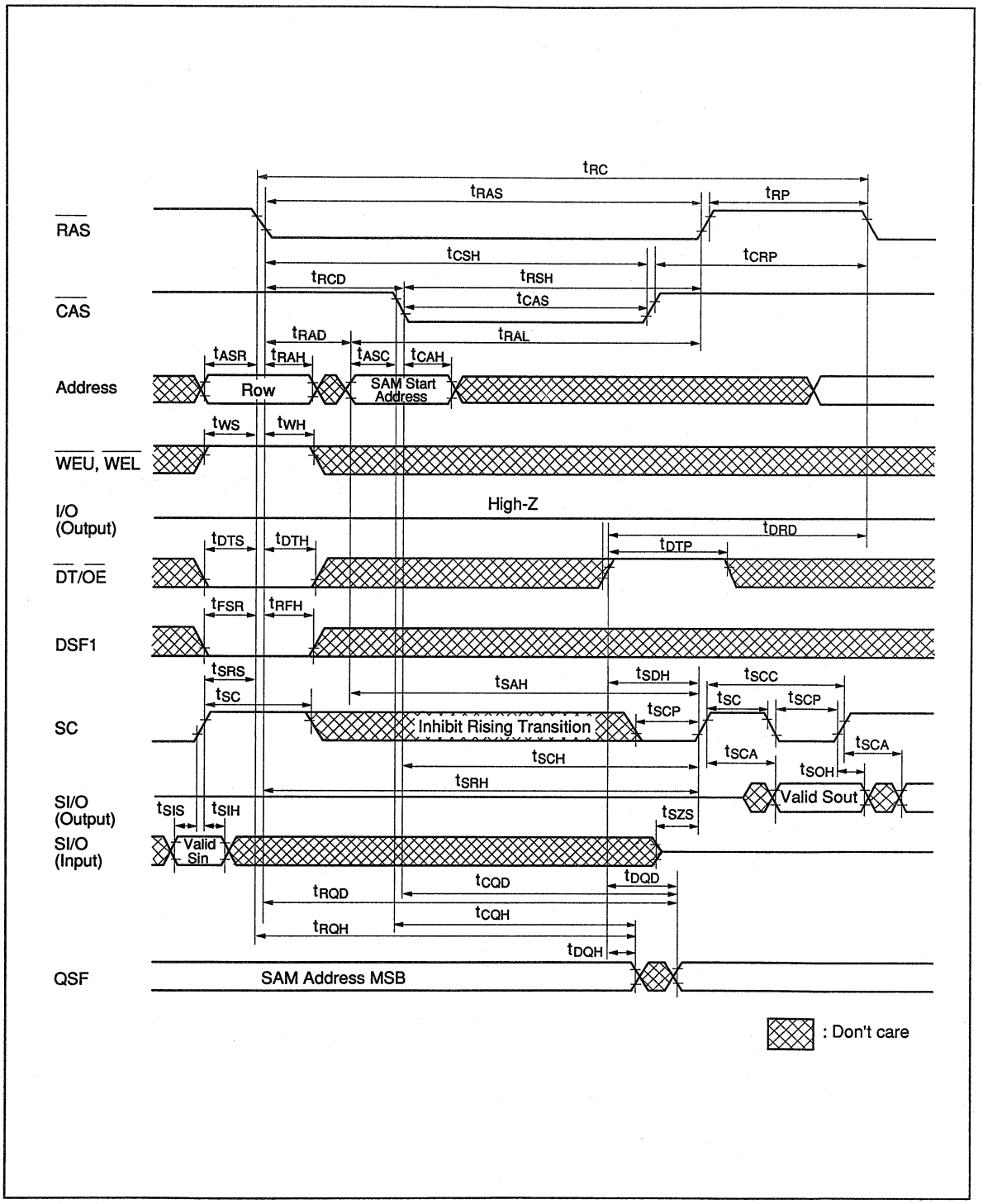
Note: 1. State of DSF1 at falling edge of $\overline{CAS}$

State	0	1
Accessed data	Mask data (LMR)	Color data (LCR)

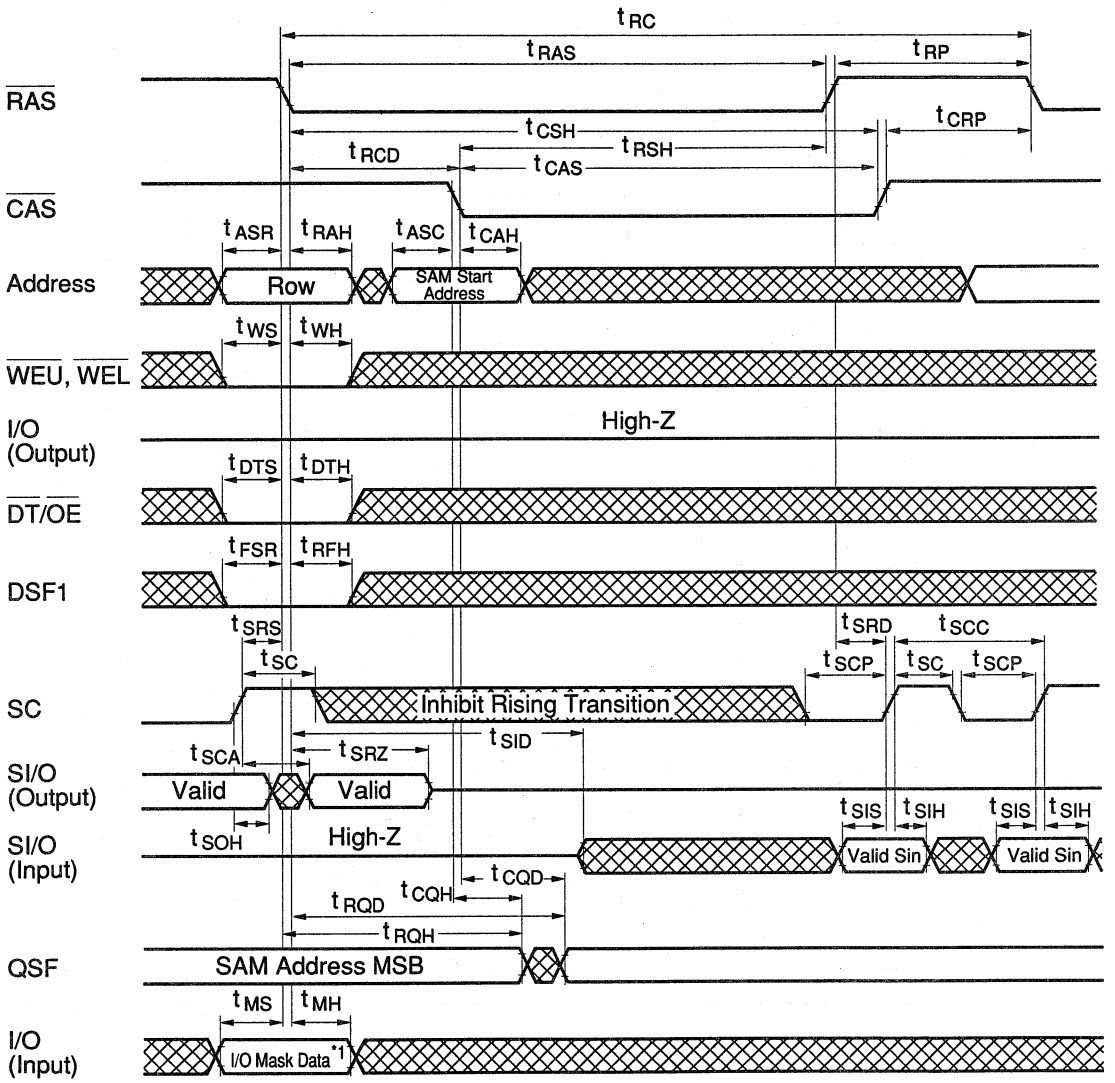
Read Transfer Cycle 1



Read Transfer Cycle 2



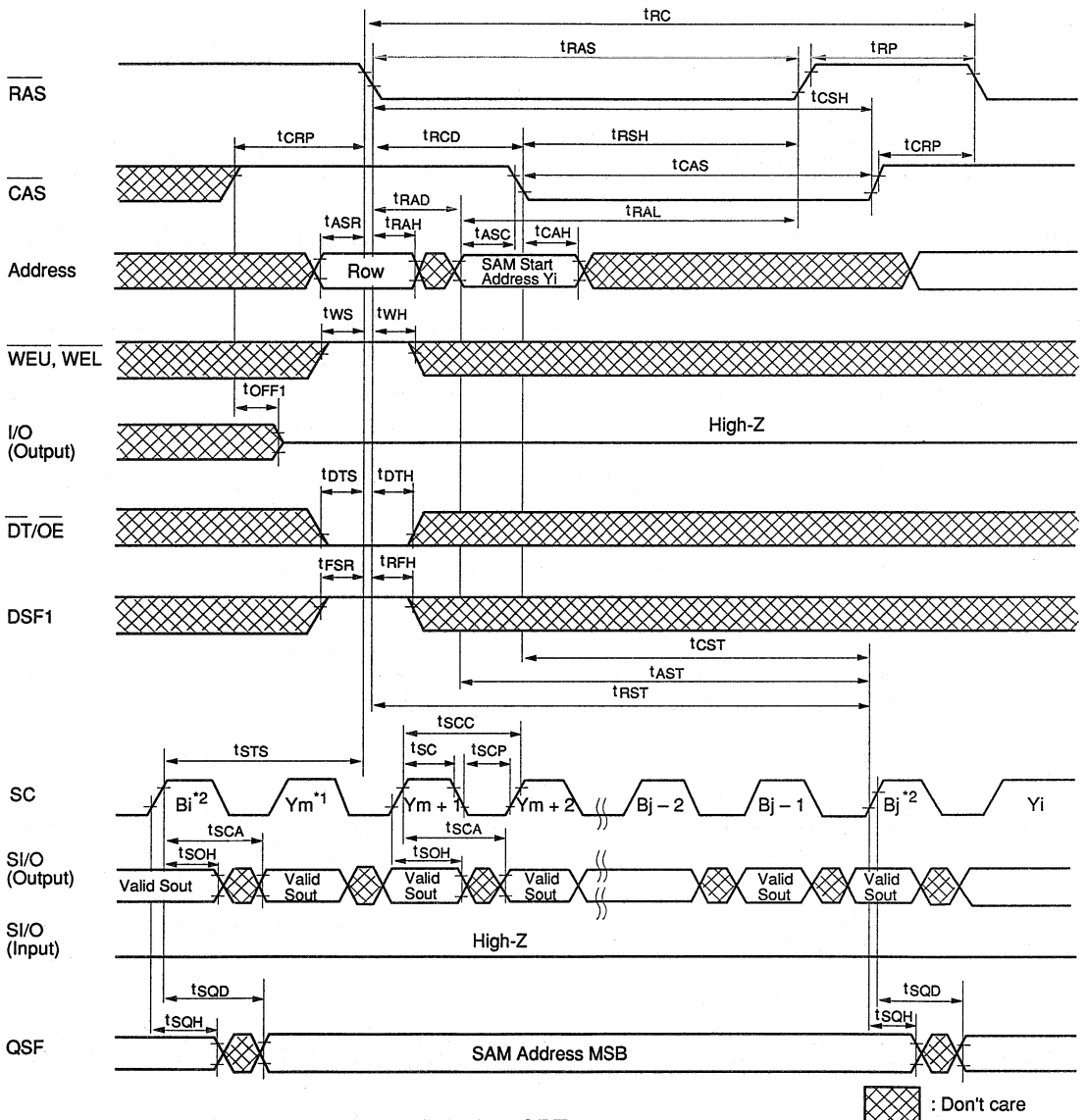
Masked Write Transfer Cycle



Note: 1. I/O mask data (In new mask mode)
Low: Mask
High: Non mask
I/O: Don't care in persistent mask mode.

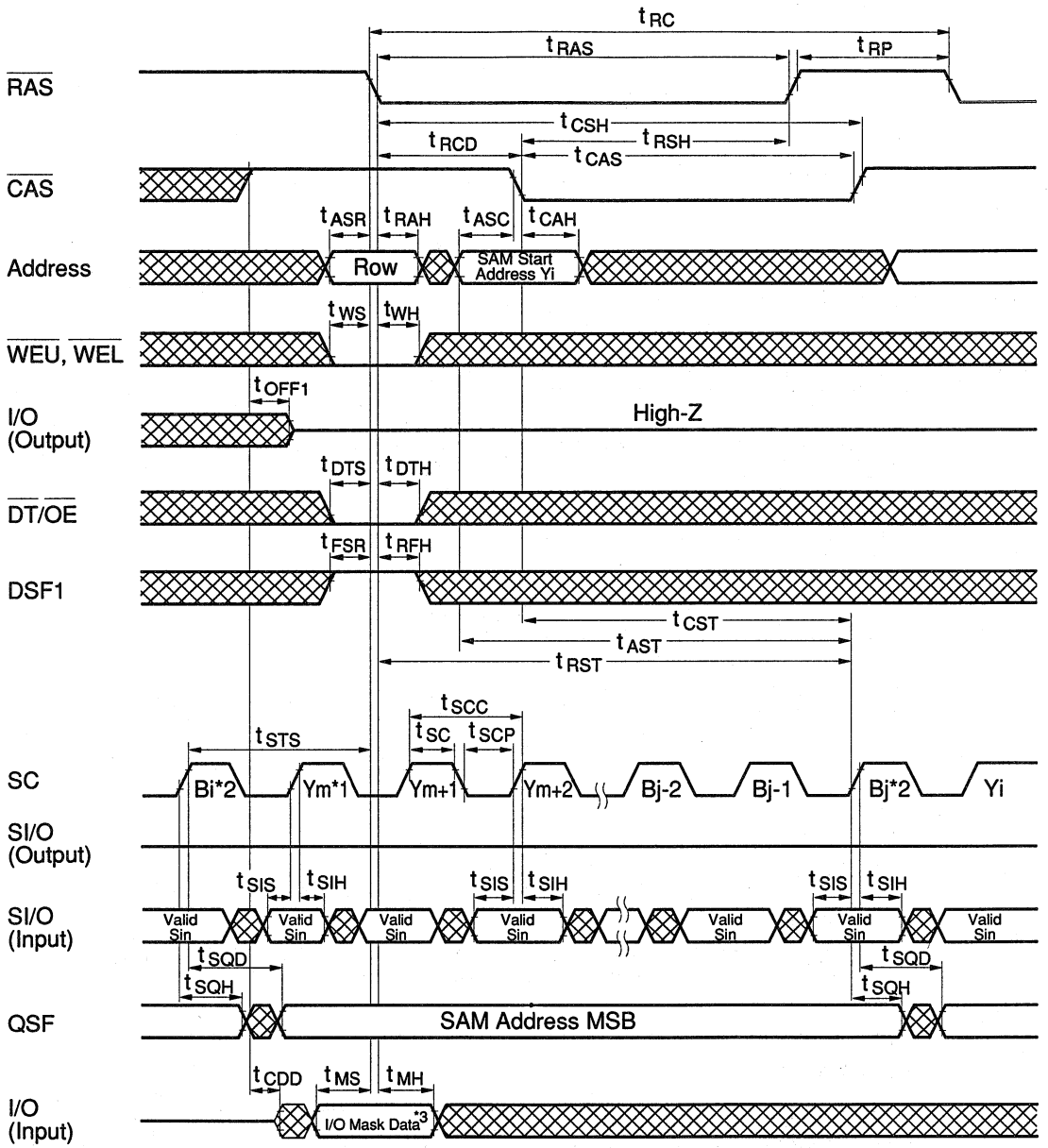
: Don't care

Split Read Transfer Cycle



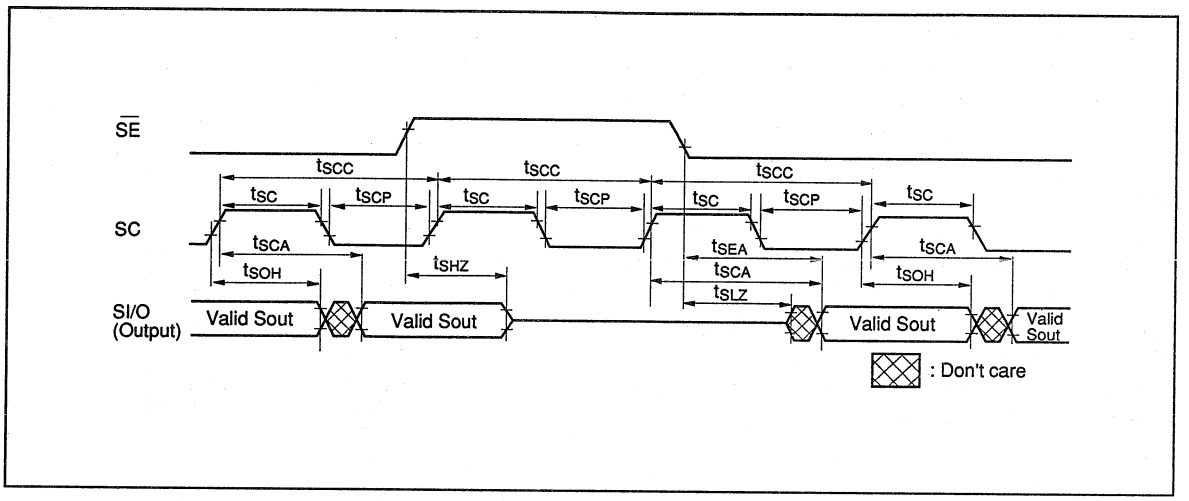
Notes: 1. Ym is the SAM start address in before SRT.
2. Bi, Bj initiate the boundary address.

Masked Split Write Transfer Cycle

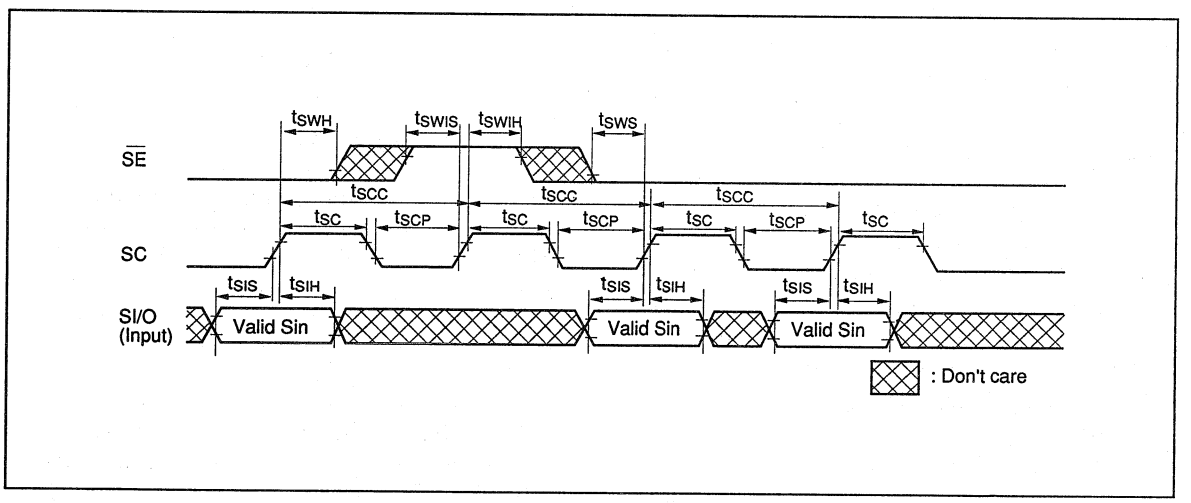


Notes: 1. Ym is the SAM start address in before SRWT.
2. Bi, Bj initiate the boundary address.
3. I/O Mask data (In new mask mode)
Low: Mask
High: Non mask
I/O: Don't care in persistent mask mode.

Serial Read Cycle



Serial Write Cycle



HM63921 Series

2048-word × 9-Bit CMOS Parallel In-Out FIFO Memory

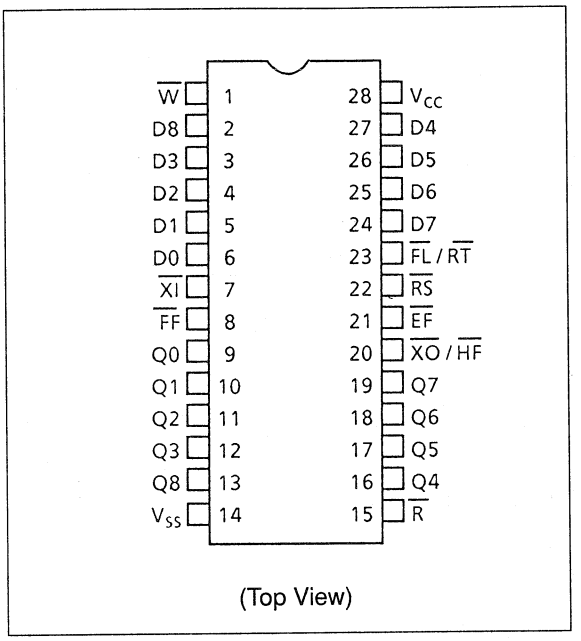
The HM63921 is a first-in, first-out memory that utilizes a high performance static RAM array with internal algorithm that controls, monitors and declares status of the memory by empty flag, full flag and half-full flag, to prevent data overflow or underflow.

Expansion logic warrants unlimited expansion capability in width and depth. Both read and write are independent from each other and their corresponding pointers are designed to select the proper locations out of the entire array serially without address information to load or unload data. Data is toggled in and out of the device through the use of the write enable ($\overline{W}$) and read enable ($\overline{R}$) pins. The device has a read/write cycle time of 30/35/45 ns. Organization of HM63921 provides a 9-bit data bus. The ninth bit could be used for control or parity for error checking at the option of the user. The HM63921 is fabricated using the Hitachi CMOS 1.3 micron technology. The device is available in DIP and SOJ.

Features

- First-in, first-out dual port memory
- 2 k × 9 organization
- Low-power CMOS 1.3 micron technology
- Asynchronous and simultaneous read and write
- Fully expandable in depth and/or width
- Single 5 V (± 10%) power supply
- Empty and full warning flags
- Half-full flag
- Access time: 20/25/35 ns
- Package: 300-mil 28-pin plastic DIP package
  300-mil 28-pin plastic SOJ package

Pin Arrangement



(Top View)

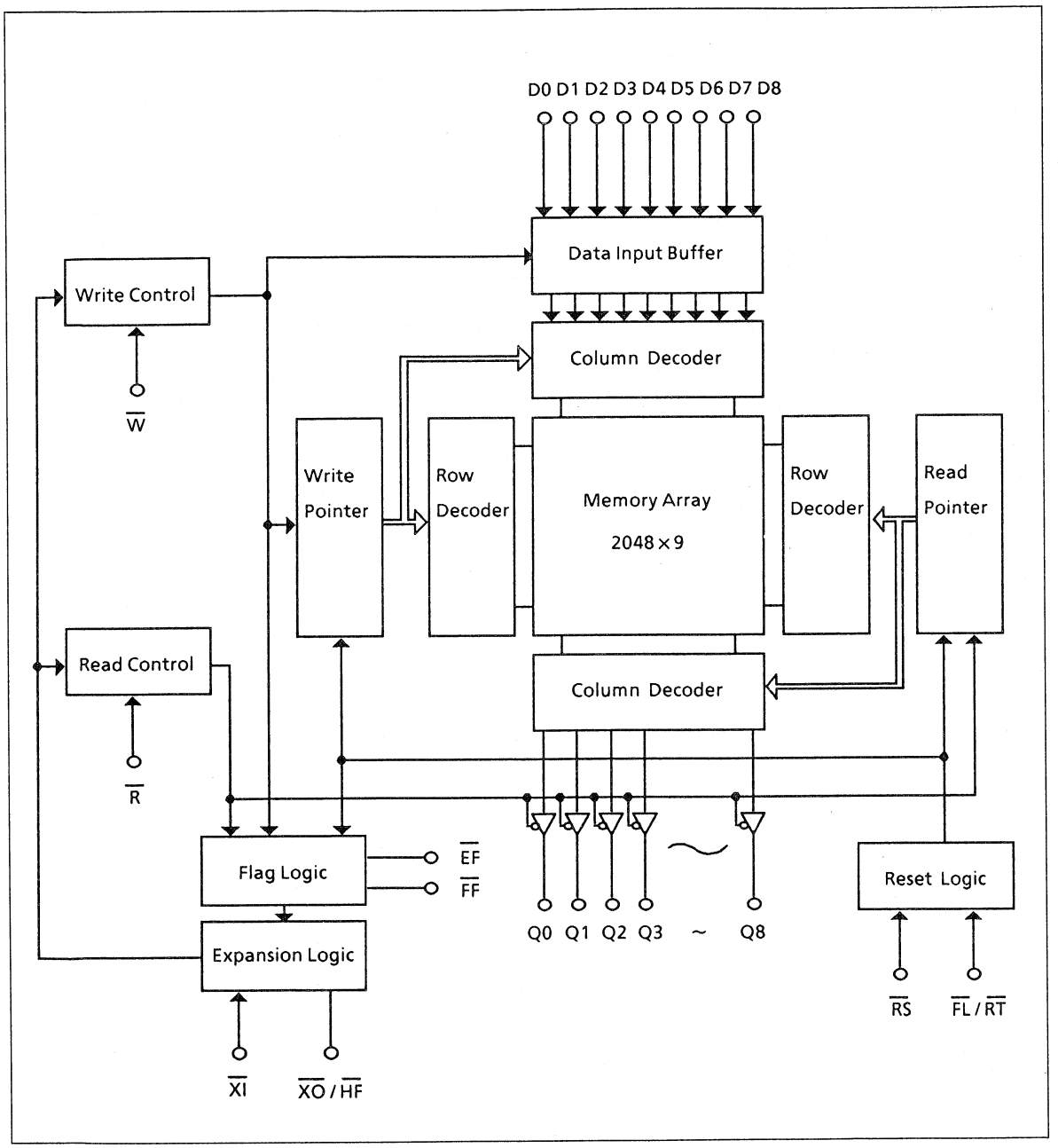
Ordering Information

Type name	Access time	Package
HM63921P-20	20 ns	300-mil 28-pin plastic DIP (DP-28NA)
HM63921P-25	25 ns	
HM63921P-35	35 ns	
HM63921JP-20	20 ns	300-mil 28-pin plastic SOJ (CP-28DN)
HM63921JP-25	25 ns	
HM63921JP-35	35 ns	

Pin Description

Pin name	Function
D0 – D8	Data inputs
$\overline{RS}$	Reset
$\overline{W}$	Write enable
$\overline{R}$	Read enable
$\overline{FL}$	First load
$\overline{RT}$	Retransmit
$\overline{XI}$	Expansion-in
$\overline{XO}$	Expansion-out
$\overline{HF}$	Half-full flag
$\overline{FF}$	Full flag
$\overline{EF}$	Empty flag
Q0 – Q8	Data outputs

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage *1	V_T	–0.5 *2 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Notes: 1. Relative to V_{SS}
2. –3.5 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.4	—	6.0	V
	V_{IL}	–0.5 *1	—	0.8	V

Note: 1. –3.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol		Min	Typ	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$		—	—	2	µA	V_{CC} = 5.5 V, Vin = 0 V – V_{CC}
Output leakage current (Q0–Q8 pins)	$\|I_{LO}\|$		—	—	2	µA	$\overline{R}$ = V_{IH}, Vout = 0 V – V_{CC}
Operating power supply current	I_{CC1}	–20	—	—	120	mA	Average operating current Min cycle, I_{OUT} = 0 mA
		–25	—	—	110	mA	
		–35	—	—	100	mA	
Standby power supply current	I_{SB1}		—	—	10	mA	$\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$ /$\overline{RT}$ = V_{IH}
	I_{SB2}		—	—	1	mA	All inputs ≥ V_{CC}–0.2 V or ≤ 0.2 V

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%) (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4 mA
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA

Capacitance (Ta = 25°C, f = 1 MHz)

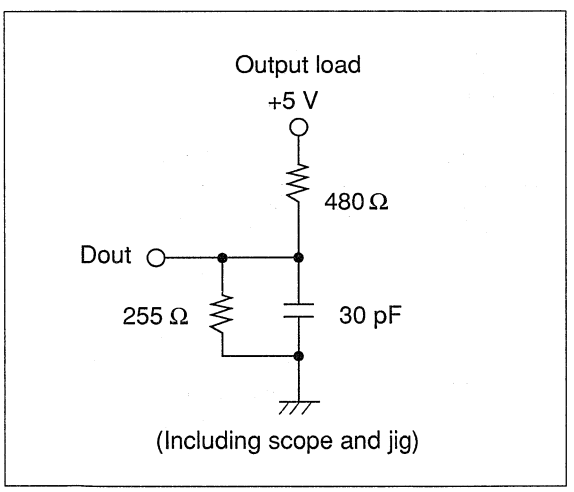
Parameter	Symbol	Typ	Max	Unit	Test conditons
Input capacitance	Cin	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	10	pF	Vout = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

Test Conditions

- Input pulse levels : V_{SS} to 3.0 V
- Input rise and fall times : 5 ns
- Input and output timing reference level : 1.5 V
- Output load : See figure



Read Cycle

		HM63921-20		HM63921-25		HM63921-35		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	30	—	35	—	45	—	ns
Access time	t_A	—	20	—	25	—	35	ns
Read recovery time	t_{RR}	10	—	10	—	10	—	ns
Read pulse width	t_{RPW}	20	—	25	—	35	—	ns
Read low to data outputs low-Z	t_{RLZ}*1	5	—	5	—	5	—	ns
Read high to data outputs high-Z	t_{RHZ}*1	—	15	—	15	—	20	ns
Data valid from read high	t_{OH}	5	—	5	—	5	—	ns
Read pulse width after empty flag high	t_{RPE}	20	—	25	—	35	—	ns
Write high to data outputs low-Z (Read data flow through mode)	t_{WLZ}*1	3	—	3	—	3	—	ns

Note: 1. t_{RLZ}, t_{RHZ} and t_{WLZ} are sampled and not 100% tested.

Write Cycle

		HM63921-20		HM63921-25		HM63921-35		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time	t_{WC}	30	—	35	—	45	—	ns
Write recovery time	t_{WR}	10	—	10	—	10	—	ns
Write pulse width	t_{WPW}	20	—	25	—	35	—	ns
Data setup time	t_{DS}	10	—	15	—	18	—	ns
Data hold time	t_{DH}	0	—	0	—	0	—	ns
Effective write pulse width after full flag high	t_{WPF}	20	—	25	—	35	—	ns

Reset Cycle

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min	Max	Min	Max	Min	Max	
Reset cycle time	t_{RSC}	30	—	35	—	45	—	ns
Reset pulse width	t_{RS}	25	—	25	—	35	—	ns
Reset setup time	t_{RSS}	20	—	25	—	35	—	ns
Reset recovery time	t_{RSR}	10	—	10	—	10	—	ns
Read low to reset low delay time	t_{RRD}	20	—	25	—	35	—	ns
XI high setup time	t_{RXS}	5	—	5	—	5	—	ns
XI high hold time	t_{RXH}	10	—	10	—	10	—	ns

Retransmit Cycle

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min	Max	Min	Max	Min	Max	
Retransmit cycle time	t_{RTC}	30	—	35	—	45	—	ns
Retransmit pulse width	t_{RT}	20	—	25	—	35	—	ns
Retransmit setup time	t_{RTS}	20	—	25	—	35	—	ns
Retransmit recovery time	t_{RTR}	10	—	10	—	10	—	ns
Read low to retransmit low delay time	t_{RTD}	20	—	25	—	35	—	ns

Flag Timing

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min	Max	Min	Max	Min	Max	
Reset to empty flag low	t_{EFL}	—	25	—	30	—	40	ns
Reset to full flag high	t_{FFH}	—	25	—	30	—	40	ns
Reset to expansion out/half-full flag high	t_{HFH}	—	25	—	30	—	40	ns
Retransmit to empty flag high	t_{TEF}	—	25	—	30	—	40	ns
Retransmit to full flag high/low	t_{TFF}	—	25	—	30	—	40	ns
Retransmit to half-full flag high/low	t_{THF}	—	40	—	45	—	50	ns
Read low to empty flag low	t_{REF}	—	20	—	25	—	35	ns
Read high to full flag high	t_{RFF}	—	20	—	25	—	35	ns
Write high to empty flag high	t_{WEF}	—	20	—	25	—	35	ns
Write low to full flag low	t_{WFF}	—	20	—	25	—	35	ns
Write low to half-full flag low	t_{WHF}	—	30	—	35	—	45	ns
Read high to half-full flag high	t_{RHF}	—	30	—	35	—	45	ns

Expansion Timing

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min	Max	Min	Max	Min	Max	
Read/write low to expansion out low	t_{XOL}	—	15	—	20	—	30	ns
Read/write high to expansion out high	t_{XOH}	—	15	—	20	—	30	ns
Expansion in pulse width	t_{XI}	20	—	25	—	35	—	ns
Expansion in recovery time	t_{XIR}	10	—	10	—	10	—	ns
Expansion in setup time	t_{XIS}	12	—	15	—	15	—	ns

Signal Description

Inputs

- Reset ($\overline{RS}$)

The device is reset whenever $\overline{RS}$ input is taken to low state, for minimum reset pulse width. When device is reset, both read and write pointers are set to the first location. A reset cycle is required after power on. Both read enable ($\overline{R}$) and write enable ($\overline{W}$) inputs must be in the high state during reset. Empty flag ($\overline{EF}$) will go low and full flag ($\overline{FF}$) and half-full ($\overline{HF}$) will go high during reset cycle.

- Write enable ($\overline{W}$)

Write cycle is initiated at the falling edge of $\overline{W}$, if the full flag ($\overline{FF}$) is not set, provided that data set-up and hold time requirements relative to the rising edge of $\overline{W}$ are met. Data is stored in the device sequentially and independently of any simultaneous read operation. To inhibit further write operations and prevent internal data overflow full flag ($\overline{FF}$) will go low.

- Read enable ($\overline{R}$)

Read cycle is initiated at the falling edge of $\overline{R}$, if the empty flag ($\overline{EF}$) is not set. Data is accessed on a first-in, first-out basis independently of simultaneous write operation. As read enable ($\overline{R}$) goes high, all outputs will return to high impedance state, till next read operation. After the last data been read from the FIFO, the empty flag ($\overline{EF}$) will go low, preventing further read operations with output kept in high impedance state. Empty flag ($\overline{EF}$) will go high during a valid write cycle (t_{WEF}), thereafter a valid read can start.

- First load/retransmit ($\overline{FL}/\overline{RT}$)

For depth expansion mode, this pin is grounded to indicate that it is the first device, while this pin of the rest of devices should connect to V_{CC} for correct operation. In single device mode, this pin resets the read pointer to the beginning of the FIFO memory, therefore data can be reread from the beginning. Both $\overline{R}$ and $\overline{W}$ should be kept high while $\overline{RT}$ is taken low.

- Expansion-in ($\overline{XI}$)

For single device mode expansion-in ($\overline{XI}$) is grounded. For depth expansion mode, expansion-in ($\overline{XI}$) should be connected to expansion-out ($\overline{XO}$) of previous device.

- Data-In (D0 to D8)

Data inputs for 9-bit wide data.

Outputs

- Full flag ($\overline{FF}$)

The full flag ($\overline{FF}$) will go low when FIFO is full, inhibiting further write operations until one or more read operations are completed or the FIFO is reset.

- Empty flag ($\overline{EF}$)

The empty flag ($\overline{EF}$) will go low when the FIFO becomes empty, inhibiting further read operations, until one or more write operations are completed, or FIFO is set to retransmit.

- Expansion-out ($\overline{XO}$)/half-full flag ($\overline{HF}$)

This output has dual functionality depending how it is used. In depth expansion configuration expansion-out ($\overline{XO}$) is connected to next expansion-in ($\overline{XI}$). The expansion-out ($\overline{XO}$) of the last FIFO is connected to the expansion-in ($\overline{XI}$) of the first FIFO. In this way the first FIFO indicates the next FIFO that it will receive the next data. In like manner, any FIFO which becomes full will indicate the next FIFO that it will receive the next data. The second function of this output is in stand alone and/or parallel expansion configurations to indicate the system user that the FIFO is half full.

- Data outputs (Q0 to Q8)

Data outputs for 9-bit wide data. These outputs are in high impedance state when $\overline{R}$ is in high state.

Various Operations Mode

- Single device mode

If only one FIFO is used, the expansion-in ($\overline{XI}$) pin should be grounded.

- Width expansion mode

Width expansion by 9-bit increments may be acheived when separately paralleling the data inputs and the data outputs. In this configuration any flags of any device may be used. To avoid output contention of the flags for short period of time, the flag outputs should not be wired together.

- Depth expansion mode

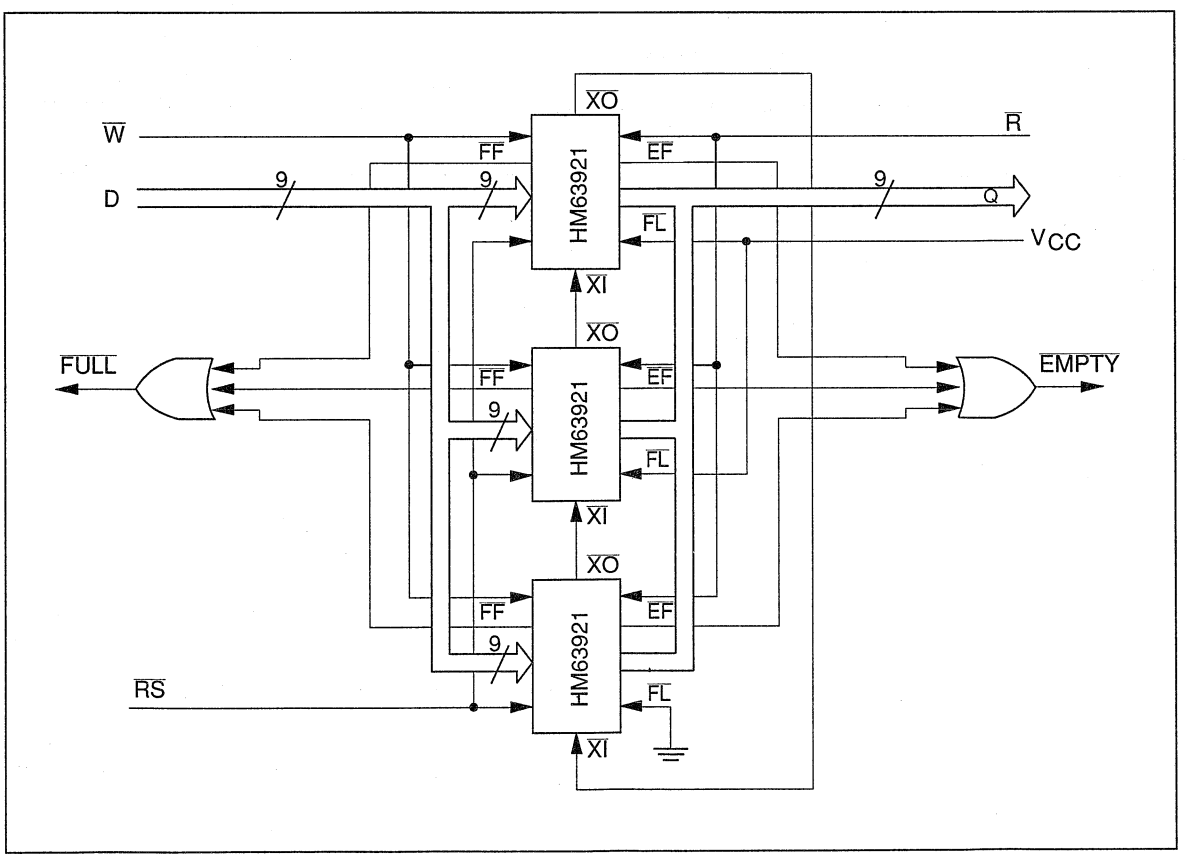
Multiple of FIFOs could provide multiple of 2 k × 9 as (N) × (2 k) by 9-bit wide, where N is the number of FIFOs connected in depth expansion mode. The following arrangement must be provided.

1. First load ($\overline{FL}$) of the first FIFO should be connected to ground.
2. All other ($\overline{FL}$) should be connected to V_{CC}.
3. Connect the expansion-out ($\overline{XO}$) of each FIFO to expansion-in ($\overline{XI}$) of the next FIFO serially and $\overline{XO}$ of the last FIFO to $\overline{XI}$ of the first FIFO.
4. Connect all the empty flag ($\overline{EF}$) together to OR gate and connect all the full flag ($\overline{FF}$) together to OR gate to obtain two separate valid empty flag ($\overline{EF}$) and full flag ($\overline{FF}$) outputs.
5. ($\overline{RT}$) and ($\overline{HF}$) will not be available in this mode.

- Compound expansion mode

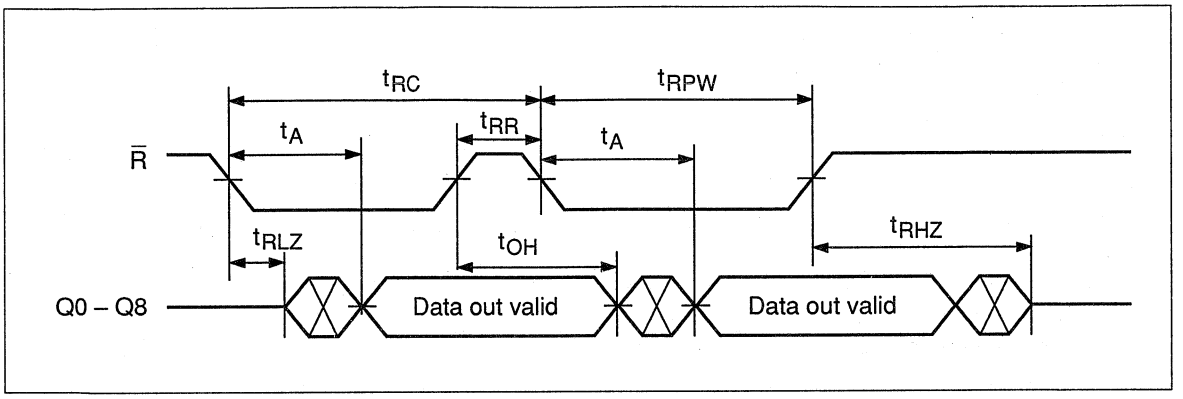
Combination of width and depth expansion modes will provide larger FIFO arrays.

Depth expansion mode

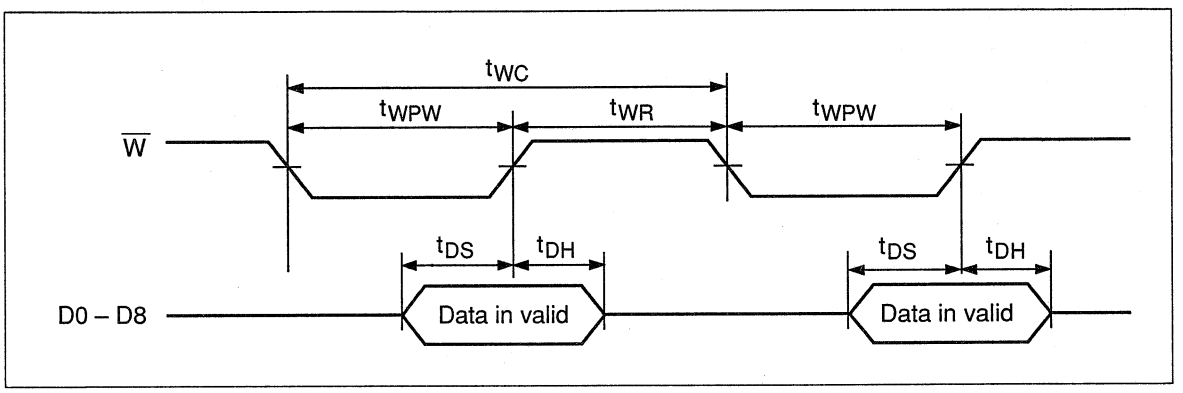


Timing Waveforms

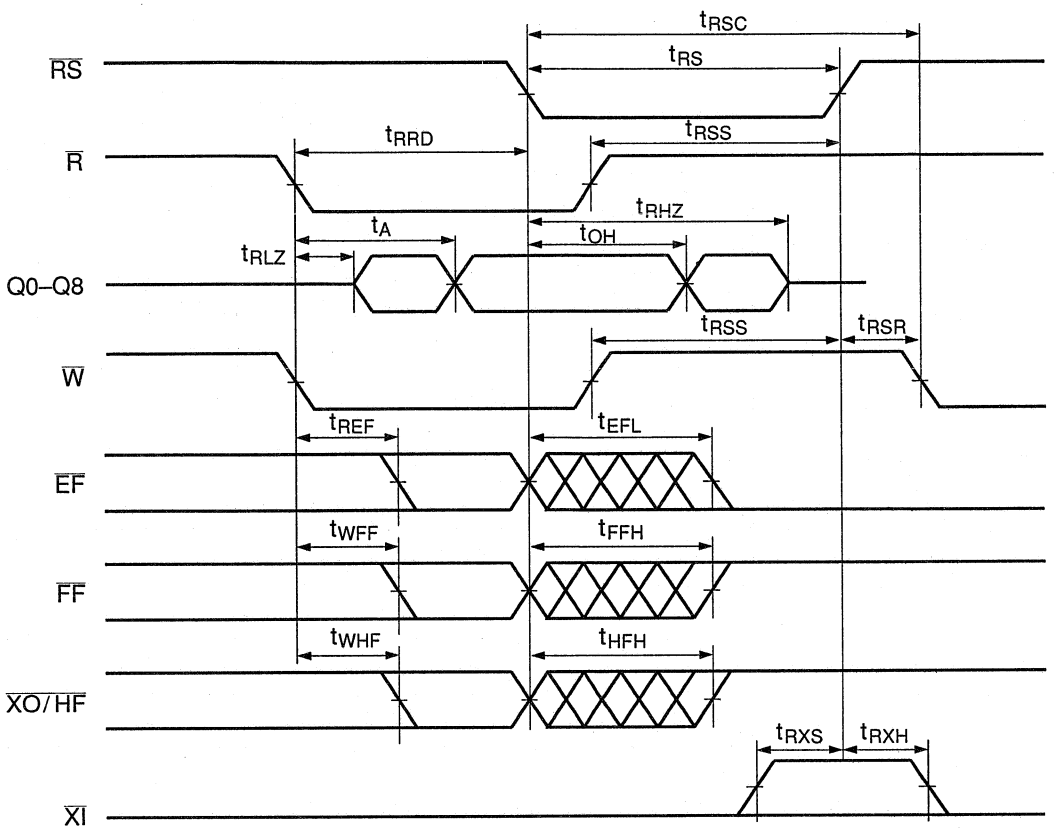
Read Cycle



Write Cycle

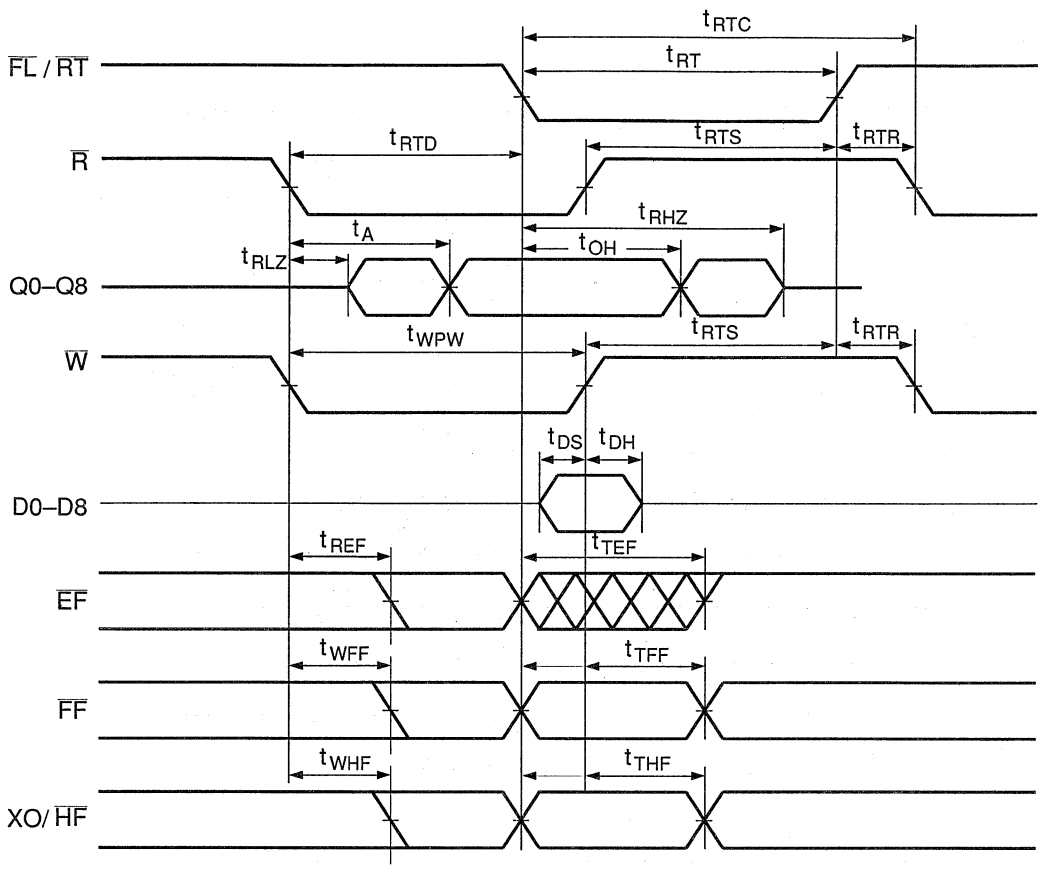


Reset Cycle



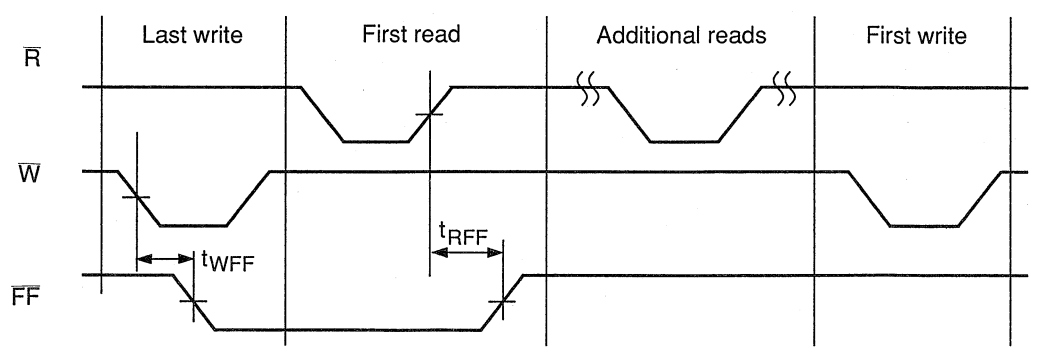
Notes: 1 $t_{RSC} = t_{RS} + t_{RSR}$
2 t_{RXS} and t_{RXH} are parameters only for depth expansion mode.

Retransmit Cycle

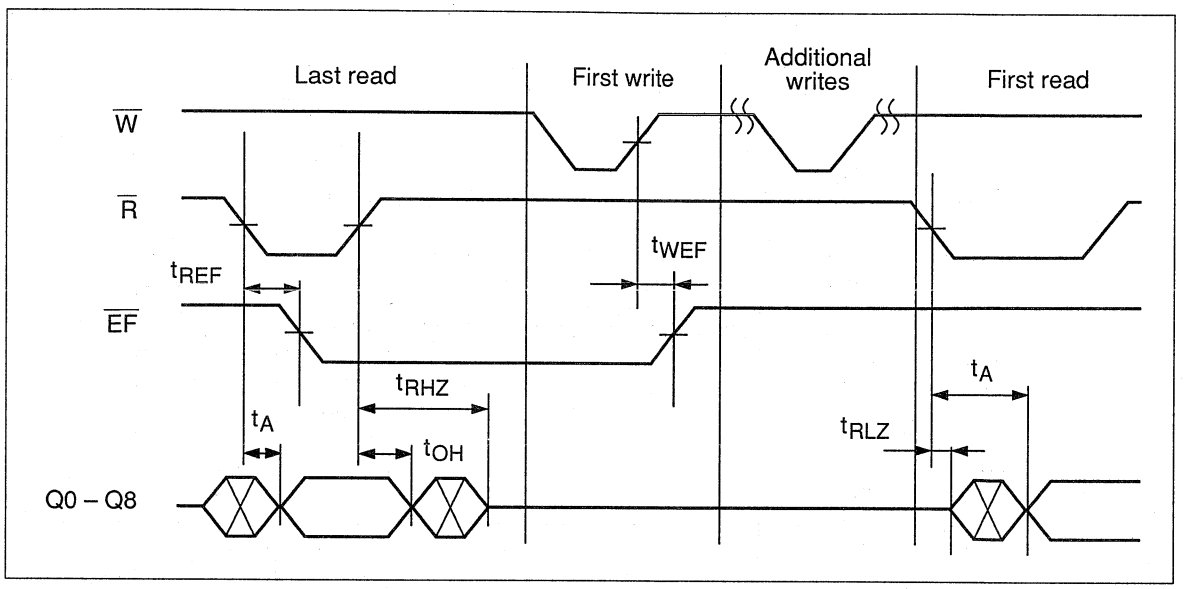


Note: 1 t_{TFF} and t_{THF} are specified by the later timing between $\overline{FL}/\overline{RT}$ falling edge and $\overline{W}$ rising edge.

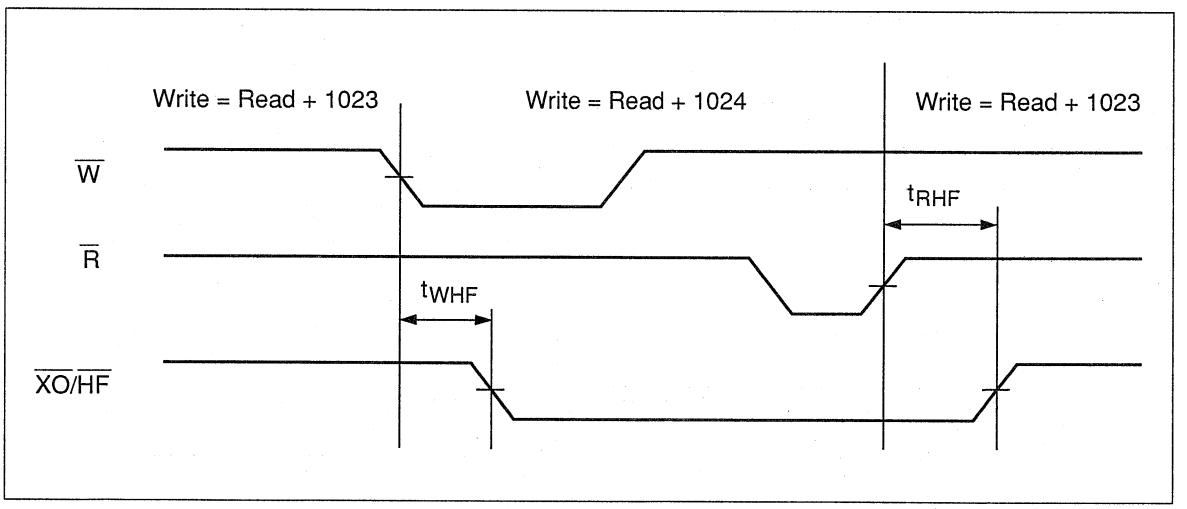
Full-Flag Cycle (From last write to first read)



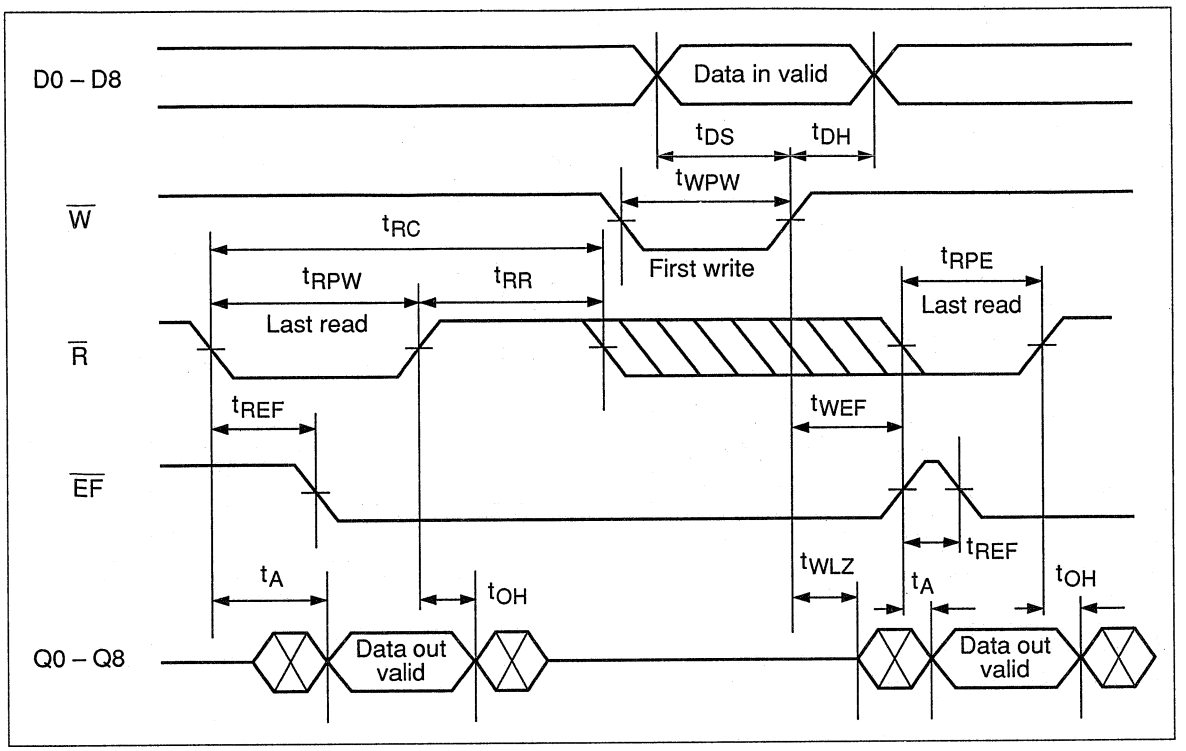
Empty-Flag Cycle (From last read to first write)



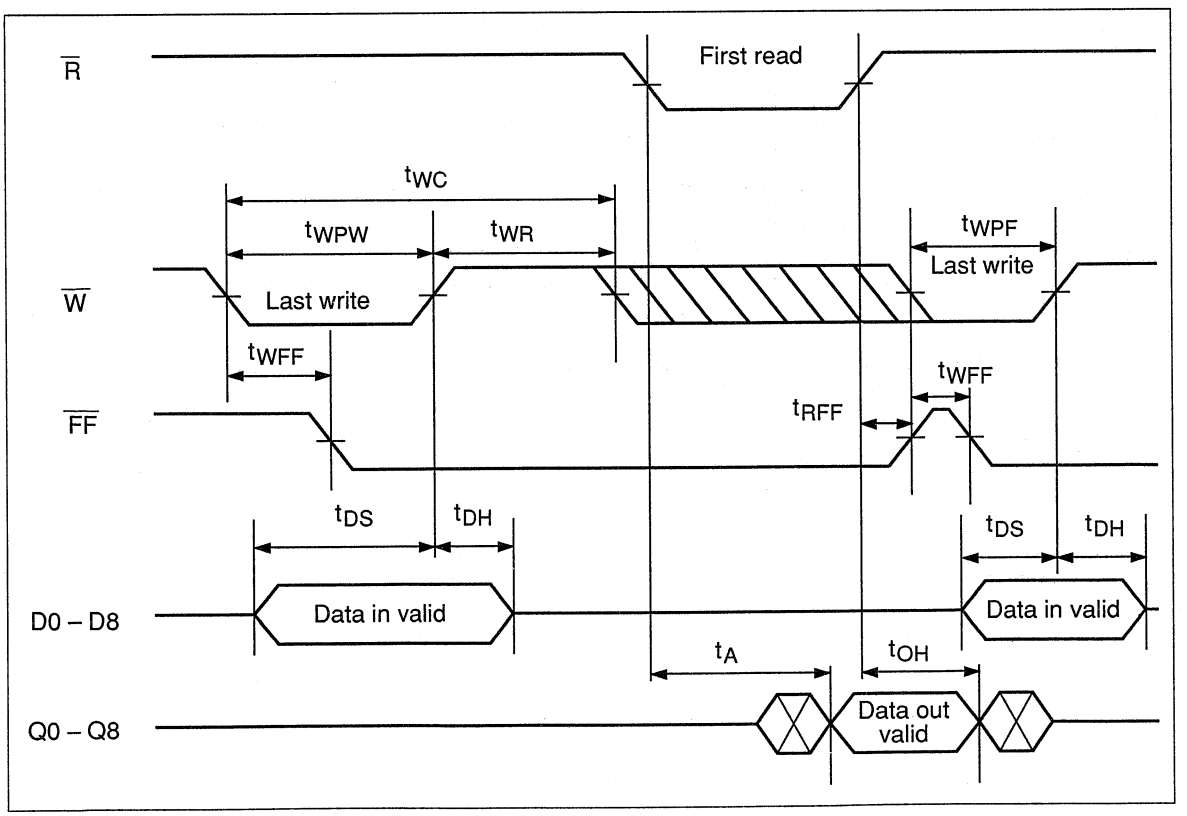
Half-Full Flag Cycle



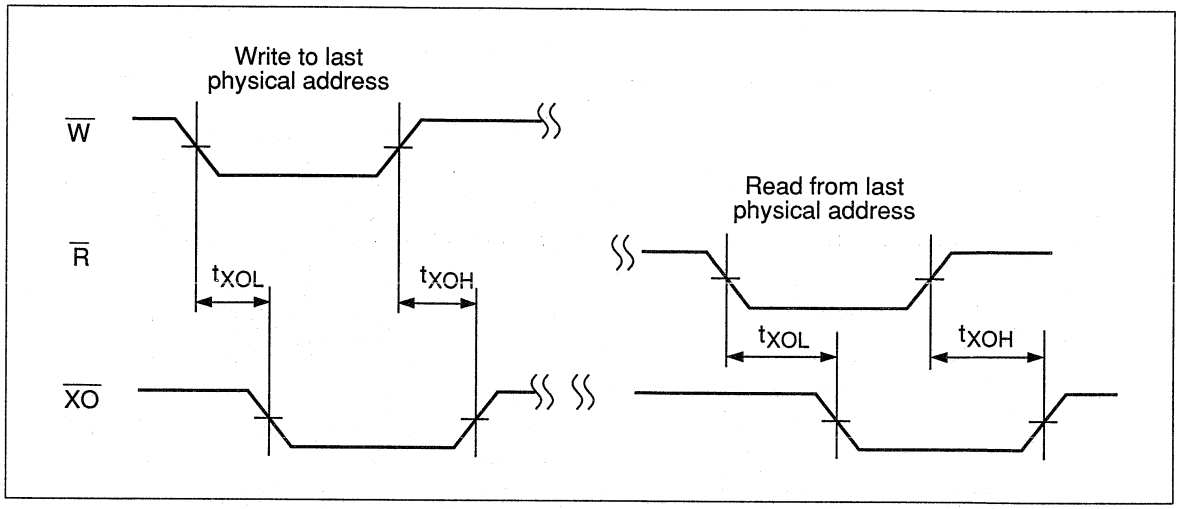
Read Data Flow Through Mode



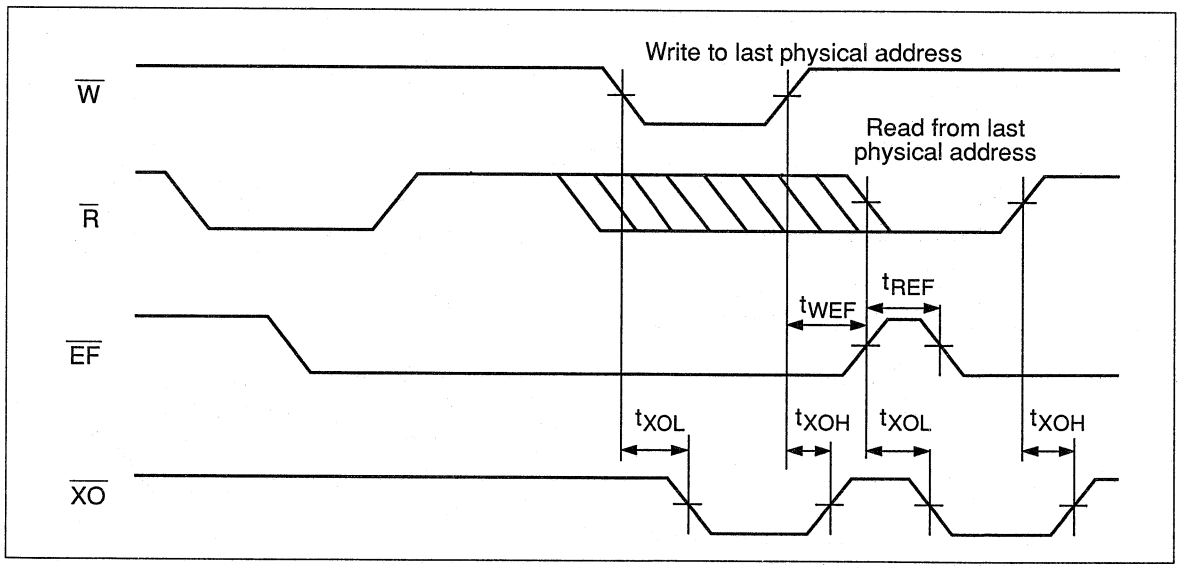
Write Data Flow Through Mode



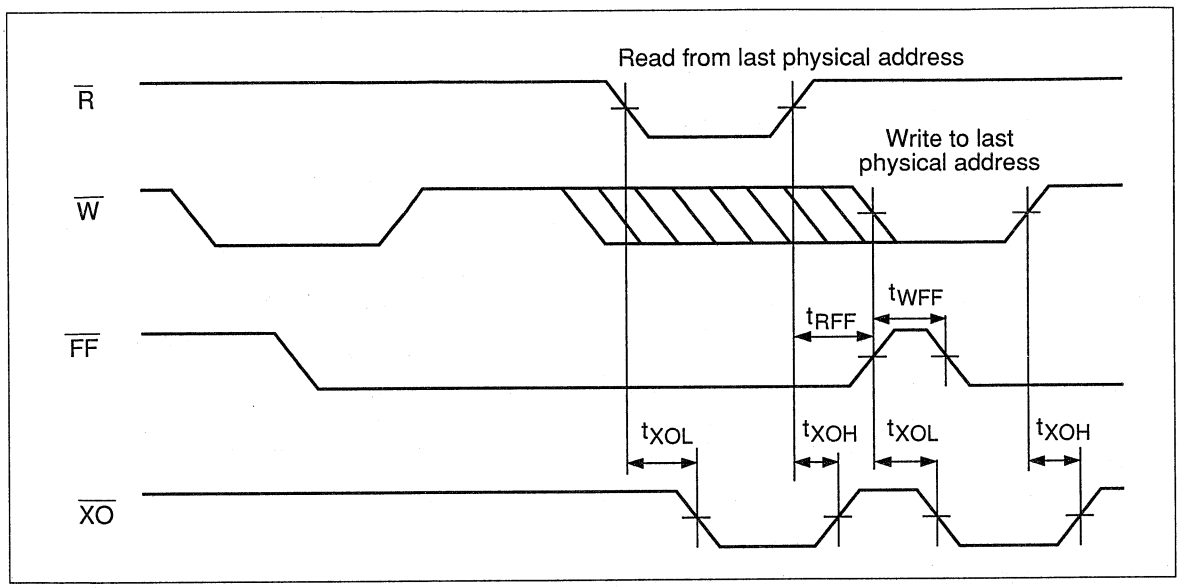
Expansion Out Cycle (1)



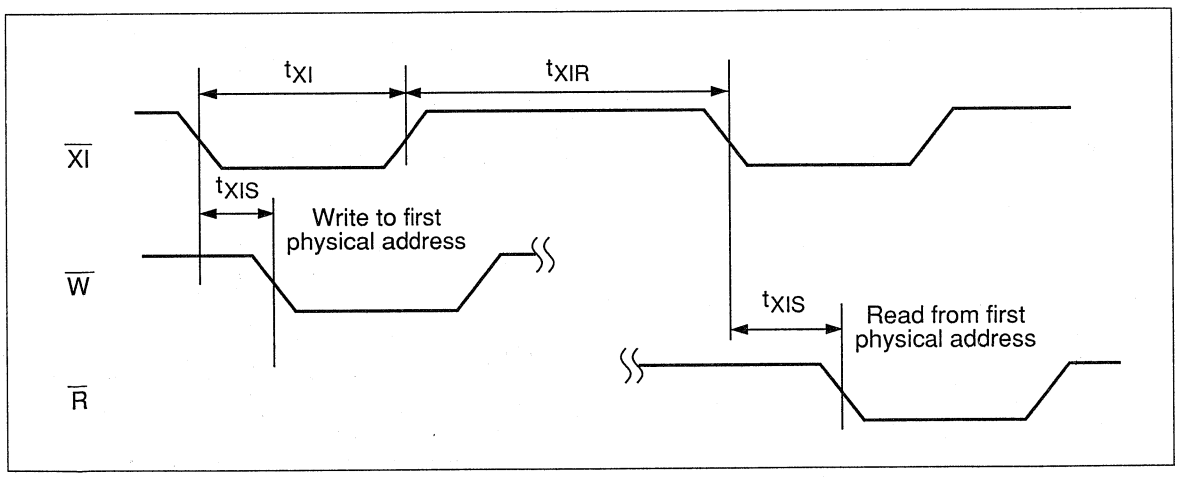
Expansion Out Cycle (2) (Read Data Flow Through Mode)



Expansion Out Cycle (3) (Write Data Flow Through Mode)



Expansion In Cycle



HM62A168, HM62A188 Series

Direct Mapped 8,192-Word × 16 (18)-Bit/2-Way 4,096-Word × 16 (18)-Bit Static Cache Memory

The Hitachi HM62A168(B)/188(B) is a high speed 128 (144)-k cache memory organized as 2-way set associative 4 k × 16 (18) or direct mapped 8 k × 16 (18).

By using two HM62A168(B)/188(B), high performance 32-bit microprocessor system can be achieved.

The HM62A168/188, packaged in a 52-pin PLCC is available for high density mounting.

Features

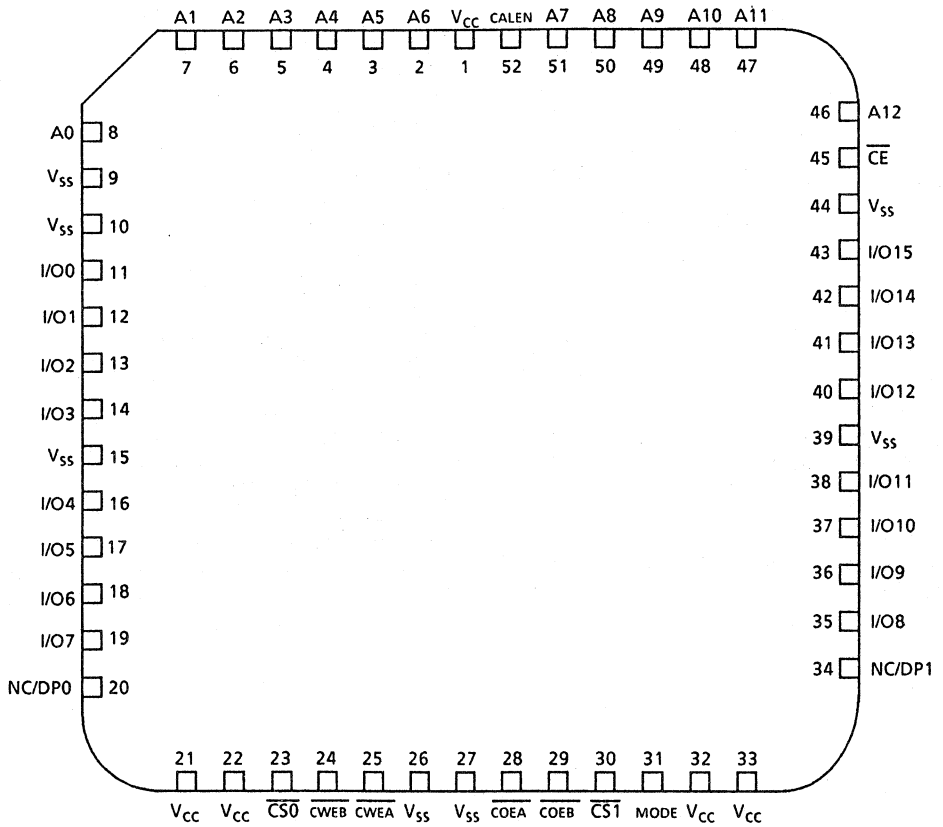
- Single 5 V supply and high density 52-pin PLCC package
- High speed:
  Access time: 25/35 ns (max)
- Directly TTL compatible
  All inputs and outputs
- Address latch
- Pin programmable for 8 k × 16 (18) or 2-way 4 k × 16 (18)

Ordering Information

Type No.	Access	Package
HM62A168CP-25	25 ns	52-pin PLCC (CP-52)
HM62A168CP-25R	25 ns	
HM62A168CP-35	35 ns	
HM62A188CP-25	25 ns	
HM62A188CP-25R	25 ns	
HM62A188CP-35	35 ns	
HM62A168BCP-25*1	25 ns	
HM62A168BCP-35*1	35 ns	
HM62A188BCP-25*1	25 ns	
HM62A188BCP-35*1	35 ns	

Note: 1. See note 6 in Write Timing Waveform(3).

Pin Arrangement



(Top View)

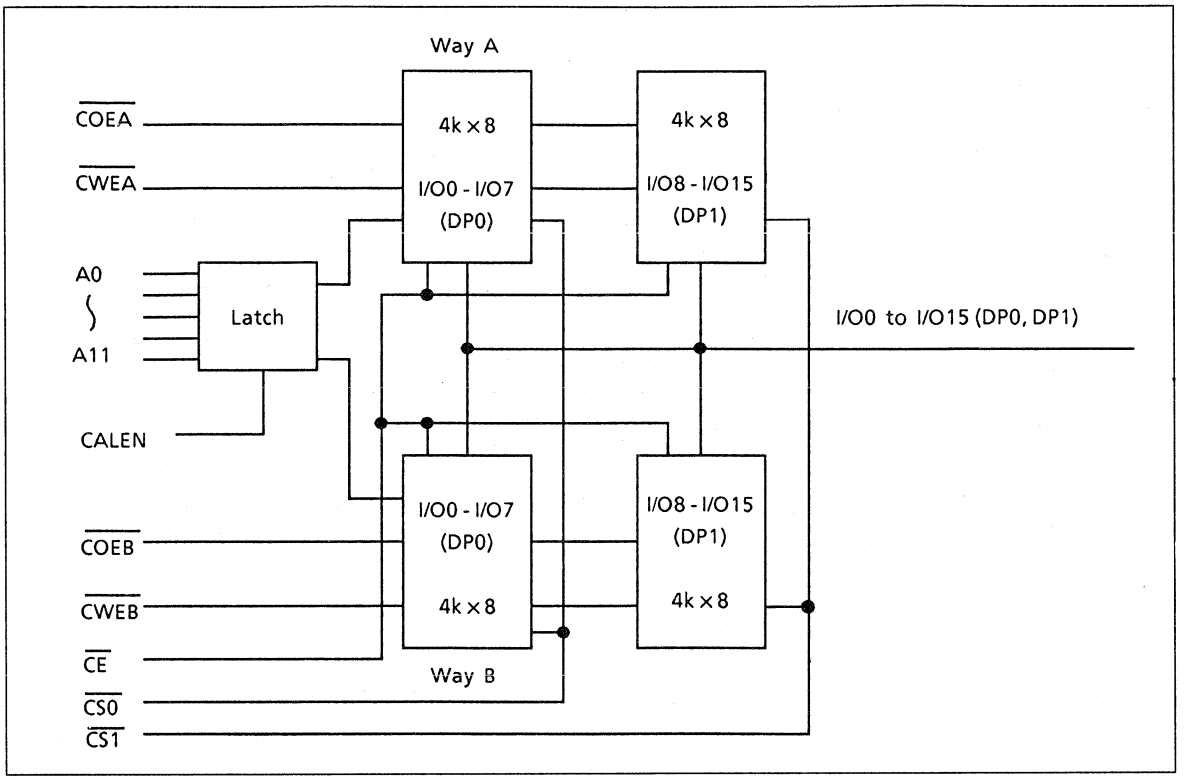
Pin Description

Pin name	Function
CALEN	Cache address latch enable
MODE	Mode select
A0 to A12	Address
$\overline{CS0}$, $\overline{CS1}$	Cache chip select
$\overline{COEA}$, $\overline{COEB}$	Cache output enable

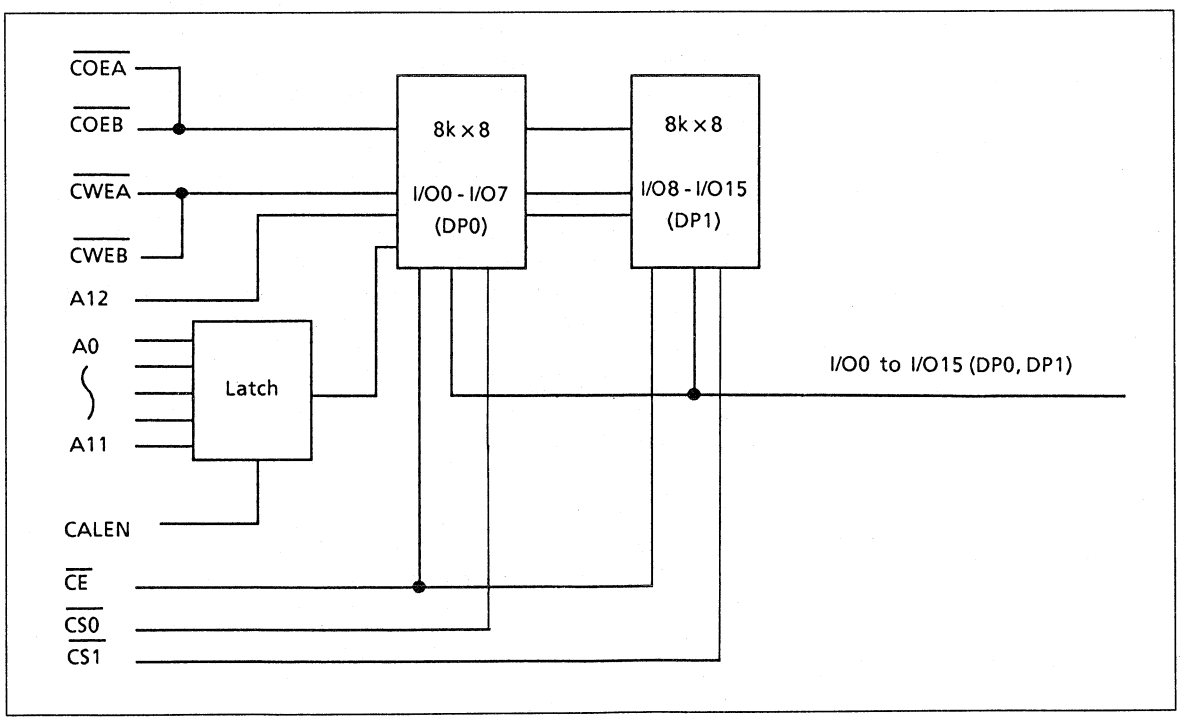
Pin name	Function
$\overline{CWEA}$, $\overline{CWEB}$	Cache write enable
I/O0 to I/O15	Data input/output
$\overline{CE}$	Cache chip enable
NC	No connection
DP0, DP1	Parity input/output

Block Diagram

Topology Two-Way Set Associative (MODE = logic high)



Topology Direct Mapped (MODE = logic low)



Signal Description

Signal name	Pin no.	Signal description
A0 – A6 A7 – A11	8 – 2 51 – 47	Address inputs to the memory array. A0 – A11 are latched on the falling edge of CALEN.
A12	46	A12 address input. In the two-way mode, address input A12 will be a "don't care" and should be externally wired to ground. In the direct-mapped mode, when MODE is connected to V_{SS}, A12 selects which of the two 4 k × 16 (18) banks is read from or written to. A12 is not latched by CALEN, as are the other address inputs.
CALEN	52	Cache Address Latch Enable input. This signal controls the internal address latches for inputs A0 - A11. When CALEN is high, the latch is transparent. The falling edge of CALEN latches the current address input levels. A12 is static and is not controlled by CALEN.
I/O0 - I/O15	11 – 14, 16 – 19 35 – 38, 40 – 43	Data inputs and outputs. These are the three-state lines that provide data access to the memory array.
MODE	31	MODE input. This signal controls whether the memory device is to be used in a direct-mapped configuration (8 k × 16 (18)) or as a two-way set-associative configuration (two 4 k × 16 (18)). When the MODE signal is high, the device is placed in the two-way mode. When the mode input is low, the cache is in the direct-mapped mode. This is a hardwired strap option and must not be changed dynamically.
$\overline{CS0}$, $\overline{CS1}$	23, 30	Cache Chip Select inputs. These active low signals selectively enable the two bytes of memory. $\overline{CS0}$ low enables bits I/O0 – I/O7 and DP0. $\overline{CS1}$ low enables bits I/O8 – I/O15 and DP1. This applies to both the direct-mapped and two-way modes.
$\overline{CE}$	45	Cache Chip Enable input (active low). This signal functions as a global chip enable. It gates the $\overline{COEA}$, $\overline{COEB}$, $\overline{CWEA}$, and $\overline{CWEB}$ inputs. A chip enable controlled write can be done by taking $\overline{CE}$ inactive high while one of the $\overline{CWEX}$ signals is active (assuming all other timings for a write cycle are met).
$\overline{COEA}$, $\overline{COEB}$	28, 29	Cache Output Enable inputs. These active low inputs enable cache bank A or bank B to drive the data bus when in the two-way mode. In the two-way mode, bank A is enabled when $\overline{COEA}$ is low and bank B is enabled when $\overline{COEB}$ is low. If both banks are activated at the same time, then both banks become deselected. In the direct-mapped mode, $\overline{COEA}$ and $\overline{COEB}$ must be tied together externally. A low on $\overline{COEA}$ and $\overline{COEB}$ then enables the outputs of the 8 k × 16 (18) memory. A12 is used to determine which 4 k × 16 (18) bank is accessed.
$\overline{CWEA}$, $\overline{CWEB}$	25, 24	Cache Write Enable inputs (active low). In the two-way mode when $\overline{CWEA}$ ($\overline{CWEB}$) is active, data is written into memory bank A (B). In the direct-mapped mode, $\overline{CWEA}$ and $\overline{CWEB}$ must be tied together externally. A low on $\overline{CWEA}$ and $\overline{CWEB}$ enables data to be written into the 8 k × 16 (18) memory. A12 is used to determine which 4 k × 16 (18) bank is accessed.

Signal Description (cont)

Signal name	Pin no.	Signal description
DP0 or NC, DP1 or NC	20, 34	Parity data inputs and outputs (HM62A188). These are three-state lines that provide parity data access to the memory array. For the HM62A168, these two pins are not used (NC) and must not be physically tied to V_{CC}, V_{SS}, or any other device inputs.
V_{CC}	1, 21, 22, 32, 33	System power +5 V (21, 22, 32, 33 are for outputs)
V_{SS}	9, 10, 15, 26, 27, 39, 44	System ground (10, 15, 39, 44 are for outputs)

Function Table

Two-Way Mode (Mode = High), 2-4 k × 16 (18)

Input signal							I/O pin		
$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$	I/O0 – I/O7 (DP0)	I/O8 – I/O15 (DP1)	Function
H	X	X	X	X	X	X	High-Z	High-Z	Disabled
X	H	H	X	X	X	X	High-Z	High-Z	Disabled
X	X	X	H	H	X	X	High-Z	High-Z	Output high-Z
X	X	X	L	L	X	X	High-Z	High-Z	Output high-Z
L	L	H	L	H	H	H	Output	High-Z	Read way A
L	L	H	H	L	H	H	Output	High-Z	Read way B
L	H	L	L	H	H	H	High-Z	Output	Read way A
L	H	L	H	L	H	H	High-Z	Output	Read way B
L	L	L	L	H	H	H	Output	Output	Read way A
L	L	L	H	L	H	H	Output	Output	Read way B
L	L	H	X	X	L	H	Input	High-Z	Write way A
L	L	H	X	X	H	L	Input	High-Z	Write way B
L	H	L	X	X	L	H	High-Z	Input	Write way A
L	H	L	X	X	H	L	High-Z	Input	Write way B
L	L	L	X	X	L	H	Input	Input	Write way A

Two-Way Mode (Mode = High), 2-4 k × 16 (18) (cont)

Input signal							I/O pin		
$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$	I/O0 – I/O7 (DP0)	I/O8 – I/O15 (DP1)	Function
L	L	L	X	X	H	L	Input	Input	Write way B
L	L	H	X	X	L	L	Input	High-Z	Write way A and B
L	H	L	X	X	L	L	High-Z	Input	Write way A and B
L	L	L	X	X	L	L	Input	Input	Write way A and B

Direct Mode (Mode = Low), 8 k × 16 (18)

Input signal							I/O pin		
$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$	I/O0 – I/O7 (DP0)	I/O8 – I/O15 (DP1)	Function
H	X	X	X	X	X	X	High-Z	High-Z	Disabled
X	H	H	X	X	X	X	High-Z	High-Z	Disabled
X	X	X	H	H	X	X	High-Z	High-Z	Output High-Z
L	L	H	L	L	H	H	Output	High-Z	Read
L	H	L	L	L	H	H	High-Z	Output	Read
L	L	L	L	L	H	H	Output	Output	Read
L	L	H	X	X	L	L	Input	High-Z	Write
L	H	L	X	X	L	L	High-Z	Input	Write
L	L	L	X	X	L	L	Input	Input	Write

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	Vin	–0.5*1 to +7.0	V
Power dissipation	P_T	1.4	W
Operation temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–10 to +85	°C

Note: 1. Vin min = –2.5 V for pulse width ≤ 10 ns

Recommended DC operating Conditions

(Ta = 0 to +70°C, exceeding minimum air flow requirement: see page 845)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5*1	5.0	5.5*1	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*2	—	0.8	V

Notes: 1. V_{CC} min = 4.75 V and V_{CC} max = 5.25 V for HM62A168/188-25/25R, HM62A168B/188B-25
2. V_{IL} min = –2.0 V for pulse width ≤ 10 ns

DC Characteristics

(Ta = 0 to +70°C, V_{CC} = 5 V ± 10%*1, V_{SS} = 0 V, exceeding minimum air flow requirement: see page 845)

Parameter	Symbol	Min	Typ*2	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	µA	V_{CC} = Max Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	10.0	µA	Output disable $V_{I/O}$ = V_{SS} to V_{CC}
Active operating power supply current	I_{CC}	—	—	220	mA	Vin = V_{SS}/V_{CC} $I_{I/O}$ = 0 mA 2 × Min. cycle, $\overline{CE}$, $\overline{CS}$ = V_{IL} max CALEN = V_{IH} min
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 4 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –1.0 mA

Notes: 1. V_{CC} = 5 V ± 5% for HM62A168/188-25/25R, HM62A168B/188B-25
2. Typical limits are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1 MHz)*1

Parameter	Symbol	Min	Max	Unit	Test conditions
Input capacitance	Cin	—	6	pF	Vin = 0 V
Input / Output capacitance	$C_{I/O}$	—	12	pF	$V_{I/O}$ = 0 V

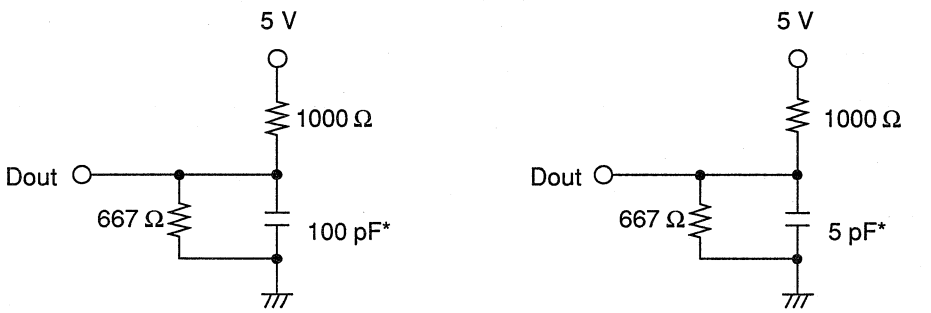
Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%*1, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures
- Exceeding minimum air flow requirement: See page 845

Note: 1. V_{CC} = 5 V ± 5% for HM62A168/188-25/25R, HM62A168B/188B-25



Output Load A

Output Load B

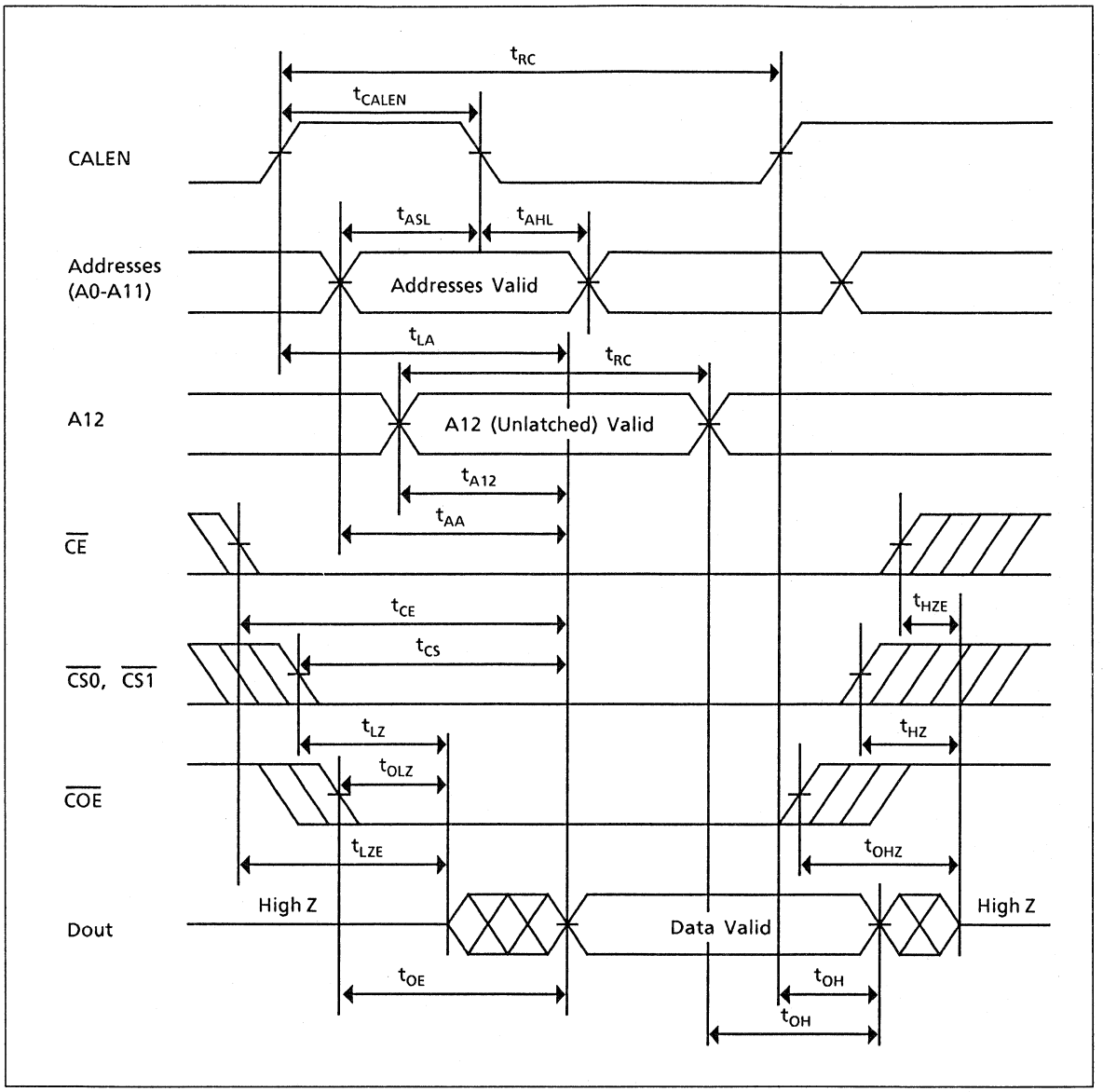
(for t_{LZ}, t_{LZE}, t_{OLZ}, t_{HZ}, t_{HZE}, t_{OHZ}, t_{WHZ}, t_{WLZ})

* Including scope and jig

Read Cycle

		HM62A168/B-25 HM62A188/B-25		HM62A168-25R HM62A188-25R		HM62A168/B-35 HM62A188/B-35			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	25	—	25	—	35	—	ns	
Address access time	t_{AA}	—	25	—	25	—	35	ns	
A12 address access time	t_{A12}	—	17	—	17	—	25	ns	
Chip select access time	t_{CS}	—	20	—	20	—	25	ns	
Chip enable access time	t_{CE}	—	20	—	22	—	25	ns	
CALEN high to output valid	t_{LA}	—	25	—	25	—	35	ns	1
Output enable to output valid	t_{OE}	—	10	—	10	—	13	ns	
Output hold from address change	t_{OH}	3	—	3	—	3	—	ns	2
Chip select to output Low-Z	t_{LZ}	3	—	3	—	3	—	ns	3
Chip enable low to output Low-Z	t_{LZE}	5	—	5	—	5	—	ns	3
Output enable to output Low-Z	t_{OLZ}	2	—	2	—	2	—	ns	3
Chip deselect to output High-Z	t_{HZ}	—	15	—	15	—	25	ns	3
Chip enable high to output High-Z	t_{HZE}	—	15	—	15	—	25	ns	3
Output disable to output High-Z	t_{OHZ}	—	10	—	10	—	14	ns	3
Address latch enable pulse width	t_{CALEN}	8	—	8	—	10	—	ns	
Address setup to latch low	t_{ASL}	4	—	4	—	6	—	ns	
Address hold to latch low	t_{AHL}	5	—	5	—	5	—	ns	

Read Timing Waveform (1) ($\overline{CWE}$ = high)

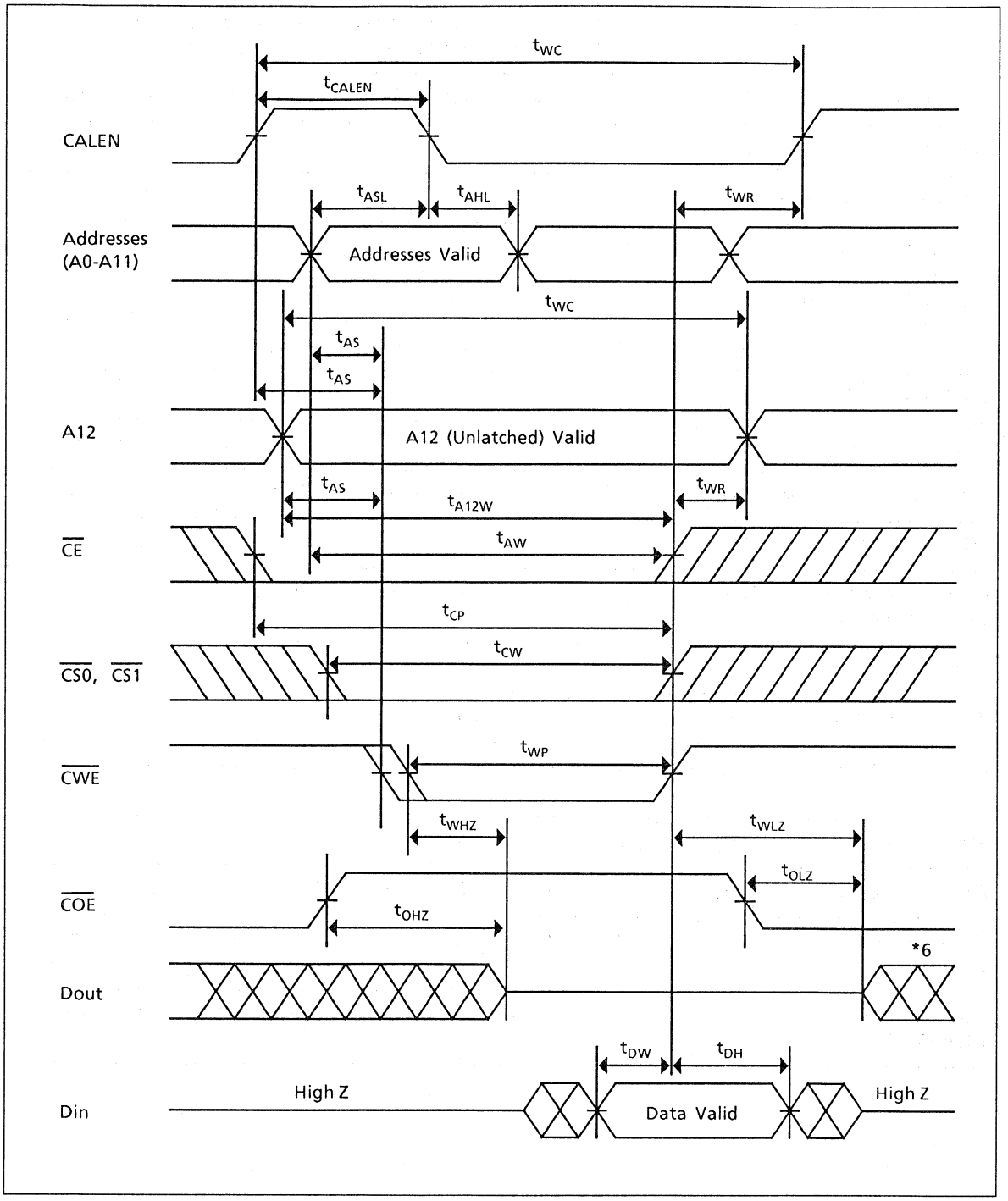


Notes: 1. t_{LA} is applied to the case that address is valid before CALEN goes high.
2. t_{OH} is determined by the earliest of CALEN going high, valid addresses A0 – A11 transition with CALEN high, or A12 transition.
3. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

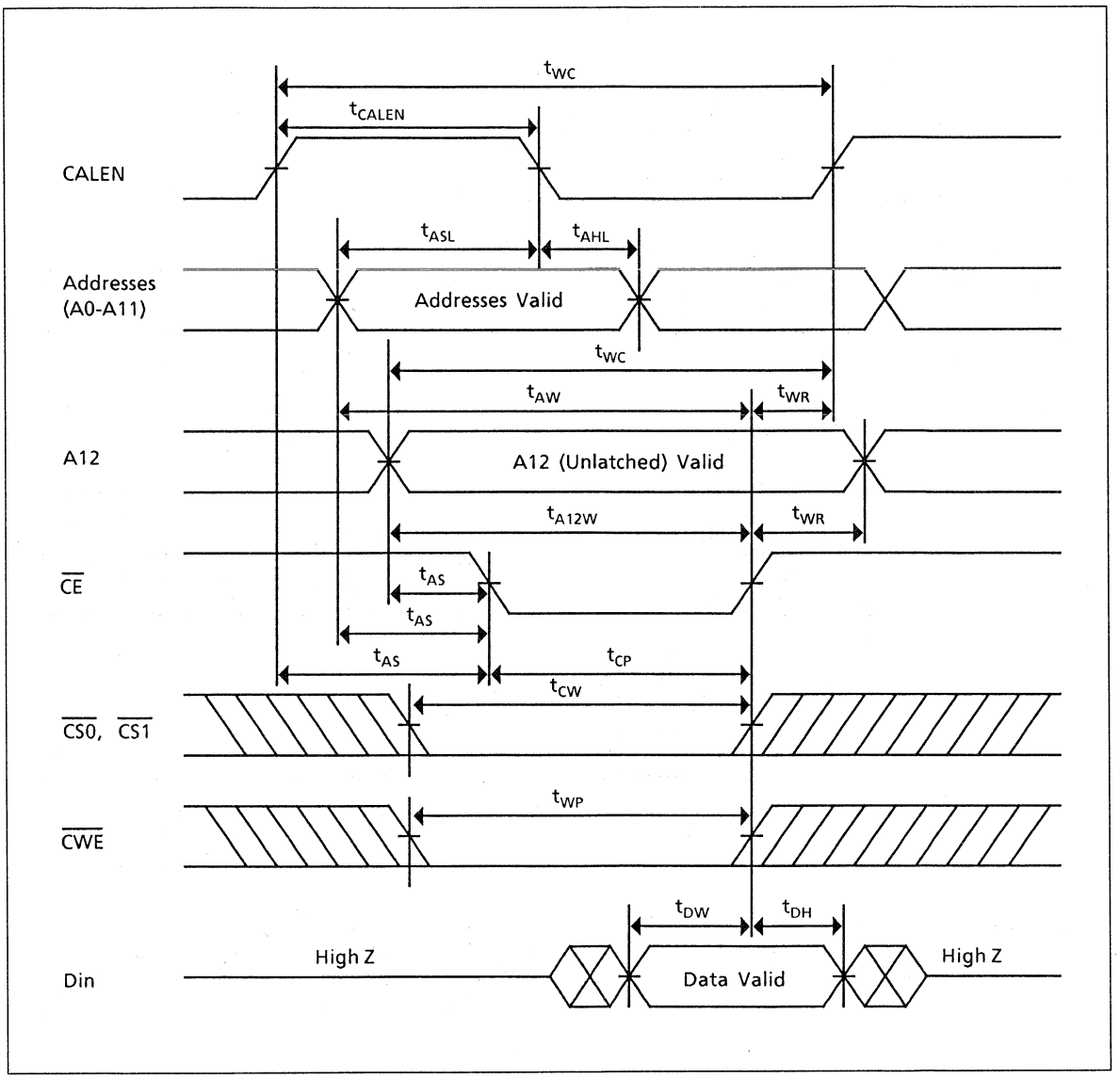
Write Cycle

		HM62A168/B-25 HM62A188/B-25		HM62A168-25R HM62A188-25R		HM62A168/B-35 HM62A188/B-35			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Write cycle time	t_{WC}	25	—	25	—	35	—	ns	
Address valid to end of write	t_{AW}	18	—	18	—	25	—	ns	1
A12 valid to end of write	t_{A12W}	18	—	18	—	25	—	ns	
Chip select to end of write	t_{CW}	18	—	18	—	25	—	ns	
Data valid to end of write	t_{DW}	10	—	10	—	10	—	ns	
Data hold from end of write	t_{DH}	0	—	0	—	0	—	ns	
Write enable active to High-Z	t_{WHZ}	—	15	—	15	—	15	ns	5
Write enable inactive to Low-Z	t_{WLZ}	3	—	3	—	3	—	ns	5
Write pulse width	t_{WP}	15	—	15	—	25	—	ns	
$\overline{CE}$ pulse width during chip enable controlled write	t_{CP}	15	—	15	—	25	—	ns	
Address setup time	t_{AS}	0	—	0	—	0	—	ns	2
Write recovery time	t_{WR}	0	—	0	—	0	—	ns	3
Address latch enable pulse width	t_{CALEN}	8	—	8	—	10	—	ns	
Address setup to latch low	t_{ASL}	4	—	4	—	6	—	ns	
Address hold to latch low	t_{AHL}	5	—	5	—	5	—	ns	
Chip enable low to output Low-Z	t_{OLZ}	2	—	2	—	2	—	ns	5
Output disable to output High-Z	t_{OHZ}	—	10	—	10	—	14	ns	5

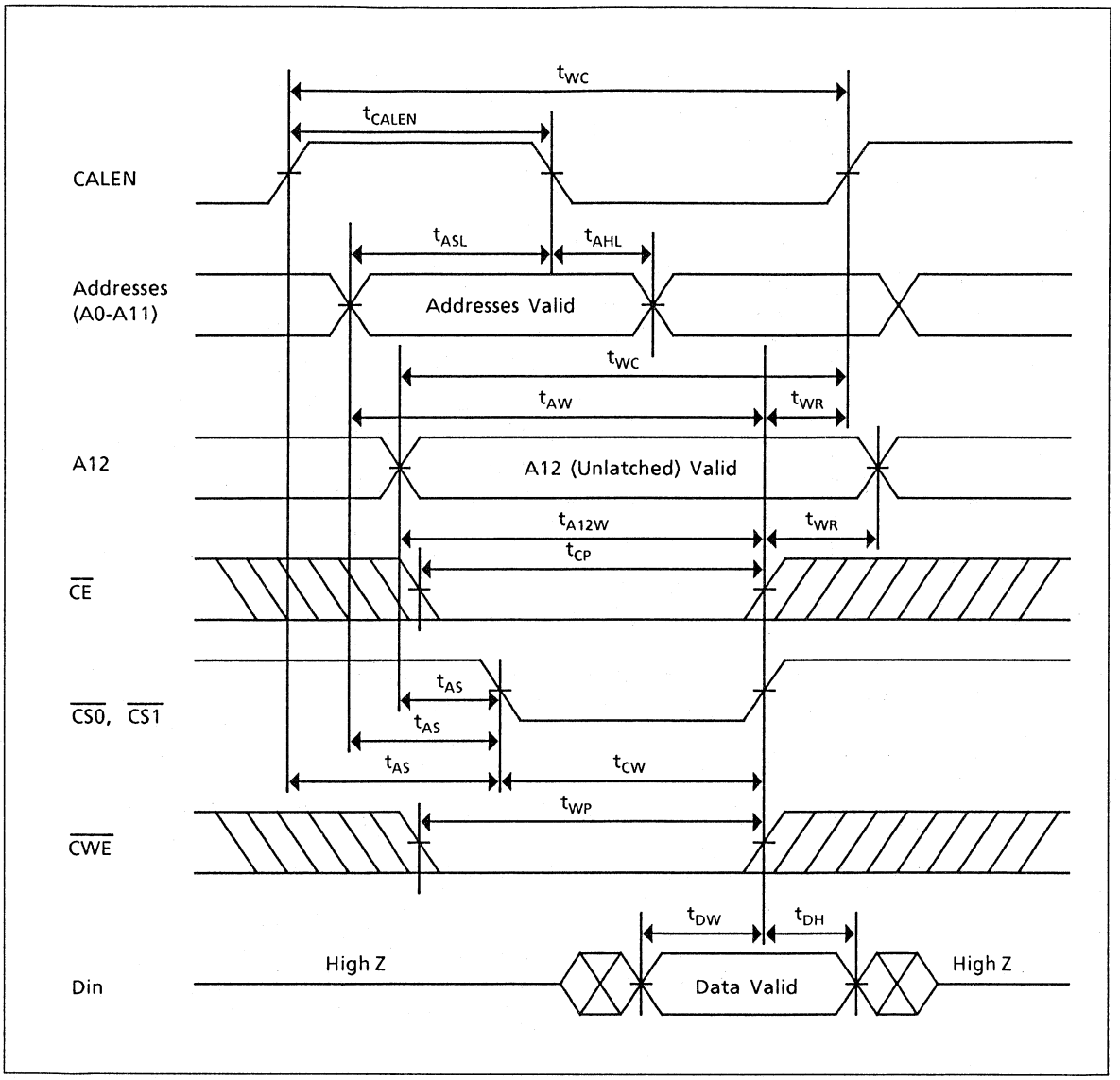
Write Timing Waveform (1) ($\overline{WE}$ controlled)



Write Timing Waveform (2) ($\overline{COE}$ = high, $\overline{CE}$ controlled)

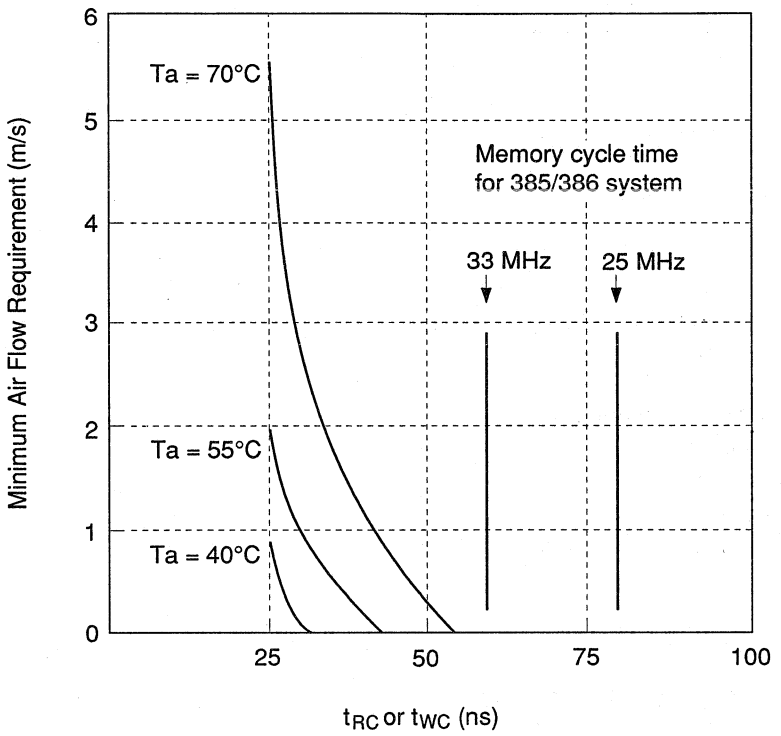


Write Timing Waveform (3) ($\overline{COE}$ = high, $\overline{CS}$ controlled)



Notes:
1. t_{AW} is measured from the later of CALEN going high, or addresses A0 – A11 transition with CALEN high to the end of write cycle.
2. t_{AS} is measured from the latest of CALEN going high, addresses A0 – A11 transition with CALEN high, or address A12 transition to the beginning of write cycle.
3. t_{WR} is measured from the earliest of $\overline{CS0}$, $\overline{CS1}$, $\overline{CE}$, or $\overline{WE}$ going high to the earlier of CALEN going high, or address A12 transition.
4. A write occurs during the overlap of a low $\overline{CS0}$ or $\overline{CS1}$, a low $\overline{CE}$, and a low $\overline{WE}$.
5. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
6. Dout is not the same phase of write data of this write cycle. Normal read cycle shall be used for write verify. This note doesn't applies to HM62A168B/188B.

Air Flow Requirements



HM62B168, HM62B188 Series

Direct Mapped 8,192-Word × 16 (18)-Bit / 2-Way 4,096-Word × 16(18)-Bit Static Cache Memory

The Hitachi HM62B168/188 is a high speed 128(144)-k Cache memory organized as 2-way set associative 4k × 16(18) or direct mapped 8k × 16(18).
By using two HM62B168/188, high performance 32-bit microprocessor system can be achieved.
The HM62B168/188, packaged in a 52-pin PLCC is available for high density mounting.

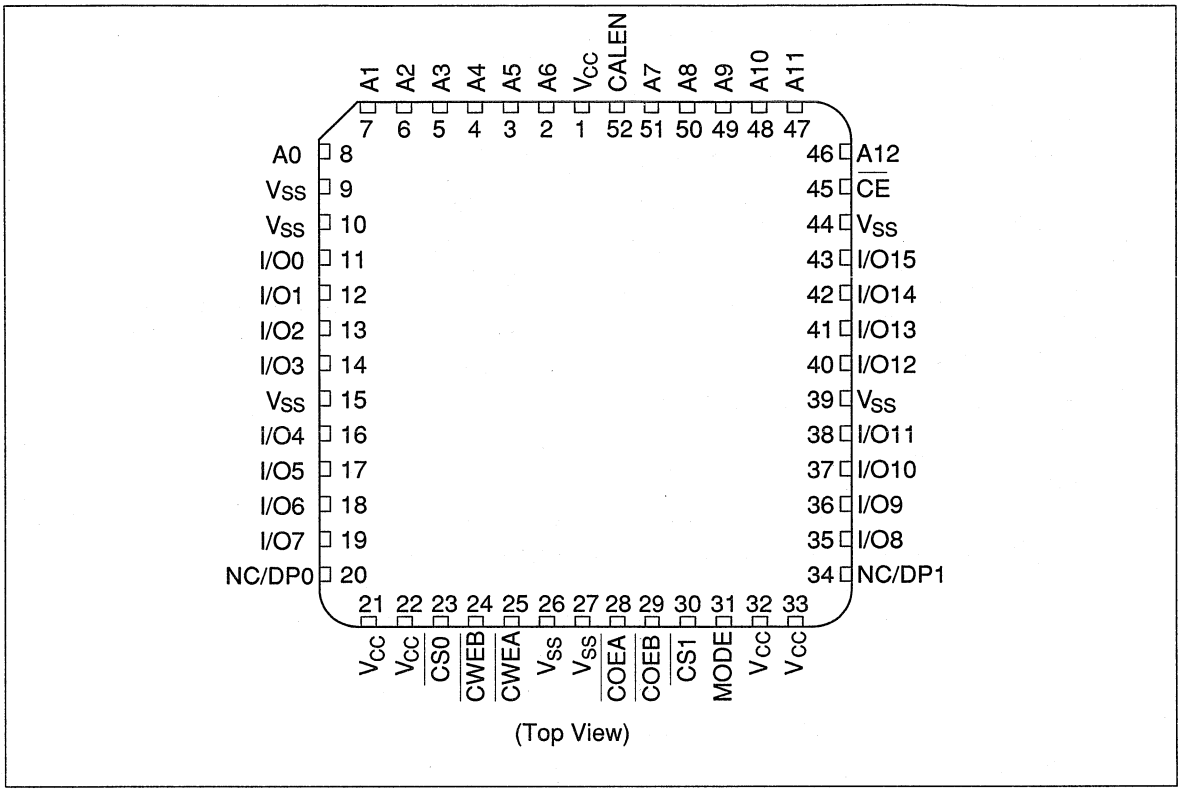
Features

- Single 5 V supply and high density 52-pin PLCC package.
- High speed
  - Access time 25/35 ns (maximum)
- Directly TTL compatible
  - All inputs and outputs
- Address and $\overline{CE}$ latch
- Pin programmable for 8k × 16(18) or 2-way 4k × 16(18)

Ordering Information

Type No.	Access time	Package
HM62B168CP-25	25 ns	52-pin PLCC (CP-52)
HM62B168CP-35	35 ns	
HM62B188CP-25	25 ns	
HM62B188CP-35	35 ns	

Pin Arrangement



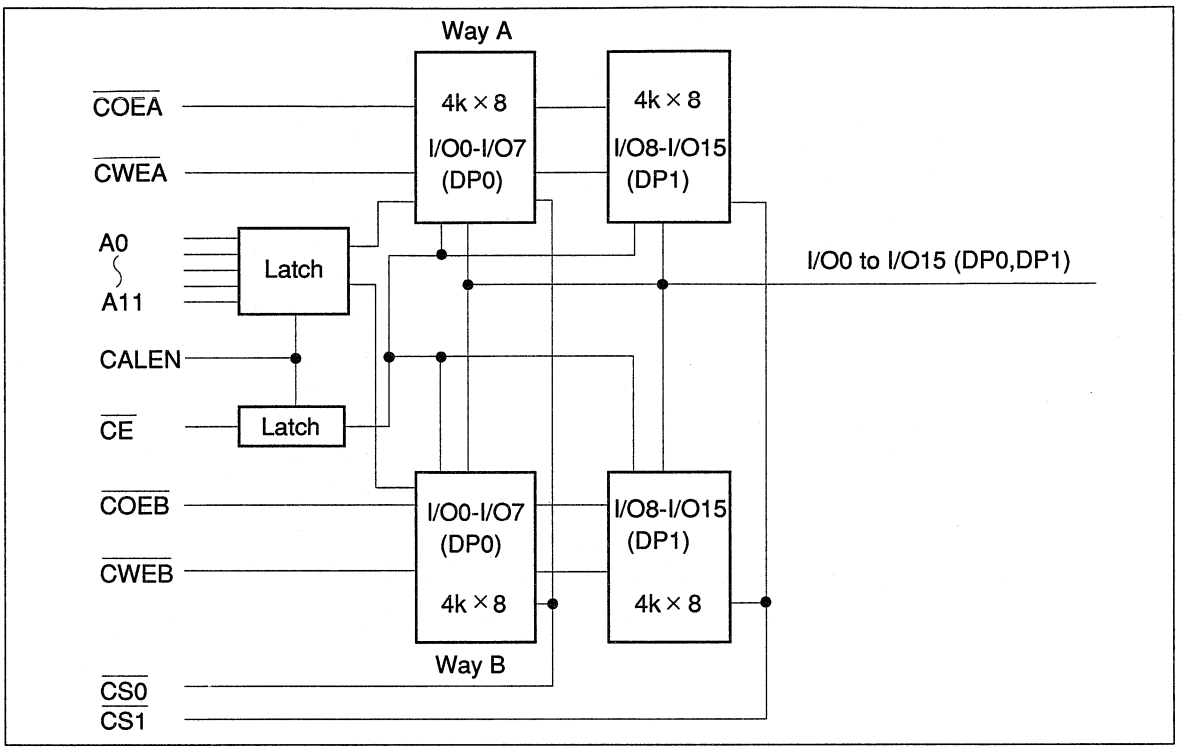
(Top View)

Pin Description

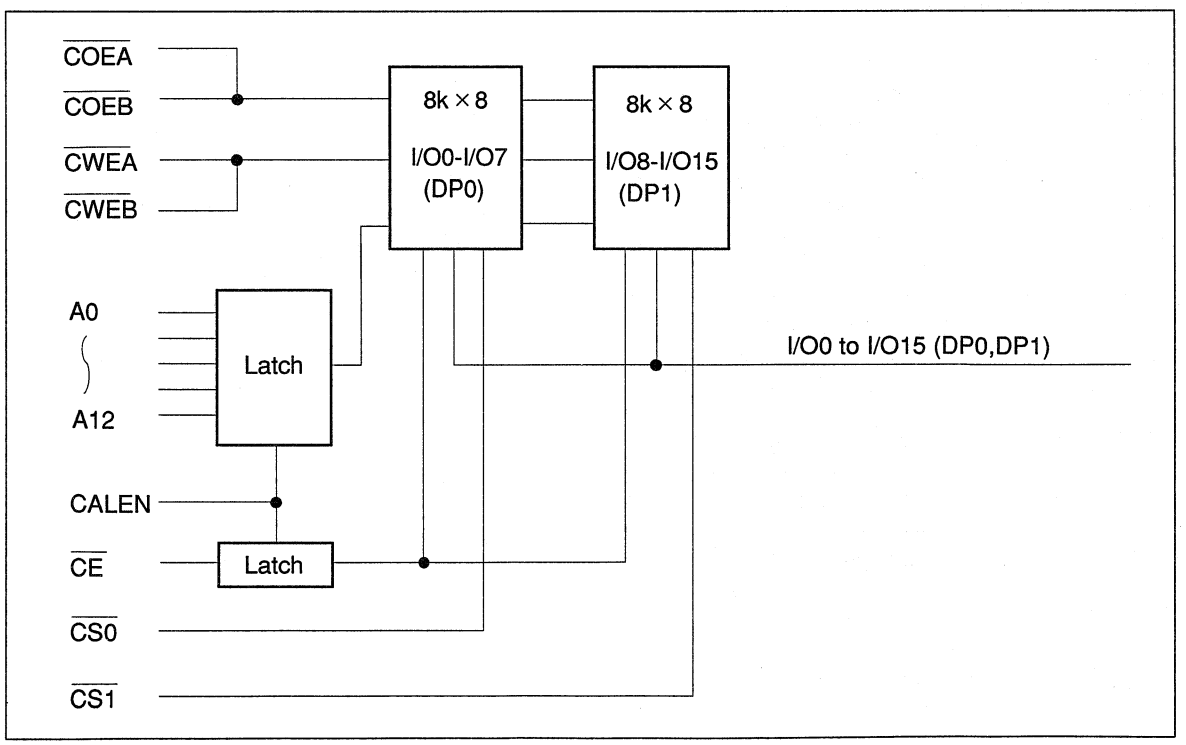
Pin name	Function
CALEN	Cache address latch and $\overline{CE}$ latch enable
MODE	Mode select
A0 to A12	Address
$\overline{CS0}$, $\overline{CS1}$	Cache chip select
$\overline{COEA}$, $\overline{COEB}$	Cache output enable
$\overline{CWEA}$, $\overline{CWEB}$	Cache write enable
I/O0 to I/O15	Data input/output
$\overline{CE}$	Cache chip enable
NC	No connection
DP0, DP1	Parity input/output

Block Diagram

- **Topology Two-Way Set Associative** (MODE = logic high)



- **Topology Direct Mapped** (MODE = logic low)



Signal Description

Signal Name	Pin Number	Signal Description
A0-A6 A7-11 A12	8-2 51-47 46	Address inputs to the memory array. A0-A12 are latched on the falling edge of CALEN. In the two-way mode, address input A12 will be a "don't care" and should be externally wired to ground.
CALEN	52	Cache Address Latch and $\overline{CE}$ Latch Enable input. This signal controls the internal address and $\overline{CE}$ latches for inputs A0-A12 and $\overline{CE}$. When CALEN is high, the latch is transparent. The falling edge of CALEN latches the current address input levels.
I/O0-1/O15	11-14, 16-19, 35-38, 40-43	Data inputs and outputs. These are the three-state lines that provide data access to the memory array.
MODE	31	MODE input. This signal controls whether the memory device is to be used in a direct-mapped configuration (8k × 16 (18)) or as a two-way set-associative configuration(two 4k × 16(18)). When the MODE signal is high, the device is placed in the two-way mode. When the mode input is low, the cache is in the direct-mapped mode. This is a hardwired strap option and must not be changed dynamically.
$\overline{CS0}$, $\overline{CS1}$	23,30	Cache Chip Select inputs. These active low signals selectively enable the two bytes of memory. $\overline{CS0}$ low enables bits I/O0-1/O7 and DP0. $\overline{CS1}$ low enables bits I/O8-I/O15 and DP1. This applies to both the direct-mapped and two-way modes.
$\overline{CE}$	45	Cache Chip Enable input (active low). $\overline{CE}$ is latched on the falling edge of CALEN. This signal functions as a global chip enable. It gates the $\overline{COEA}$, $\overline{COEB}$, $\overline{CWEA}$, and $\overline{CWEB}$ inputs. A chip enable controlled write can be done by taking $\overline{CE}$ inactive high while one of the $\overline{CWEX}$ signals is active (assuming all other timings for a write cycle are met).
$\overline{COEA}$, $\overline{COEB}$	28, 29	Cache Output Enable inputs. These active low input enable cache bank A or bank B to drive the data bus when in the two-way mode. In the two-way mode, bank A is enabled when $\overline{COEA}$ is low and bank B is enabled when $\overline{COEB}$ is low. If both banks are activated at the same time, then both banks become deselected. In the direct-mapped mode, $\overline{COEA}$ and $\overline{COEB}$ must be tied together externally. A low on $\overline{COEA}$ and $\overline{COEB}$ then enables the outputs of the 8k × 16(18) memory.
$\overline{CWEA}$, $\overline{CWEB}$	25, 24	Cache Write Enable inputs (active low). In the two-way mode when $\overline{CWEA}$ ($\overline{CWEB}$) is active, data is written into memory bank A (B). In the direct-mapped mode, $\overline{CWEA}$ and $\overline{CWEB}$ must be tied together externally. A low on $\overline{CWEA}$ and $\overline{CWEB}$ enables data to be written into the 8k × 16 (18) memory.
DP0 or NC DP1 or NC	20 34	Parity data inputs and outputs (HM62B188). These are three-state lines that provide parity data access to the memory array. For the HM62B168, these two pins are not used (NC) and must not be physically tied to V_{CC}, V_{SS}, or any other device inputs.

Signal Description (cont)

Signal Name	Pin Number	Signal Description	
V_{CC}	1, 21, 22, 32, 33	System Power +5 V.	(21, 22, 32, 33 are for outputs)
V_{SS}	9, 10, 15, 26, 27 39, 44	System Ground.	(10, 15, 39, 44 are for outputs)

Function Table

Two-Way Mode (Mode = High)
2-4k × 16(18)

Input Signal							I/O Pin		
$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$	I/O0-I/O7(DP0)	I/O8-I/O15(DP1)	Function
H	X	X	X	X	X	X	High-z	High-z	Disabled
X	H	H	X	X	X	X	High-z	High-z	Disabled
X	X	X	H	H	X	X	High-z	High-z	Output high-Z
X	X	X	L	L	X	X	High-z	High-z	Output high-Z
L	L	H	L	H	H	H	Output	High-z	Read way A
L	L	H	H	L	H	H	Output	High-z	Read way B
L	H	L	L	H	H	H	High-z	Output	Read way A
L	H	L	H	L	H	H	High-z	Output	Read way B
L	L	L	L	H	H	H	Output	Output	Read way A
L	L	L	H	L	H	H	Output	Output	Read way B
L	L	H	X	X	L	H	Input	High-z	Write way A
L	L	H	X	X	H	L	Input	High-z	Write way B
L	H	L	X	X	L	H	High-z	Input	Write way A
L	H	L	X	X	H	L	High-z	Input	Write way B
L	L	L	X	X	L	H	Input	Input	Write way A
L	L	L	X	X	H	L	Input	Input	Write way B
L	L	H	X	X	L	L	Input	High-z	Write way A & B
L	H	L	X	X	L	L	High-z	Input	Write way A & B
L	L	L	X	X	L	L	Input	Input	Write way A & B

Direct Mode (Mode = Low)
8k × 16(18)

Input Signal							I/O Pin		
$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$	I/O0-I/O7(DP0)	I/O8-I/O15(DP1)	Function
H	X	X	X	X	X	X	High-z	High-z	Disabled
X	H	H	X	X	X	X	High-z	High-z	Disabled
X	X	X	H	H	X	X	High-z	High-z	Output high-z
L	L	H	L	L	H	H	Output	High-z	Read
L	H	L	L	L	H	H	High-z	Output	Read
L	L	L	L	L	H	H	Output	Output	Read
L	L	H	X	X	L	L	Input	High-z	Write
L	H	L	X	X	L	L	High-z	Input	Write
L	L	L	X	X	L	L	Input	Input	Write

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	Vin	–0.5*[1] to +7.0	V
Power dissipation	P_T	1.4	W
Operation temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–10 to +85	°C

Note: 1. Vin min = –2.5 V for pulse width ≤10 ns.

Recommended DC Operating Conditions (Ta = 0 to + 70°C, exceeding minimum air flow requirement: see page 861.)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5*1	5.0	5.5*1	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*2	—	0.8	V

Notes: 1. V_{CC} min = 4.75 V and V_{CC} max = 5.25 V for HM62B168/188-25
2. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to + 70°C, V_{CC} = 5 V ± 10%*1, V_{SS} = 0 V, exceeding minimum air flow requirement: see page 861.)

Parameter	Symbol	Min	Typ*2	Max	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	µA	V_{CC} = Max. Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	10.0	µA	Output disable $V_{I/O}$ = V_{SS} to V_{CC}
Active operating power supply current	I_{CC}	—	—	220	mA	Vin = V_{SS}/V_{CC}, $I_{I/O}$ = 0 mA 2X Min. cycle, $\overline{CE}$, $\overline{CS}$ = V_{IL} max, CALEN = V_{IH} min
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 4 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –1.0 mA

Notes: 1. V_{CC} = 5 V ± 5 % for HM62B168/188 - 25
2. Typical limits are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1 MHz) *1

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	Cin	—	6	pF	Vin = 0V
Input/output capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

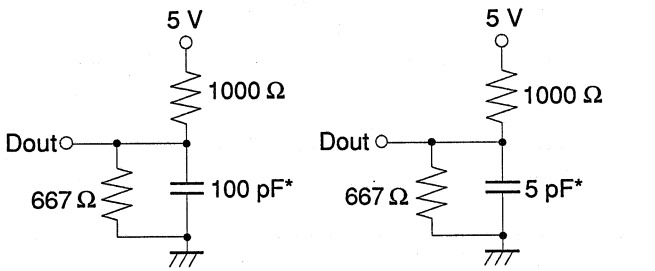
Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to + 70°C, V_{CC} = 5 V ± 10%*1, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures.
- Exceeding minimum air flow requirement: See page 861.

Note: 1 V_{CC} = 5 V ± 5% for HM62B168/188-25



Output Load (A)

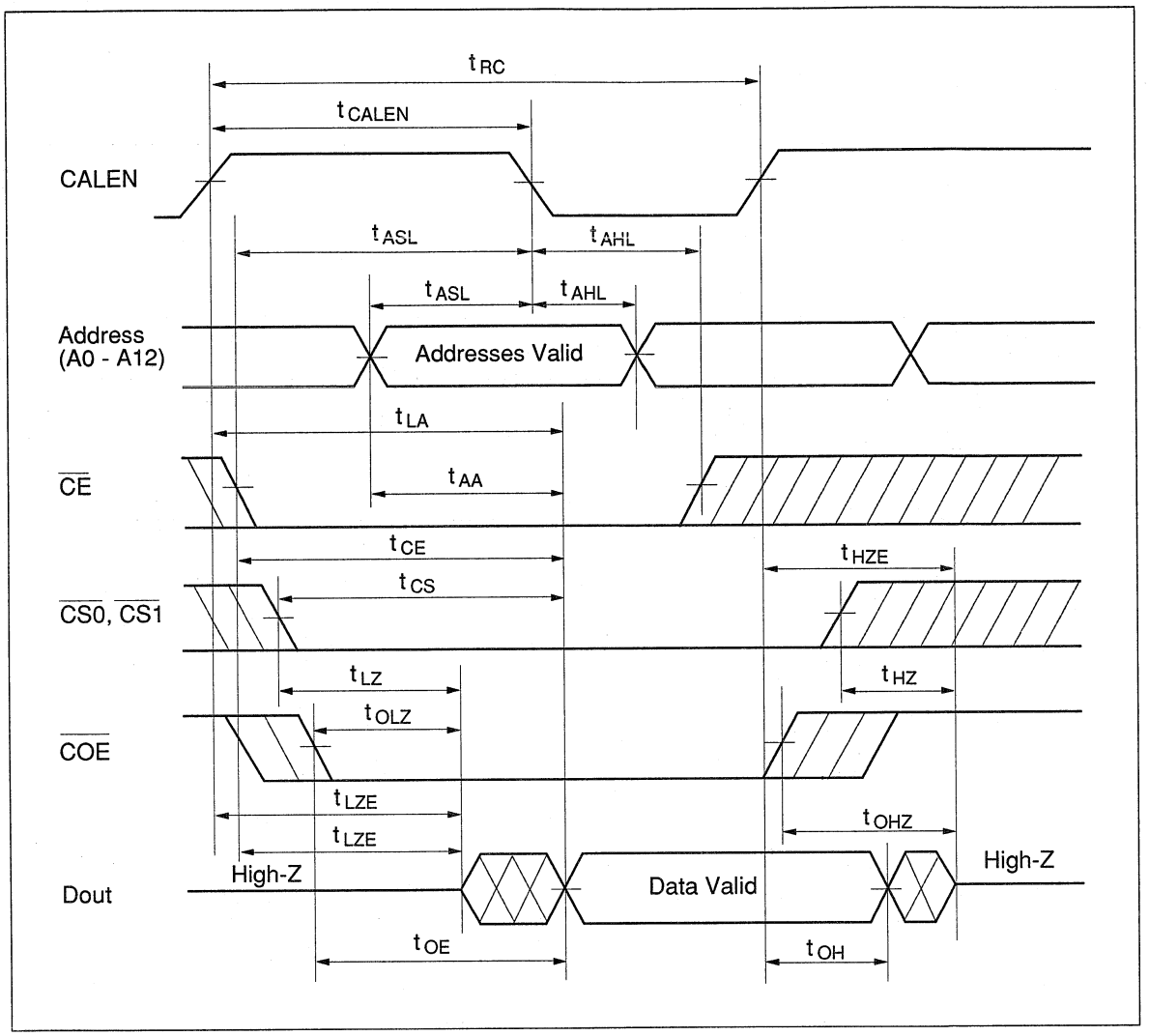
Output Load (B)
(for t_{LZ}, t_{LZE}, t_{OLZ}, t_{HZ}, t_{HZE}, t_{OHZ}, t_{WHZ}, t_{WLZ})

* Including scope and jig.

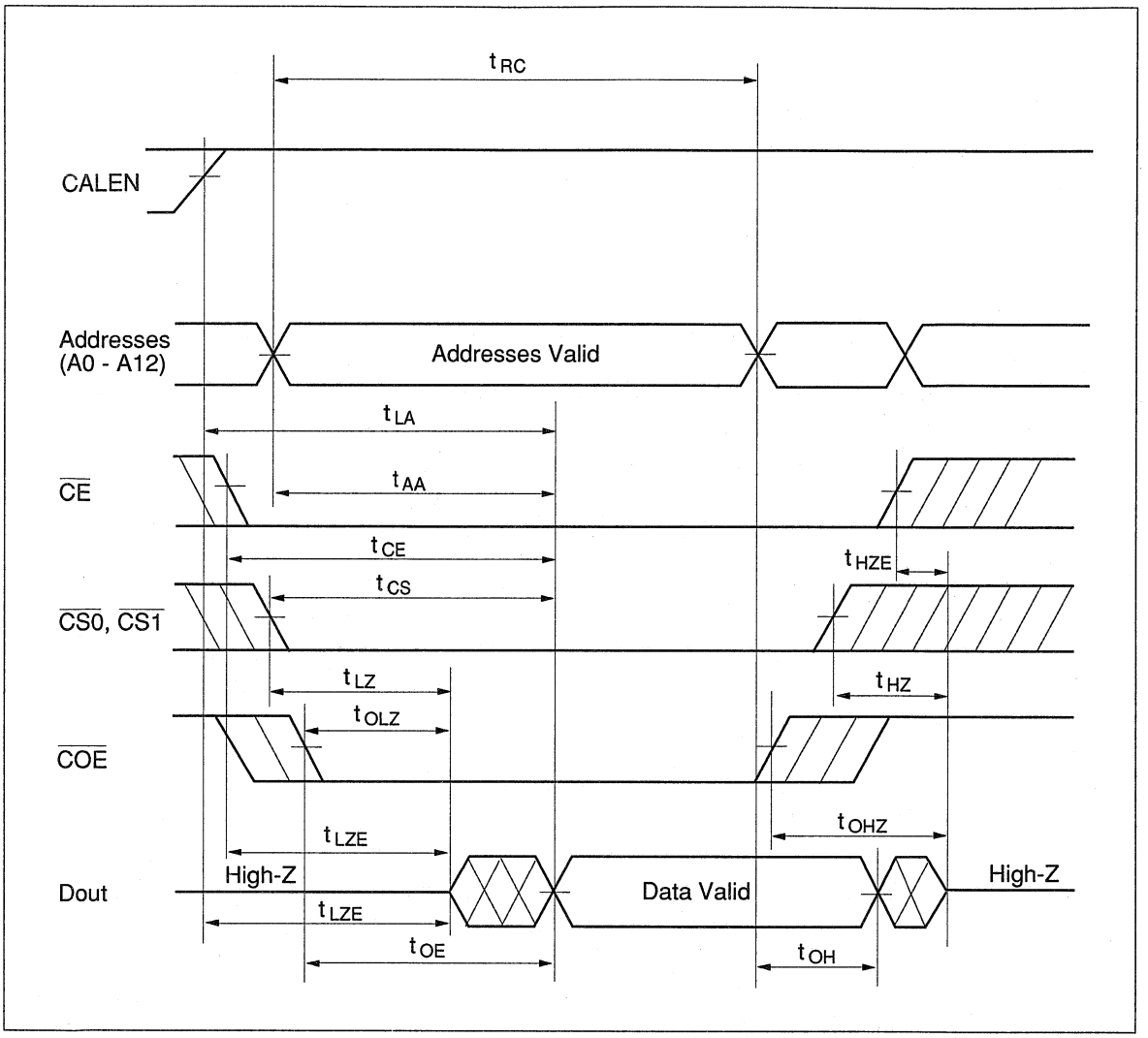
Read Cycle

Parameter	Symbol	HM62B168-25 HM62B188-25 Min	HM62B168-25 HM62B188-25 Max	HM62B168-35 HM62B188-35 Min	HM62B168-35 HM62B188-35 Max	Unit	Notes
Read cycle time	t_{RC}	25	—	35	—	ns	
Address access time	t_{AA}	—	25	—	35	ns	
Chip select access time	t_{CS}	—	20	—	25	ns	
Chip enable access time	t_{CE}	—	22	—	25	ns	
CALEN high to output valid	t_{LA}	—	25	—	35	ns	1
Output enable to output valid	t_{OE}	—	10	—	13	ns	
Output hold from address change	t_{OH}	5	—	5	—	ns	2
Chip select to output Low-Z	t_{LZ}	5	—	5	—	ns	3
Chip enable low to output Low-Z	t_{LZE}	5	—	5	—	ns	3,5
Output enable to output Low-Z	t_{OLZ}	2	—	2	—	ns	3
Chip deselect to output High-Z	t_{HZ}	—	12	—	25	ns	3
Chip enable high to output High-Z	t_{HZE}	—	15	—	25	ns	3,6
Output disable to output High-Z	t_{OHZ}	—	10	—	14	ns	3
Address latch enable pulse width	t_{CALEN}	8	—	10	—	ns	
Address and chip enable setup latch low	t_{ASL}	4	—	6	—	ns	
Address and chip enable hold to latch low	t_{AHL}	5	—	5	—	ns	

Read Timing Waveform (1) ($\overline{CWE}$ = high, CALEN = Clock)



Read Timing Waveform (2) ($\overline{CWE}$ = high, CALEN = high)

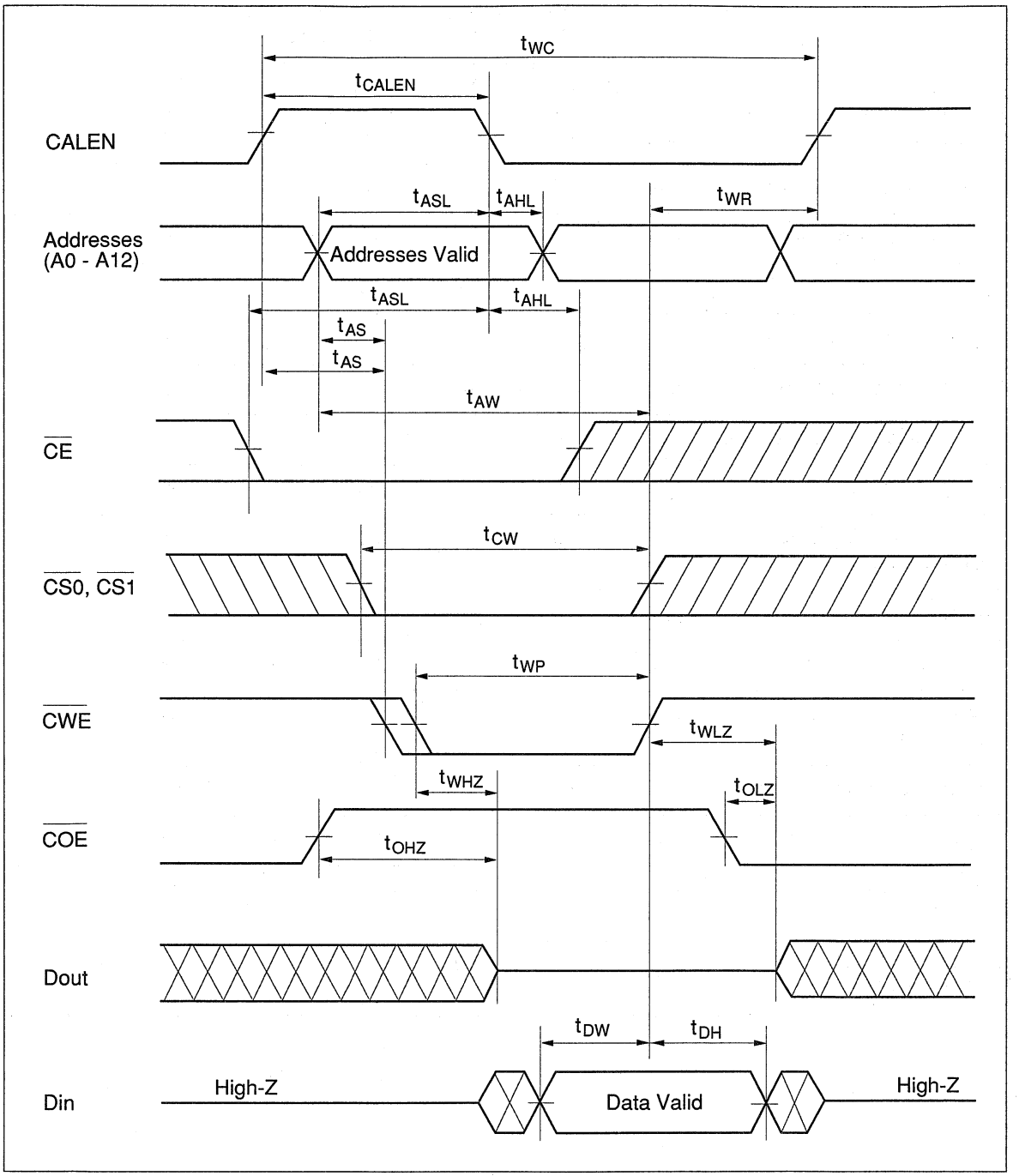


Notes:
1. t_{LA} is applied to the case that address is valid before CALEN goes high.
2. t_{OH} is determined by the earliest of CALEN going high, valid addresses A0-A12 transition with CALEN high.
3. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
4. When MODE input is high, address input A12 will be a "don't care".
5. t_{LZE} is determined by $\overline{CE}$ going low with CALEN high or CALEN going high with $\overline{CE}$ low.
6. t_{HZE} is determined by $\overline{CE}$ going high with CALEN high or CALEN going high with $\overline{CE}$ high.

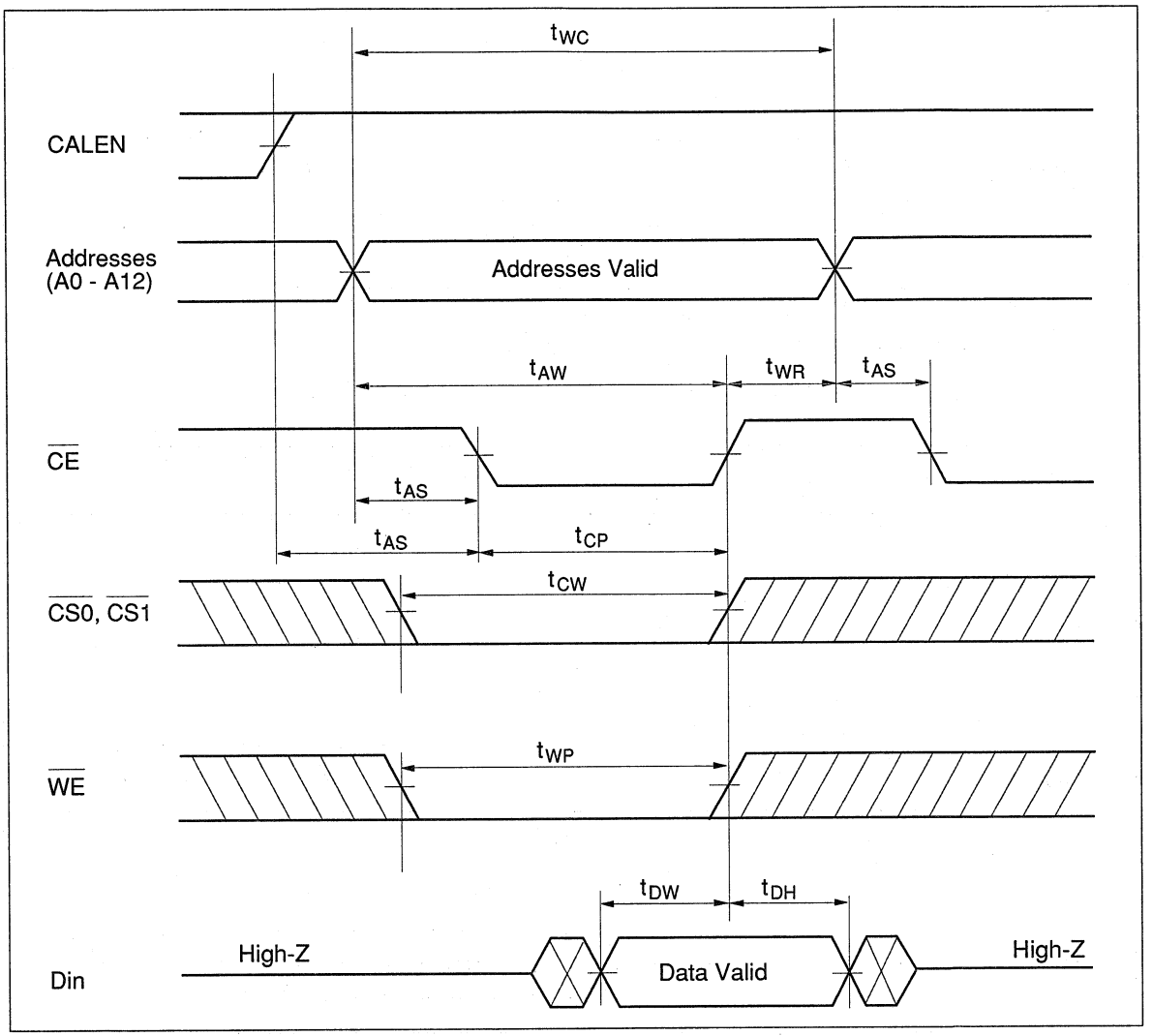
Write Cycle

Parameter	Symbol	HM62B168-25 HM62B188-25 Min	HM62B168-25 HM62B188-25 Max	HM62B168-35 HM62B188-35 Min	HM62B168-35 HM62B188-35 Max	Unit	Note
Write cycle time	t_{WC}	25	—	35	—	ns	
Address valid to end of write	t_{AW}	15	—	25	—	ns	1
Chip select to end of write	t_{CW}	15	—	25	—	ns	
Data valid to end of write	t_{DW}	10	—	10	—	ns	
Data hold from end of write	t_{DH}	0	—	0	—	ns	
Write enable active to High-Z	t_{WHZ}	—	12	—	15	ns	5
Write enable inactive to Low-Z	t_{WLZ}	3	—	3	—	ns	5
Write pulse width	t_{WP}	15	—	25	—	ns	
$\overline{CE}$ pulse width during chip enable controlled write	t_{CP}	15	—	25	—	ns	
Address setup time	t_{AS}	0	—	0	—	ns	2
Write recovery time	t_{WR}	0	—	0	—	ns	3
Address latch enable pulse width	t_{CALEN}	8	—	10	—	ns	
Address setup to latch low	t_{ASL}	4	—	6	—	ns	
Address hold to latch low	t_{AHL}	5	—	5	—	ns	
Output enable low to output Low-Z	t_{OLZ}	2	—	2	—	ns	5
Output disable to output High-Z	t_{OHZ}	—	10	—	14	ns	5

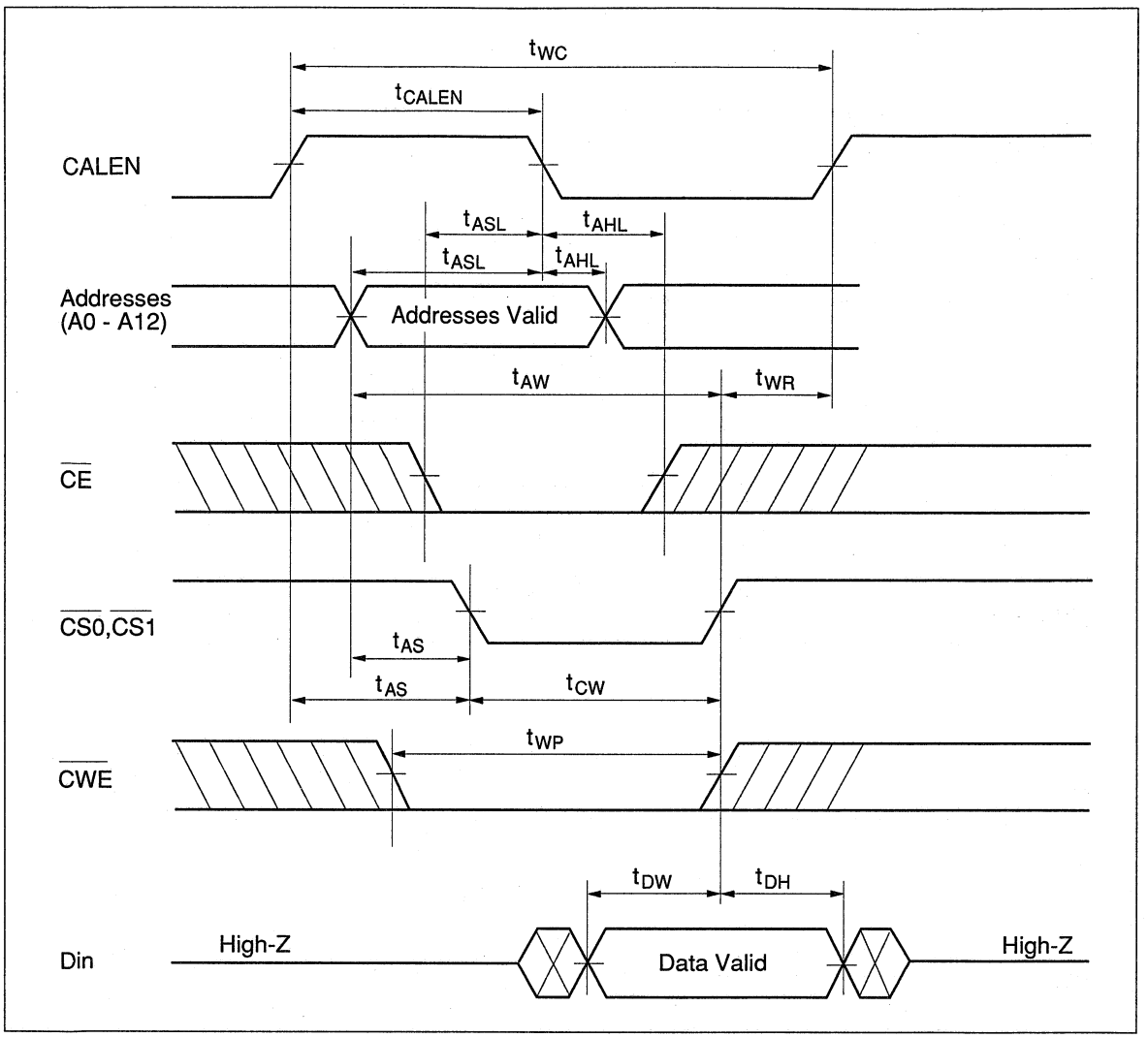
Write Timing Waveform (1) ($\overline{WE}$ controlled)



Write Timing Waveform (2) ($\overline{COE}$ = high, $\overline{CE}$ controlled, CALEN = high)

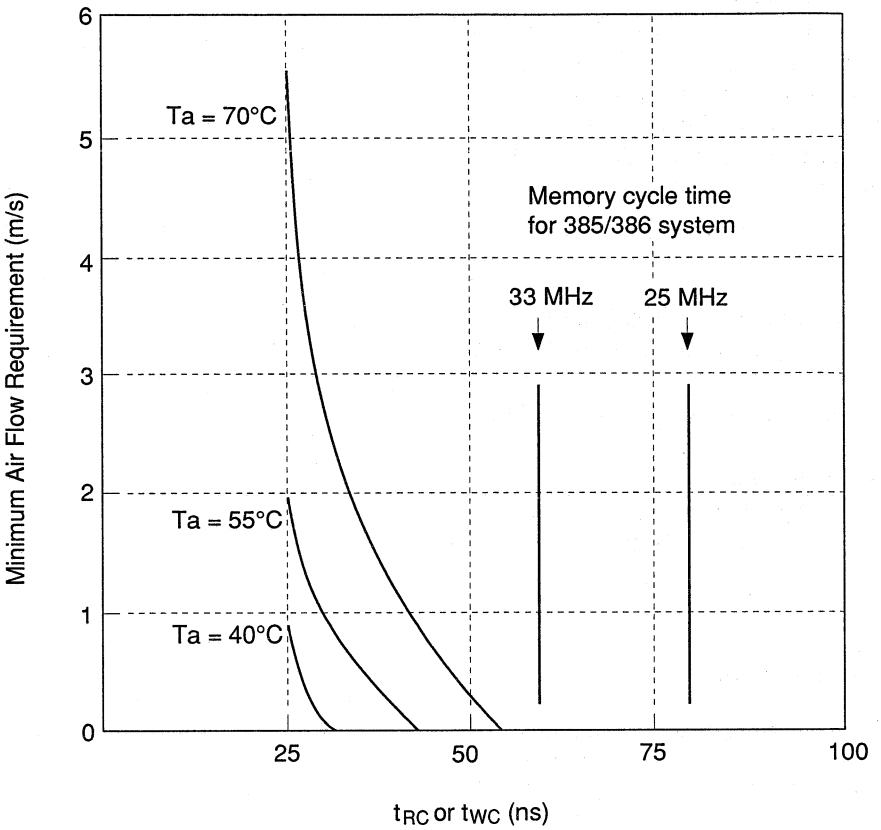


Write Timing Waveform (3) ($\overline{COE}$ = high, $\overline{CS}$ controlled)



Notes:
1. t_{AW} is measured from the later of CALEN going high, or addresses A0-A12 transition with CALEN high to the end of write cycle.
2. t_{AS} is measured from the latest of CALEN going high, or addresses A0-A12 transition with CALEN high to the beginning of write cycle.
3. t_{WR} is measured from the earliest of $\overline{CS0}$, $\overline{CS1}$, $\overline{CE}$, or $\overline{WE}$ going high to the earlier of CALEN going high.
4. A write occurs during the overlap of a low $\overline{CS0}$ or $\overline{CS1}$, a low $\overline{CE}$, and a low $\overline{WE}$.
5. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
6. When MODE input is high, address input A12 will be a "don't care".

Air Flow Requirements



HM67B932 Series

8192-word × 9-Bit × 4 row Static Cache RAM

The Hitachi HM67B932CP-25 is a high speed 288-kbit static cache RAM organized as a 4-way set associative 8 k × 9 or as a direct mapped 32 k × 9 with a 4-row selector for burst mode operation. By using HM67B932CP-25 with high speed standard microprocessors high performance computer systems can be easily designed.
The HM67B932CP-25 is available in a 44-pin PLCC for high density mounting.

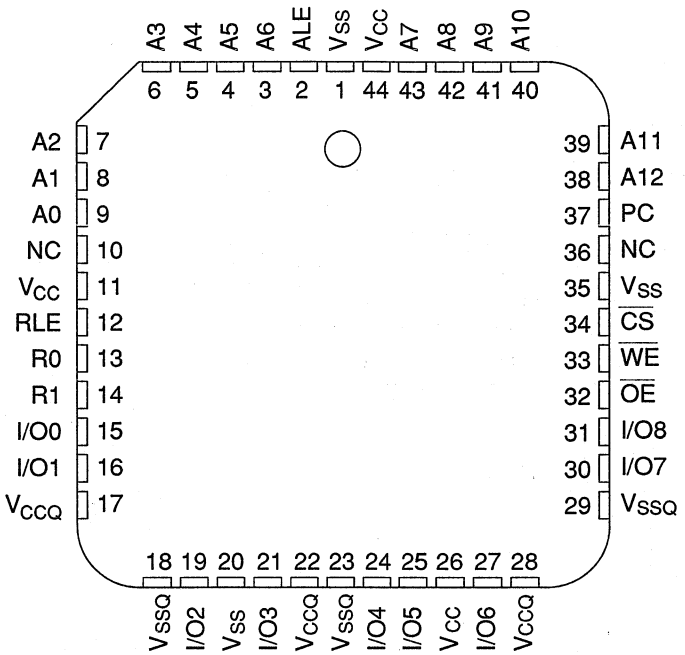
Features

- For high speed cache memory applications
- High speed byte access capability using lower 2-addresses
- Pipeline access capability with on chip address & row latches
- On chip parity generator
- Organization: 288 kbit (8 kw × 9 bit × 4 row)
- High drive capability (C_L = 100 pF)
- PLCC 44 pin
- TTL I/O

Ordering Information

Type No.	Access time	Package
HM67B932CP-25	25 ns	44-pin PLCC (CP-44)

Pin Arrangement



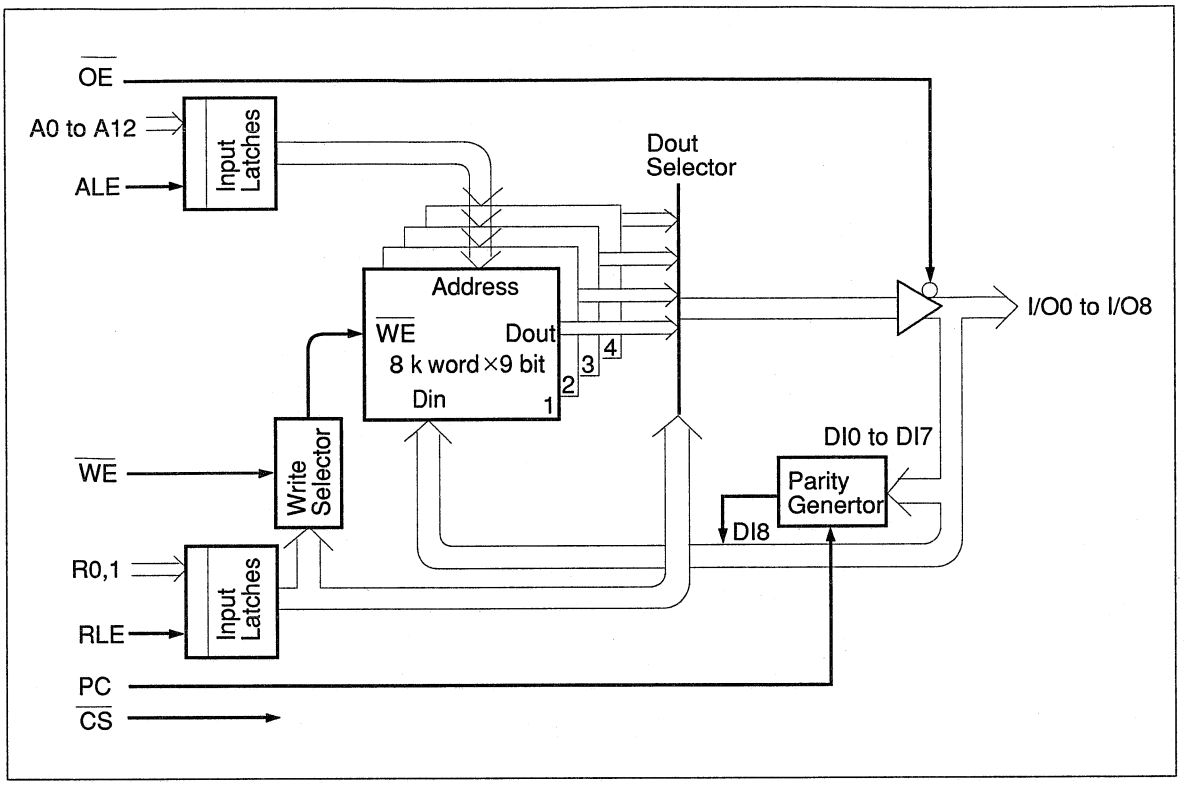
(Top View)

Pin Description

Pin name	Function
ALE	Address latch enable
A0 – A12	Address
$\overline{RLE}$	Row latch enable
R0 – R1	Row
I/O0 – I/O7	Data input/output
I/O8	Data input/output (even parity)
$\overline{CS}$	Chip select

Pin name	Function
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
PC	Parity control
V_{CC}	Power
V_{SS}	Ground
V_{CCQ}	Power (for output transistors)
V_{SSQ}	Ground (for output transistors)

Block Diagram



Function Table

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	PC	Mode	V_{CC} current	I/O pin	Ref. cycle	Notes
H	×	×	×	Not selected	I_{SB}, I_{SB1}	High Z		
L	H	H	×	Output disabled	I_{CC}, I_{CC1}	High Z		
L	L	H	×	Read	I_{CC}, I_{CC1}	Dout	Read cycle No. 1, 2	2
L	H	L	L	Write	I_{CC}, I_{CC1}	Din	Write cycle No. 1, 2	
L	L	L	L	Write	I_{CC}, I_{CC1}	Din	Write cycle No. 3	
L	H	L	H	Write (Parity generate)	I_{CC}, I_{CC1}	Din	Write cycle No. 1	1
L	L	L	H	Write (Parity generate)	I_{CC}, I_{CC1}	Din		1

Notes: 1. DI8 input is ignored and generated as parity bit from DI0 to DI7.
2. Leave DO8 output disconnected (floating) when not used.

Input Latch Table

Address Latch

ALE	Mode	Latch Output
H	Load	Address input
L	Hold	Previous address

Row Address Latch

RLE	Mode	Latch Output
H	Load	Row input
L	Hold	Previous row

Absolute Maximum Rating

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range (with bias)	Tstg (bias)	–10 to +85	°C
Storage temperature	Tstg	–55 to +125	°C

Recommanded DC Operating Conditions (Ta = 0 to +70 °C)

Item	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V	
	V_{IL}	–0.5	—	0.8	V	1

Note: 1. –3.0 V for pulse width ≤ 20 ns.

DC Characteristics (V_{CC} = 5 V ± 10%, Ta = 0 to +70°C, V_{SS} = 0 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Input leakge current	I_{LI}	—	—	2	µA	V_{CC} = 5.5 V, Vin = V_{SS} to V_{CC}
Output leakage current	I_{LO}	—	—	10	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current	I_{CC}	—	—	180	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA
Average operating current	I_{CC1}	—	—	285	mA	Min. Cycle Duty: 100%, $I_{I/O}$ = 0 mA, $\overline{OE}$ = "H"
Standby power supply current	I_{SB}	—	—	50	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}	—	—	30	mA	$\overline{CS}$ ≥ V_{CC} – 0.2 V Vin ≤ 0.2 V or Vin ≥ V_{CC} – 0.2 V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 16 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = – 8 mA
		2.7	—	—	V	I_{OH} = –100 µA

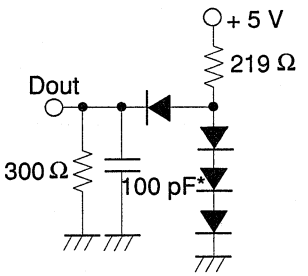
Capacitance (Ta = 25°C, f = 1.0 MHz)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

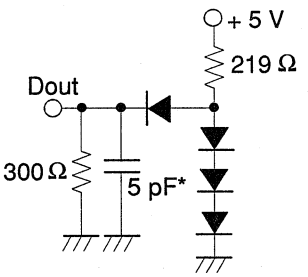
AC Characteristics (V_{CC} = 5 V ± 10%, Ta = 0 to +70°C)

Test Conditions

- Input pulse levels : 0.4 V to 2.4 V
- Input rise and fall times : 4 ns
- Input timing reference levels : 0.8 V, 2.0 V
- Output timing reference levels : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Output load : See figures



Output Load (A)



Output Load (B)

(t_{CHZ}, t_{WHZ}, t_{OHZ}, t_{CLZ}, t_{OW} & t_{OLZ})

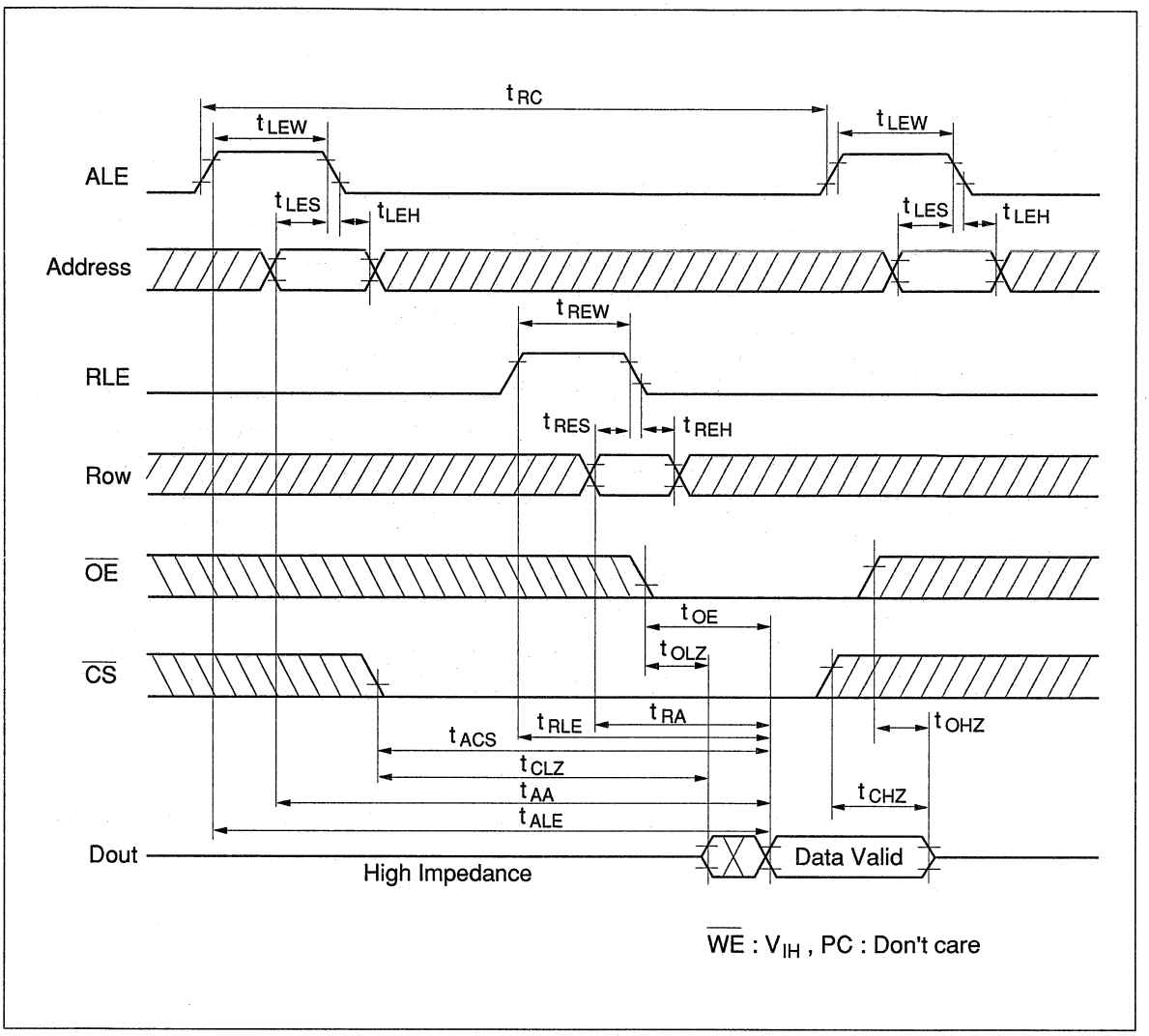
* Including scope and jig

Read Cycle

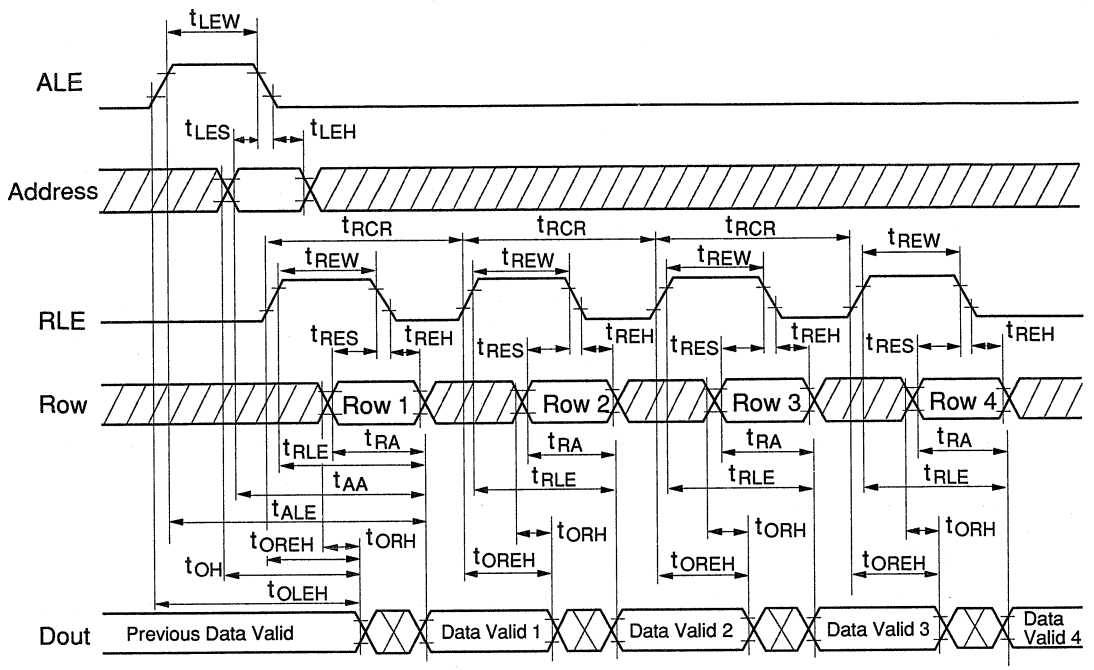
Item	Symbol	Min	Max	Unit	Notes
Read cycle time	t_{RC}	30	—	ns	
Row selector read cycle time	t_{RCR}	18	—	ns	
Address latch enable pulse width	t_{LEW}	7	—	ns	
Address latch enable setup time	t_{LES}	5	—	ns	
Address latch enable hold time	t_{LEH}	3	—	ns	
Row latch enable pulse width	t_{REW}	7	—	ns	
Row latch enable setup time	t_{RES}	5	—	ns	
Row latch enable hold time	t_{REH}	3	—	ns	
Address access time	t_{AA}	—	25	ns	
Output hold from address change	t_{OH}	5	—	ns	
Address latch enable access time	t_{ALE}	—	26	ns	
Output hold from end of address latch hold	t_{OLEH}	5	—	ns	
Row selector access time	t_{RA}	—	13	ns	
Output hold from row selector change	t_{ORH}	0	—	ns	
Row latch enable access time	t_{RLE}	—	14	ns	
Output hold from end of row latch hold	t_{OREH}	0	—	ns	
Chip select access time	t_{ACS}	—	25	ns	
Chip selection to output in low-Z	t_{CLZ}	0	—	ns	1, 2
Chip deselection to output in high-Z	t_{CHZ}	0	10	ns	1, 2
Output enable to output valid	t_{OE}	0	13	ns	
Output enable to output in low-Z	t_{OLZ}	0	—	ns	1, 2
Output disable to output in high-Z	t_{OHZ}	0	10	ns	1, 2

Notes: 1. Transition is measured ±200 mV from steady state voltage with Load (B).
2. This parameter is sampled and not 100% tested.

Read Timing Waveform (1) (Cache Read Cycle)



Read Timing Waveform (2) (Serial Read Cycle with Row Selector)



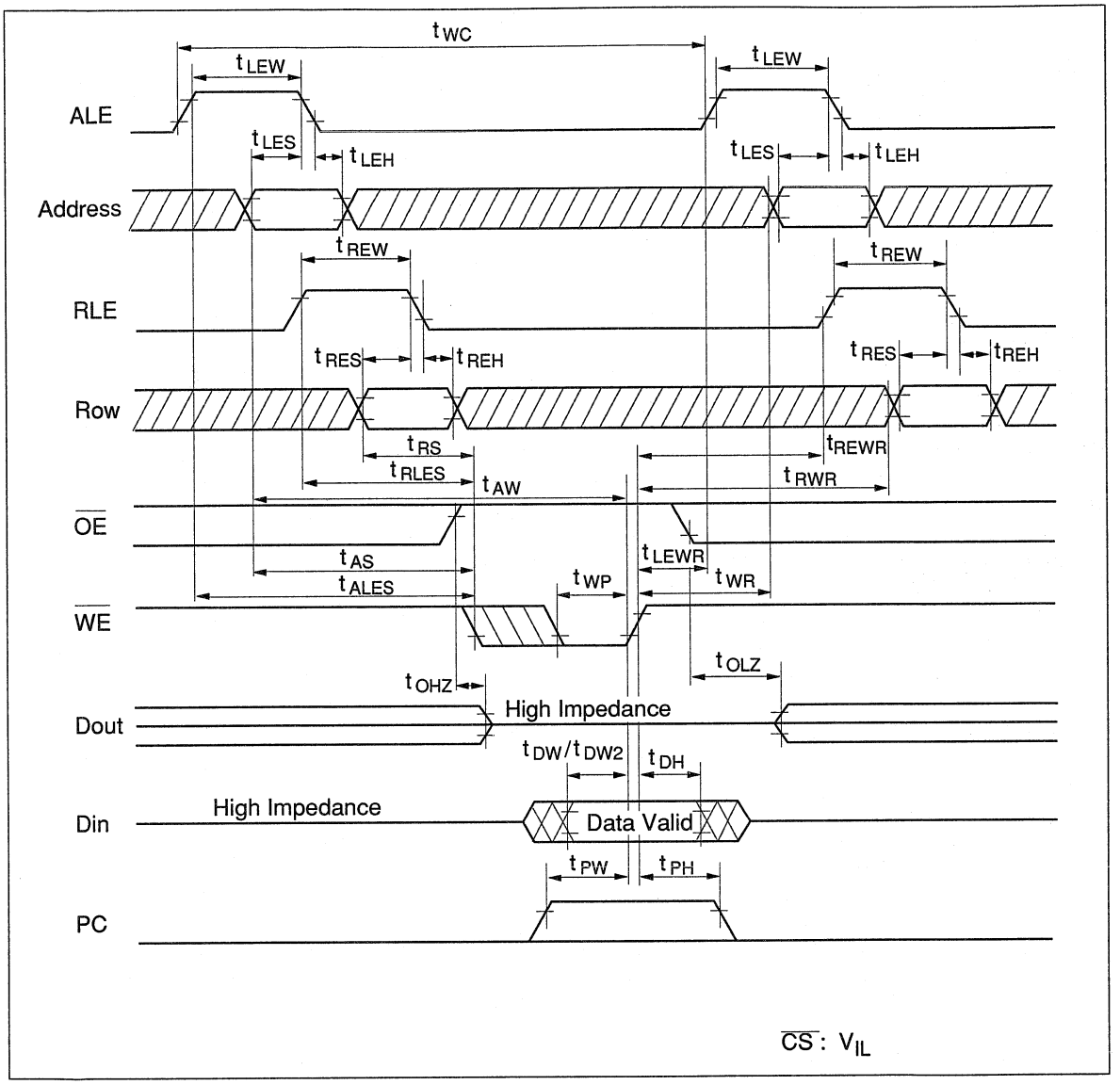
$\overline{WE}$: V_{IH}, $\overline{CS}$: V_{IL}, $\overline{OE}$: V_{IL}, PC : Don't care

Write Cycle

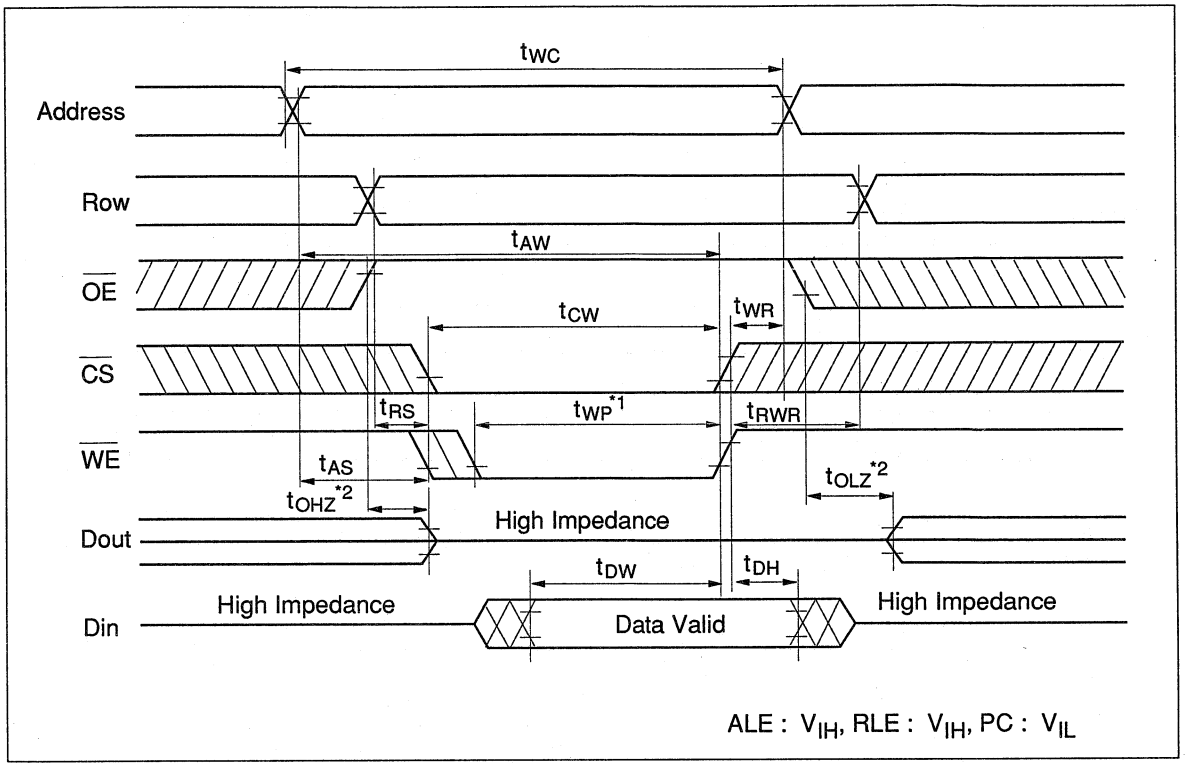
Item	Symbol	Min	Max	Unit	Notes
Write cycle time	t_{WC}	30	—	ns	
Chip selection to end of write	t_{CW}	20	—	ns	
Address setup time	t_{AS}	0	—	ns	
Address latch enable setup time	t_{ALES}	0	—	ns	
Row selector setup time	t_{RS}	0	—	ns	
Row latch enable setup time	t_{RLES}	0	—	ns	
Address valid to end of write	t_{AW}	20	—	ns	
Write pulse width	t_{WP}	14	—	ns	
Write recovery time	t_{WR}	3	—	ns	
Write recovery to end of address latch hold	t_{LEWR}	3	—	ns	
Write recovery to row selector change	t_{RWR}	5	—	ns	
Write recovery to end of row latch hold	t_{REWR}	5	—	ns	
Write to output in high-Z	t_{WHZ}	0	10	ns	1, 2
Data valid to end of write	t_{DW}	10	—	ns	
Data valid to end of write (parity generate mode)	t_{DW2}	15	—	ns	
Data hold time	t_{DH}	0	—	ns	
Output active from end of write	t_{OW}	0	—	ns	1, 2
Parity control setup time	t_{PW}	15	—	ns	
Parity control hold time	t_{PH}	3	—	ns	

Notes: 1. Transition is measured ±200 mV from steady state voltage with Load (B).
2. This parameter is sampled and not 100% tested.

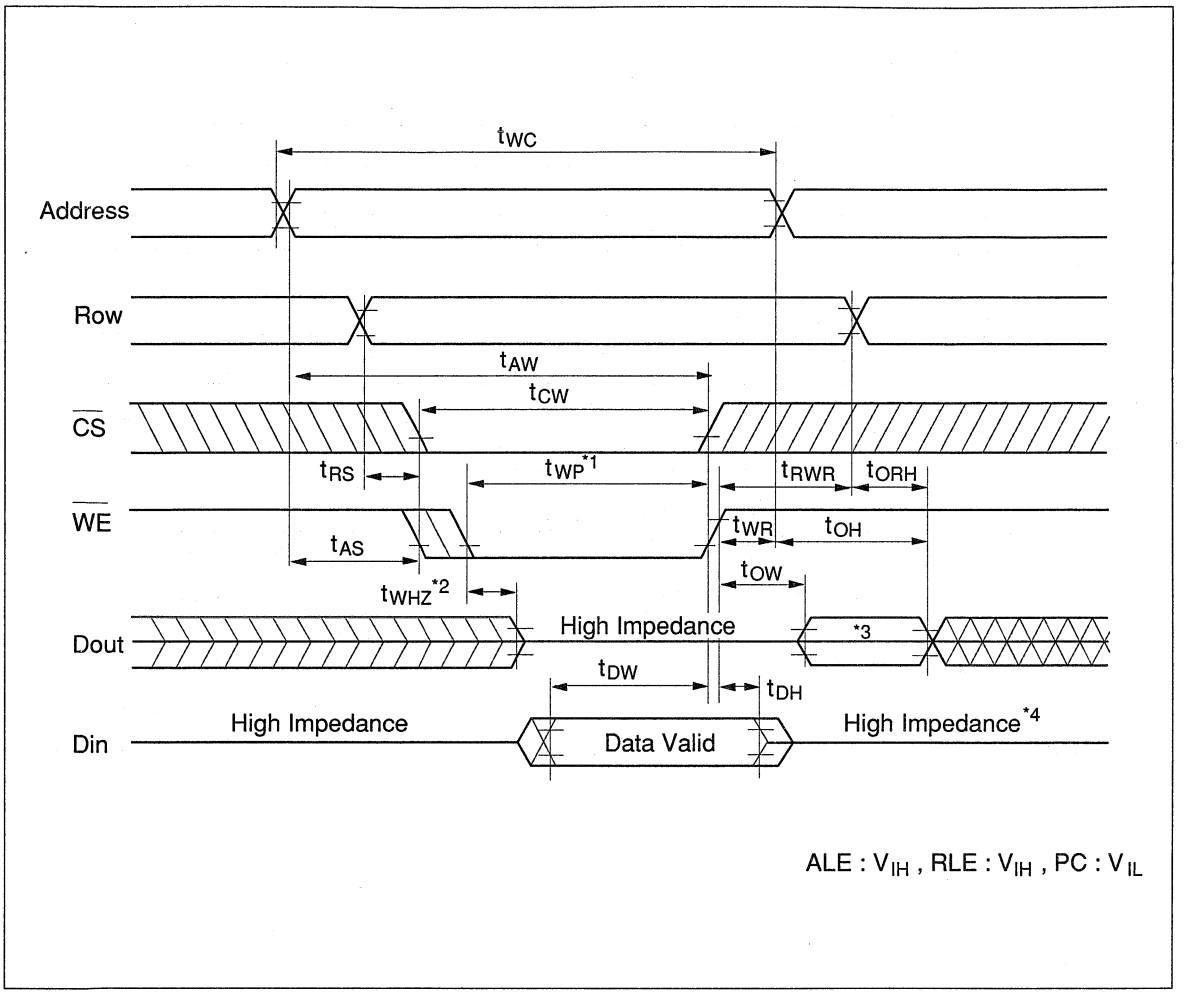
Write Timing Waveform (1) (Cache Write Cycle) *5



Write Timing Waveform (2) ($\overline{OE}$ = Clocked, $\overline{WE}$ controlled)

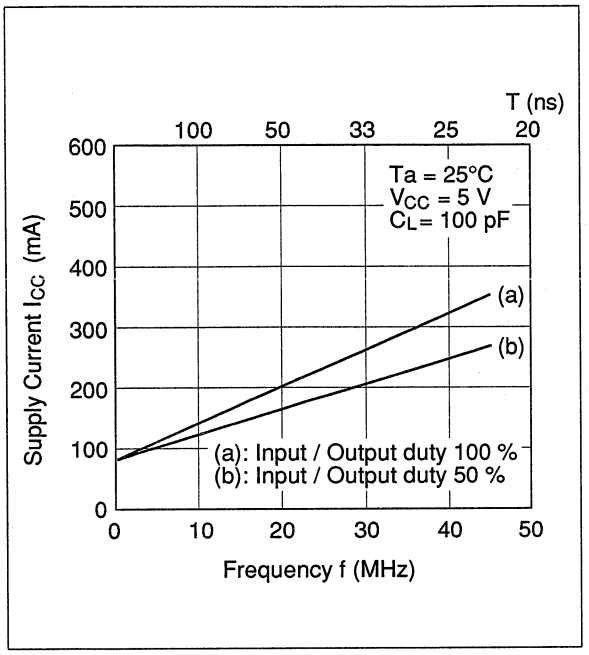


Write Timing Waveform (3) ($\overline{OE}$ = L, $\overline{WE}$ controlled)

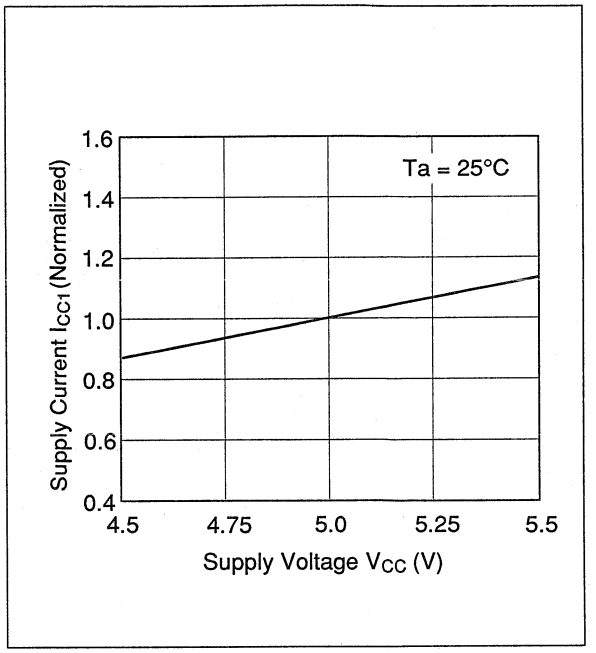


Notes:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
5. DI8 input : Don't care in parity generate mode.

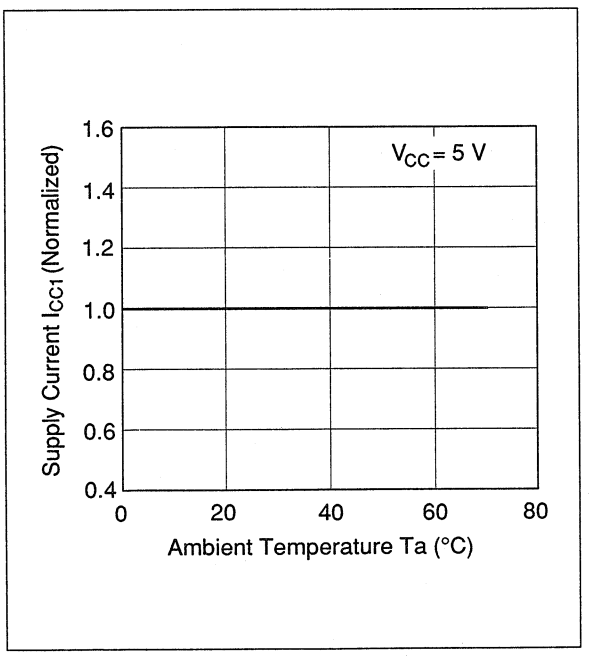
Typical Characteristics



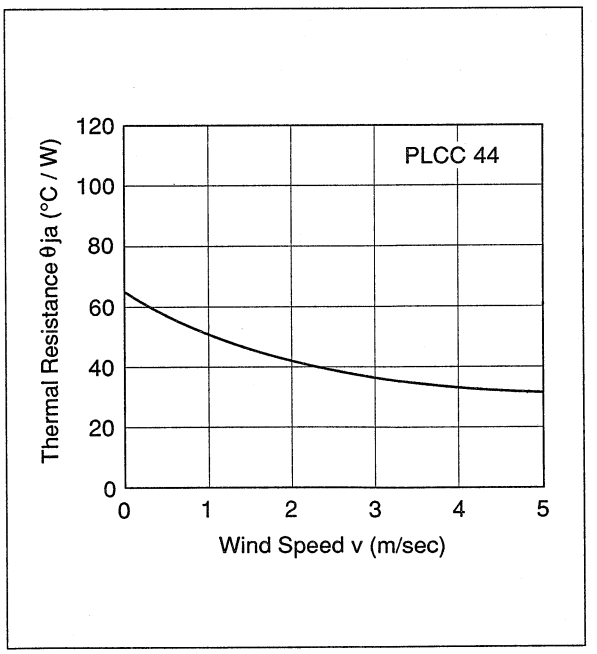
Supply Current vs. Frequency



Supply Current vs. Supply Voltage

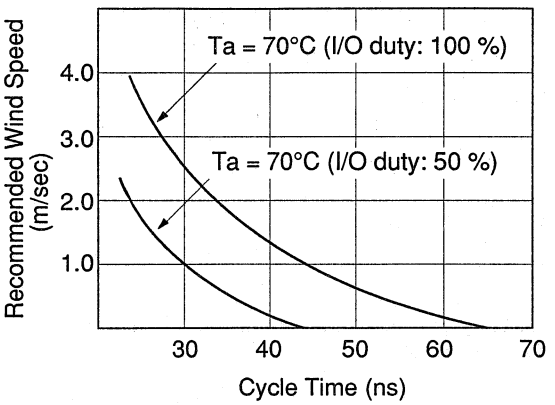


Supply Current vs. Ambient Temperature



Thermal Resistance vs. Wind Speed

Typical Characteristics (cont)



Recommended Wind Speed vs. Cycle Time

HM62A2016 Series

Dual 8192-word × 20-bit Static Cache Memory

The HM62A2016 is a high speed 327680-bit cache memory organized as two banks of 8192 words by 20 bits. The device includes dual address latches, dual chip select latches, data multiplexer with multiple chip enables and output enables. It can be used in a cache memory system adopting Harvard architecture which requires separate instruction and data storages.

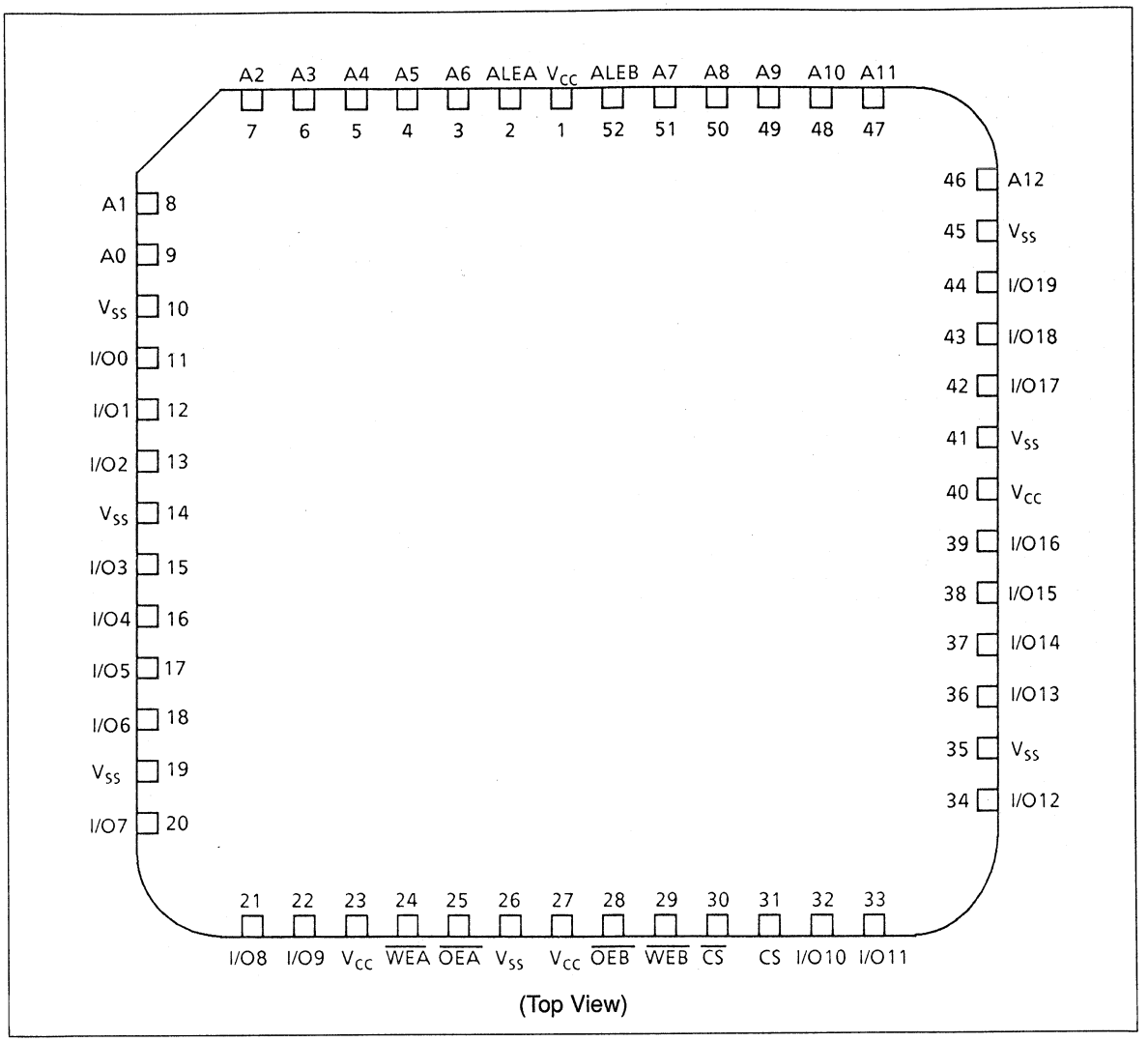
Features

- High speed: up to 33 MHz operation
  Address access time: 17/20/25/30 ns
  Output enable access time: 7/7/8/8 ns
- Dual 8k × 20 memory arrays with data multiplexer
- Dual latches for address and chip select inputs
- Expandable both in width and depth
  Two separate chip selects
- 52-pin PLCC

Ordering Information

Type No.	Access time	Package
HM62A2016CP-17	17 ns	52-pin PLCC (CP-52)
HM62A2016CP-20	20 ns	
HM62A2016CP-25	25 ns	
HM62A2016CP-30	30 ns	

Pin Arrangement

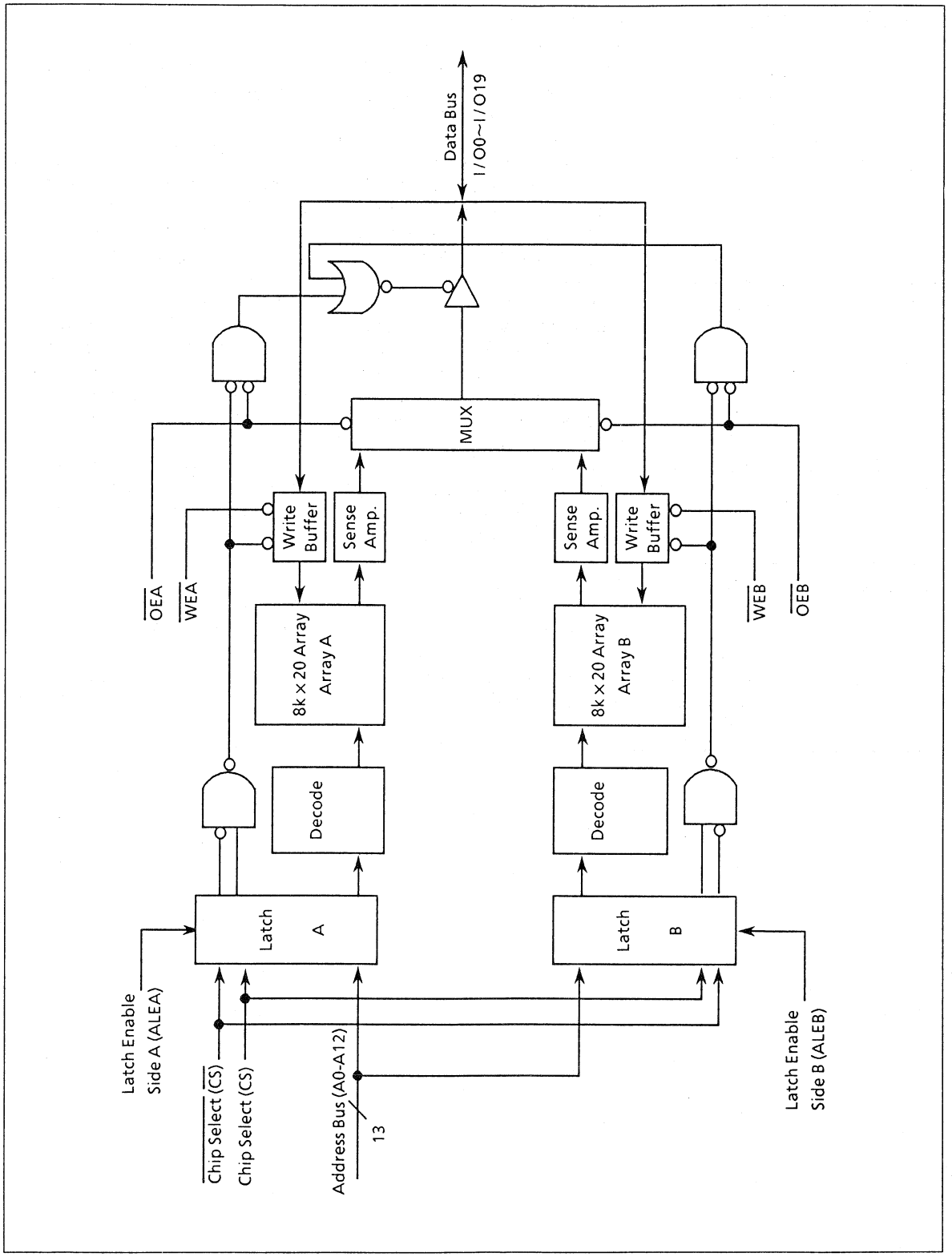


(Top View)

Pin Description

Pin name	Function
A0 – A12	Address inputs
ALEA, ALEB	Latch enables
$\overline{OEA}$, $\overline{OEB}$	Output enables
$\overline{WEA}$, $\overline{WEB}$	Write enables
I/O0-I/O19	Data inputs and outputs
CS, $\overline{CS}$	Chip selects

Block Diagram



Signal Description

Signal name	Pin no.	Signal description
A0 – A12	3-9 46-51	Shared address inputs to both Memory Array A and Memory Array B. Current A0 – A12 values are latched into Latch A or Latch B by the falling edge of ALEA or ALEB.
ALEA, ALEB	2, 52	Latch enable inputs. When ALEA or ALEB is high, Latch A or Latch B is transparent to address and chip select input values. The falling edge of ALEA and ALEB latches current inputs at A0-A12 and current states of CS and $\overline{CS}$. These latched values remain applied to the respective memory arrays until ALEA or ALEB transition to a high state.
$\overline{CS}$, CS	30, 31	Active low and active high chip select inputs. The current states of CS and $\overline{CS}$ are latched by the falling edge of ALEA and ALEB. When $\overline{CS}$ is low and CS is high, read and write access to both arrays is possible. $\overline{CS}$ should be grounded and CS should be tied to V_{CC} in applications where no device depth expansion takes place. See the Depth Expansion Section on page 882 for a detailed description of the chip select function.
$\overline{WEA}$, $\overline{WEB}$	24, 29	Active low write enable inputs. $\overline{WEA}$ controls writing into Array A and $\overline{WEB}$ controls writing into Array B. Both $\overline{WEA}$ and $\overline{WEB}$ must not be both low simultaneously.
$\overline{OEA}$, $\overline{OEB}$	25, 28	Active low output enable inputs. $\overline{OEA}$ and $\overline{OEB}$ are used to control driving of stored data from Array A or Array B onto the I/O lines during read operations. $\overline{OEA}$ and $\overline{OEB}$ must not be both low simultaneously.
I/O0 – I/O19	11-13, 15-18, 20-22, 32-34, 36-39, 42-44	Data inputs and outputs. These are three-state lines that provide data access to both memory arrays.

Function Table

CS	$\overline{CS}$	ALEA	ALEB	$\overline{WEA}$	$\overline{WEB}$	$\overline{OEA}$	$\overline{OEB}$	Operation	I/O Status
L	X	*1	*1	X	X	X	X	Not selected	Outputs high-Z
X	H	*1	*1	X	X	X	X	Not selected	Outputs high-Z
H	L	X	X	H	H	H	H	Data I/O's disabled	Outputs high-Z
H	L	H	X	H	H	L	H	Read from Array A (current addresses)	Data out
H	L	L	X	H	H	L	H	Read from Array A (latched addresses)	Data out
H	L	X	H	H	H	H	L	Read from Array B (current addresses)	Data out
H	L	X	L	H	H	H	L	Read from Array B (latched addresses)	Data out
H	L	X	X	X	X	L*2	L*2	Not allowed in same phase	—
H	L	H	X	L	H	H	H	Write to Array A (current addresses)	Data in
H	L	L	X	L	H	H	H	Write to Array A (latched addresses)	Data in
H	L	X	X	L*3	H	L*3	H	Not allowed in same phase	—
H	L	X	X	L*4	H	H	L*4	Not allowed in same phase	—
H	L	X	H	H	L	H	H	Write to Array B (current addresses)	Data in
H	L	X	L	H	L	H	H	Write to Array B (latched addresses)	Data in
H	L	X	X	H	L*4	L*4	H	Not allowed in same phase	—
H	L	X	X	H	L*3	H	L*3	Not allowed in same phase	—
H	L	X	X	L*5	L*5	X	X	Not allowed in same phase	—

X = Don't care, H = High, L = Low, High-Z = High impedance

Notes: 1. CS and $\overline{CS}$ values shown in the table must have propagated through transparent latches and meet specified chip select setup times before a deselect operation can occur.
2. If data are read simultaneously from both arrays, an undefined data outputs. Specified AC and DC parameters are not guaranteed in this state.
3. Simultaneous reading and writing of a single array or of both arrays is not permitted.
4. Simultaneous reading from one array while writing to the other array is not possible.
5. Simultaneous writing to both arrays is not permitted during normal R3000 based cache operation.

Functional Description

The HM62A2016 is a highly-integrated memory device with several performance-enhancing features which allow direct interfacing to a MIPS R3000 or R3000A RISC processor. Two independent address latches, with fast setup times, are provided on-chip to allow faster addressing of two 8k × 20 memory arrays, Array A and Array B. Address inputs and data I/O lines are shared between the two arrays.

Two sets of $\overline{OE}$ and $\overline{WE}$ inputs, coupled with an on-chip multiplexer control read and write access to each of the arrays. Integrating a 2:1 output data multiplexer on-chip reduces the problem of data bus contention that may occur when using discrete SRAMs and multiplexers, and allows easier synchronization of output enable signals.

$\overline{OEA}$ and $\overline{OEB}$ inputs directly control the driving of stored data at the outputs of the HM62A2016 during read operations. Fast (7 ns) output enable and disable times are matched and permit data to be quickly taken off the data bus as well as driven on. This high level of device feature integration demonstrated by the HM62A2016 allows construction of a dual 32-kbyte cache memory subsystem by combining only three devices together to reach the full 60-bit tag plus data width requirements of the MIPS R3000(A) processor.

The HM62A2016 is designed to permit storage and retrieval of tag address and cache data information to and from the two memory arrays in a direct-mapped, split data/instruction cache format. It is functionally compatible to and meets all MIPS R3000(A) cache memory timing requirement. The HM62A2016 fully supports "pipelined" reads and writes, as described below.

Valid addresses that appear at A0 – A12 inputs are recognized by on-chip Latches A or B when they are transparent (i.e., when ALEA or ALEB inputs are high). Current address input values are latched by the falling edge of ALEA or ALEB.

For an R3000(A) to HM62A2016 cache interface, addresses are latched during the first phase of a 2-phase read operation cycle, and valid data appears at outputs (I/O0 – I/O19) during the second phase.

These addresses will remain latched and applied to Array A or Array B as long as ALEA or ALEB remains low. Similarly, for a write operation, valid addresses are also latched during the first phase, while data is actually written into the addressed location during the second phase.

These sequential reads occur in a pipe-lined manner, where data or instructions are read from one array during the same phase when addresses for a subsequent read from the other array are latched.

Similarly, alternating consecutive writes to the two memory arrays are possible as long as the minimum 2-phase write operation cycle is met with correct timings.

A write operation to a memory array can occur in the phase that immediately precedes or follows a read operation from the other array.

It is not possible to write to or read from both arrays at the same time. Nor is it possible to do more than one read or write per phase. It is not possible to read from or write to the same array in consecutive phases because of the minimum 2-phase read/write operation cycle requirements. See the Function Table on page 881 for a detailed listing of prohibited operations, as well as legitimate read and write modes.

Array A and B are interchangeable and can arbitrarily be designated as for data or instruction storage.

Depth Expansion

Overview

Each HM62A2016 has a latched active high chip select input (CS) as well as an active low input ($\overline{CS}$). Depth expansion is achieved by connecting address line (A13) into CS and $\overline{CS}$ inputs of two HM62A2016's and grounding or tying to V_{CC} the other remaining chip select of each device, as shown in figure 1. Corresponding (A or B) control inputs ($\overline{OE}$, $\overline{WE}$, and ALE) of depth–expanded HM62A 2016's should be tied together.

The latched chip select function of the HM62A2016 is designed to permit one array to be latched "on" (active for read or write access) while the other corresponding array of a different device is turned "off".

Detailed Description

The current states of CS and $\overline{CS}$ are latched on-chip by the falling edge of ALEA or ALEB. An

"array select" state (both CS = 1 and $\overline{CS}$ = 0), that passes through a single transparent Latch (A or B) and meets t_{CSL} timing, will permit that particular array (A or B) to be active for read and write access. An array in a selected state will remain active as long as its ALE input remains low. If an array select state is recognized by both transparent latches (A and B), then both arrays for that HM62A2016 device will be active.

A "deselect" state (either CS = 0 or $\overline{CS}$ = 1) that propagates through a single transparent latch (A or B) and meets the minimum specified chip select setup time will disable both read and write access to that respective array (Array A or Array B). If a deselecting input state passes through both transparent latches A and B, then read and write access to both arrays is disabled.

Example

An example of consecutive reads from two depth-expanded HM62A2016's is shown in Read Cycle No.2. In the first phase, an instruction is read from the I-cache of the "low RAM". At the beginning of this phase, A13 transitions from low to high and causes the selection of the D-cache array of the "high RAM" for a read operation in the following phase. This high A13 state also deselects the D-cache array of the "low RAM" for the following phase.

Consecutive operations are possible because the latching of A13 to select or deselect an array can occur in the same phase as a read or write operation from another array of a different HM62A2016.

As a further example, the timings for a depth-expanded store-load sequence are shown in Write Cycle No.2 on page 890.

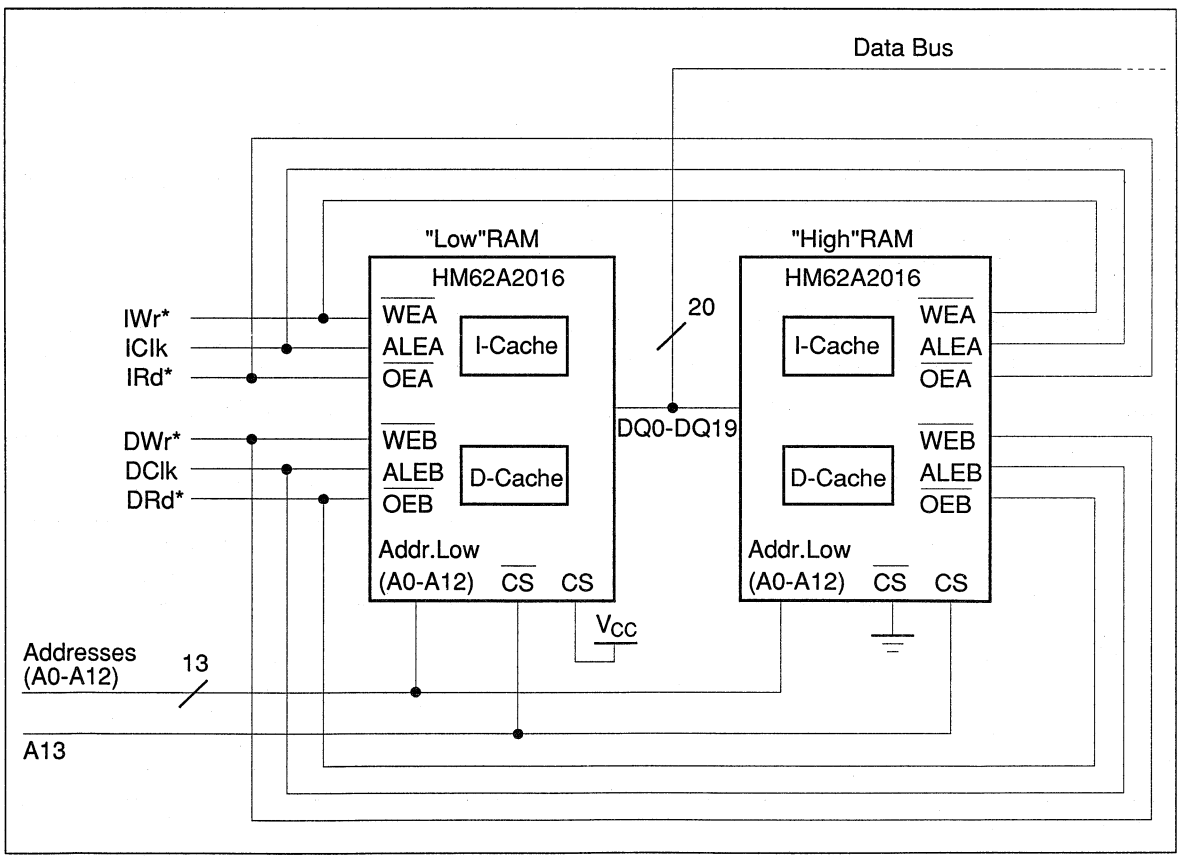


Figure 1 16k × 20 × 2 Cache SRAM from two 8k × 20 × 2 Cache SRAMs

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	−0.5*1 to +7.0	V
Voltage on any input pin relative to V_{SS}	Vin	−0.5*1 to V_{CC} + 0.3	V
Power dissipation	P_T	2.0	W
Operation temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C

Note: 1. Vin min = −2.5 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C, exceeding minimum air flow requirement : see page 891)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.0	5.25	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	V_{CC} +0.3	V
Input low (logic 0) voltage	V_{IL}	−0.5*1	—	0.8	V

Notes: 1. V_{IL} min = −2.0 V for pulse width ≤ 10 ns.
2. The supply voltage with all V_{CC} pins must be on the same level.
The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V, exceeding minimum air flow requirement : see page 891)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	µA	V_{CC} = Max. Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	2.0	µA	Output disable $V_{I/O}$ = V_{SS} to V_{CC}
Active operating power supply current	I_{CC}	—	—	330	mA	Vin = V_{SS} to V_{CC}, outputs open load, Iout = 0 mA tcycle = Min. cycle $\overline{CS}$ = V_{IL} max CS = V_{IH} min
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = −4mA

Note: 1. Typical limits are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1 MHz)*1

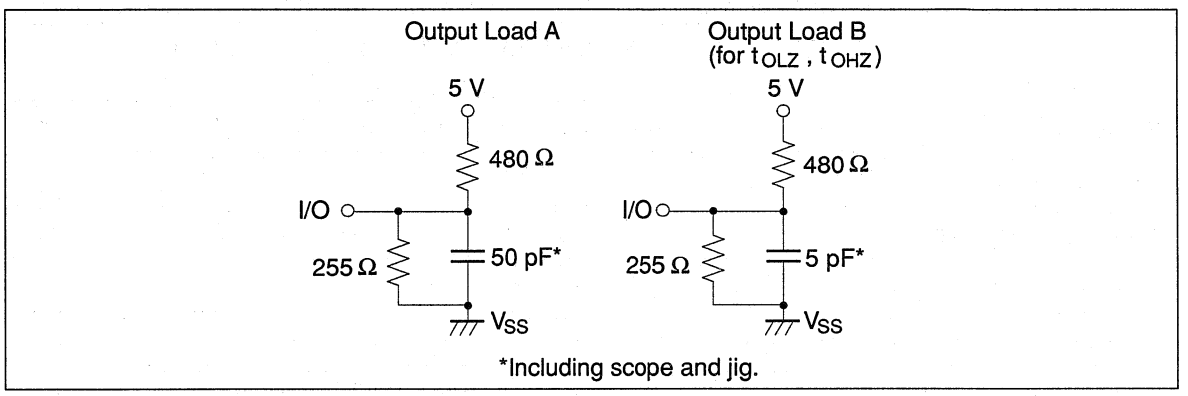
Parameter	Symbol	Min	Max	Unit	Test conditions
Input capacitance	Cin	—	5	pF	Vin = 0 V
Input / Output capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC} = 5 V ± 5%, Ta = 0 to +70°C, exceeding minimum air flow requirement : see page 891)

Test Conditions

- Input and output timing reference levels: 1.5 V
- Input pulse levels: V_{SS} to 3 V
- Input rise and fall times: 3 ns
- Output load: See figures



Read Cycle

	Frequency:	33 MHz		25 MHz		20 MHz		16.67 MHz		
		HM62A2016 -17		HM62A2016 -20		HM62A2016 -25		HM62A2016 -30		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Read cycle time	t_{RC}	17	—	20	—	25	—	30	—	ns
Address valid to output valid	t_{AA}	—	17	—	20	—	25	—	30	ns
Chip select access time	t_{ACS}*1	—	17	—	20	—	25	—	30	ns
Output enable low to output valid	t_{OE}	—	7	—	7	—	8	—	8	ns
Output enable low to output low-Z	t_{OLZ}	1	—	2	—	2	—	2	—	ns
Output enable high to output high-Z	t_{OHZ}	0	7	0	7	0	8	0	8	ns
Output hold from latch enable	t_{LOH}	3	—	3	—	3	—	3	—	ns
Address setup to latch enable low	t_{ASL}	5	—	5	—	5	—	5	—	ns
Address hold from latch enable low	t_{AHL}	2	—	2	—	2	—	2	—	ns

	Frequency:	33 MHz		25 MHz		20 MHz		16.67 MHz		
		HM62A2016 -17		HM62A2016 -20		HM62A2016 -25		HM62A2016 -30		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Chip select setup to latch enable low	t_{CSL}*1	5	—	5	—	5	—	5	—	ns
Chip select hold from latch enable low	t_{CSH}*1	2	—	2	—	2	—	2	—	ns
Output enable separation time	t_{OSP}	2	—	2	—	2	—	2	—	ns
Latch high to address valid	t_{LAV}	3	—	3	—	3	—	3	—	ns

Note: 1. Indicates depth expansion parameter only. These parameters apply for both CS and $\overline{CS}$.

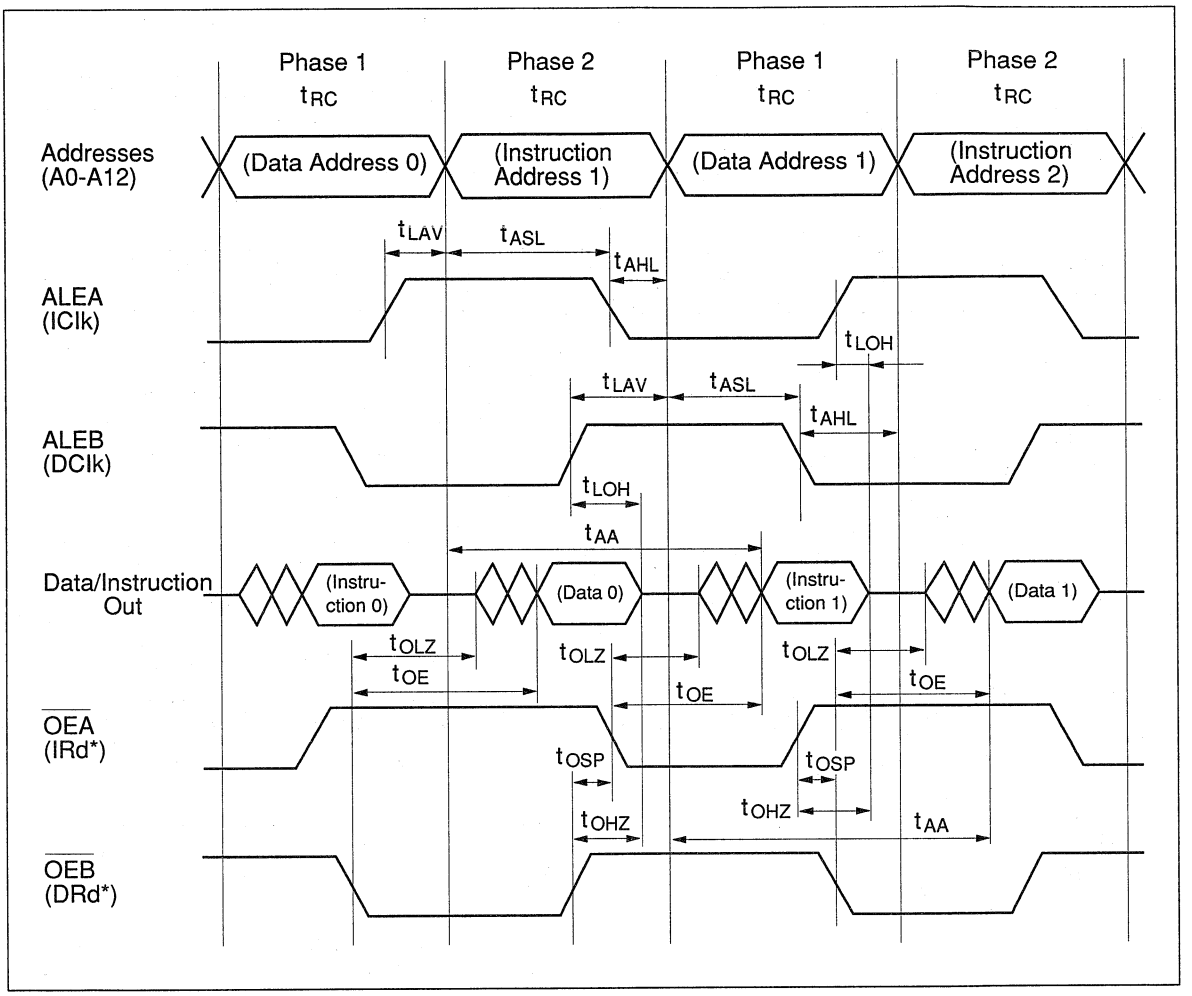
Write Cycle

	Frequency:	33 MHz		25 MHz		20 MHz		16.67 MHz		
		HM62A2016 -17		HM62A2016 -20		HM62A2016 -25		HM62A2016 -30		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Write cycle time	t_{WC}	17	—	20	—	25	—	30	—	ns
Address valid to end of write	t_{AW}	12	—	15	—	20	—	25	—	ns
Data valid to end of write	t_{DS}	6	—	8	—	8	—	10	—	ns
Data hold from end of write	t_{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	10	—	15	—	17	—	22	—	ns
Chip enable to end of write	t_{CW}*1	12	—	15	—	20	—	25	—	ns
Address setup time before write start	t_{AS}	0	—	0	—	0	—	0	—	ns
Latch enable hold from end of write	t_{WHL}	0	—	0	—	0	—	0	—	ns
Address setup to latch enable low	t_{ASL}	5	—	5	—	5	—	5	—	ns
Address hold from latch enable low	t_{AHL}	2	—	2	—	2	—	2	—	ns
Chip select setup to latch enable low	t_{CSL}*1	5	—	5	—	5	—	5	—	ns
Chip select hold from latch enable low	t_{CSH}*1	2	—	2	—	2	—	2	—	ns
Read/write separation time	t_{RWS}	2	—	2	—	2	—	2	—	ns
Latch high to address valid	t_{LAV}	3	—	3	—	3	—	3	—	ns

Note: 1. Indicates depth expansion parameter only. These parameters apply for both CS and $\overline{CS}$.

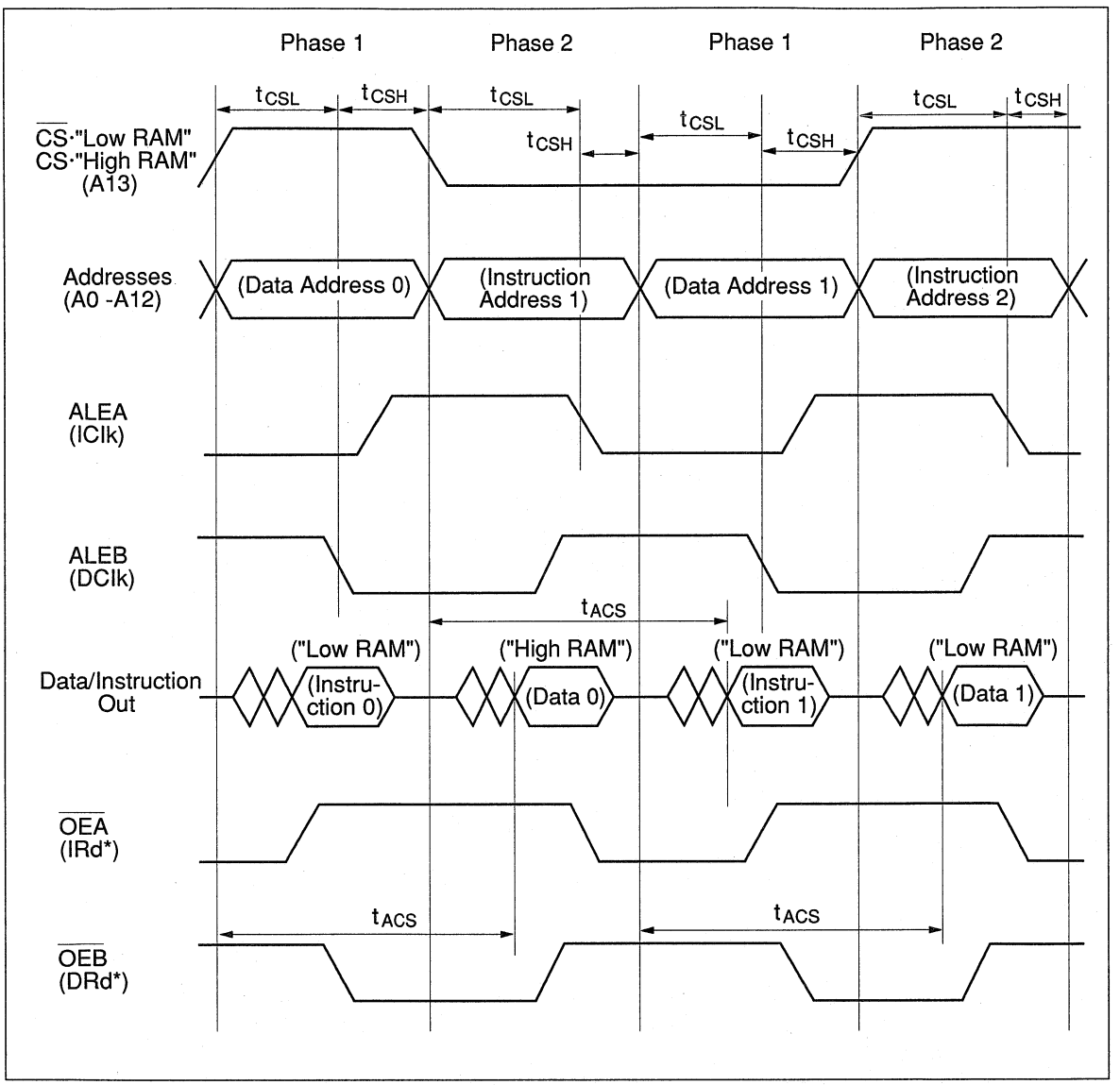
Timing Waveforms

Read Cycle No.1 ($\overline{CS}$ = low, CS, $\overline{WEA}$, $\overline{WEB}$ = high)



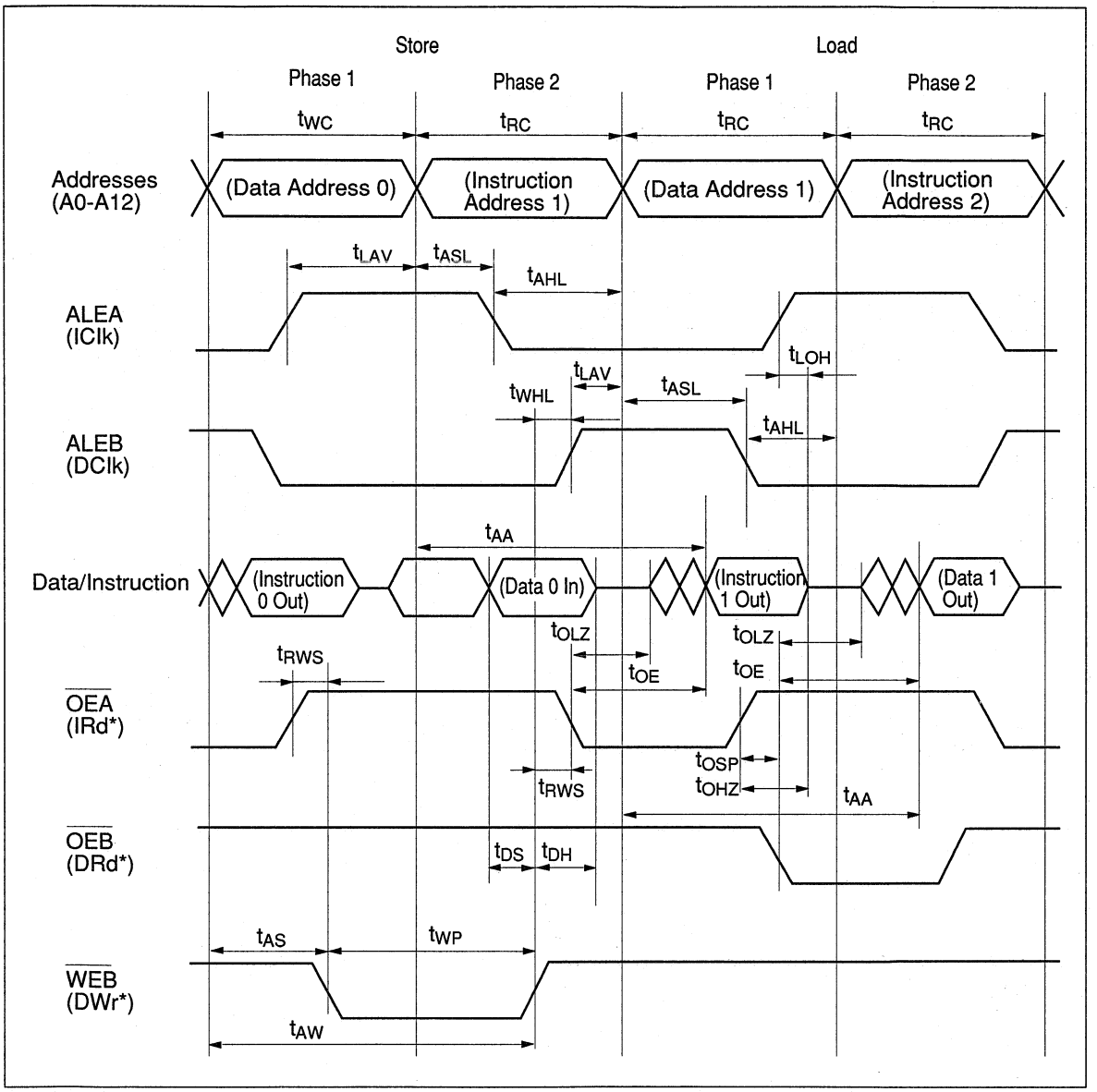
Notes:
1. All timing parameters are measured with output load A unless otherwise noted.
2. Read cycle time (t_{RC}) refers to read operations with current addresses applied to a transparent (high) latch.
   Read timing parameters are referenced from the last valid address to the first transition address.
3. Transition is measured ±200 mV from steady state voltage with output load B for t_{OLZ} and t_{OHZ}. These parameters are sampled and not 100% tested.

Read Cycle No. 2 ($\overline{WEA}$, $\overline{WEB}$ = high)
(Consecutive Reads from Two Depth-expanded HM62A2016's)



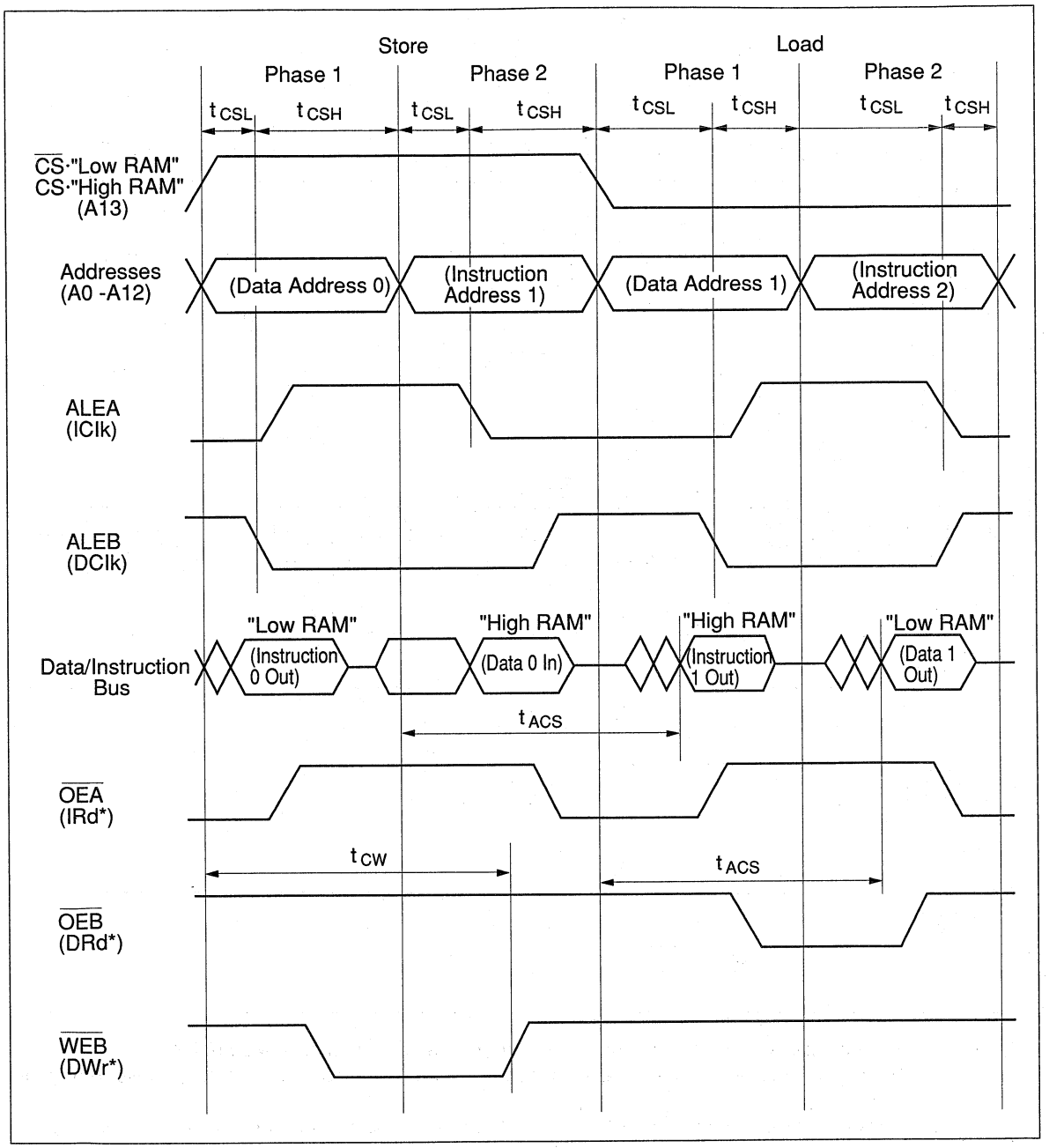
Note: 1. All other non depth-expansion parameters shown in Read Cycle No. 1 still apply, and are not shown for simplicity.

Write Cycle No. 1 ($\overline{CS}$ = low, CS, $\overline{WEA}$ = high)



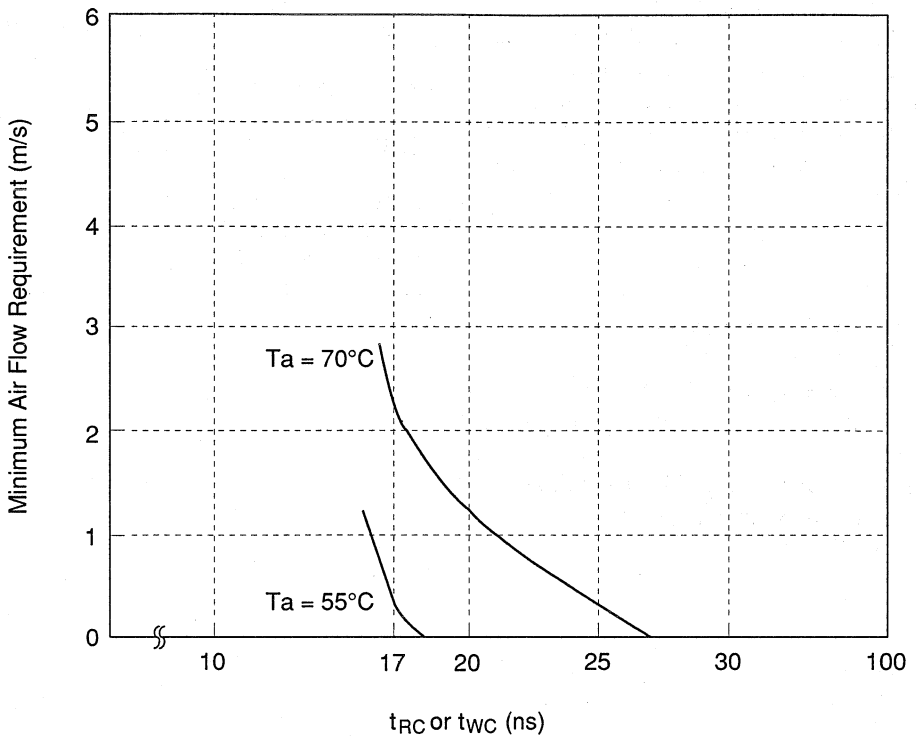
Notes:
1. All timing parameters are measured with output load A unless otherwise noted.
2. Write cycle time refers to write operations with current addresses applied to a transparent (high) latch.
3. Transition is measured ±200mV from steady state voltage with output load B for t_{OLZ}, t_{OHZ}. These parameters are sampled and not 100% tested.

Write Cycle No. 2 ($\overline{WEA}$ = high)
(Store-Load Sequence of Two Depth-expanded HM62A2016's)



Note: 1. All other non depth-expansion parameters shown in Write Cycle No. 1 still apply, and are not shown for simplicity.

Air Flow Requirements



HM62A2017 Series

Dual 8,192-word × 20-bit Static Cache Memory

The HM62A2017 is a high speed 327680-bit cache memory organized as two banks of 8192 words by 20 bits. The device includes dual address latches, dual chip select latches, data multiplexer with multiple chip enables and output enables. It can be used in a cache memory system adopting Harvard architecture which requires separate instruction and data storages.

Features

- High speed: up to 33 MHz operation
  Address access time: 17/20/25/30 ns
  Output enable access time: 7/7/8/8 ns
- Dual 8k × 20 memory arrays with data multiplexer
- Dual latches for address and chip select inputs
- Expandable both in width and depth
  Two separate chip selects
- 68-pin PLCC

Ordering Information

Type No.	Access time	Package
HM62A2017CP-17	17 ns	68-pin PLCC (CP-68)
HM62A2017CP-20	20 ns	
HM62A2017CP-25	25 ns	
HM62A2017CP-30	30 ns	

HM62A9128/8128 Series — Preliminary

131,072-word × 9(8)-bit Synchronous Cache SRAM

Features

- For high speed cache memory applications
- Pipeline access capability with on-chip address, strobe and I/O resisters
- Organization: 128 kword x 9(8) bit
- SOJ - 32-pin
- TTL I/O

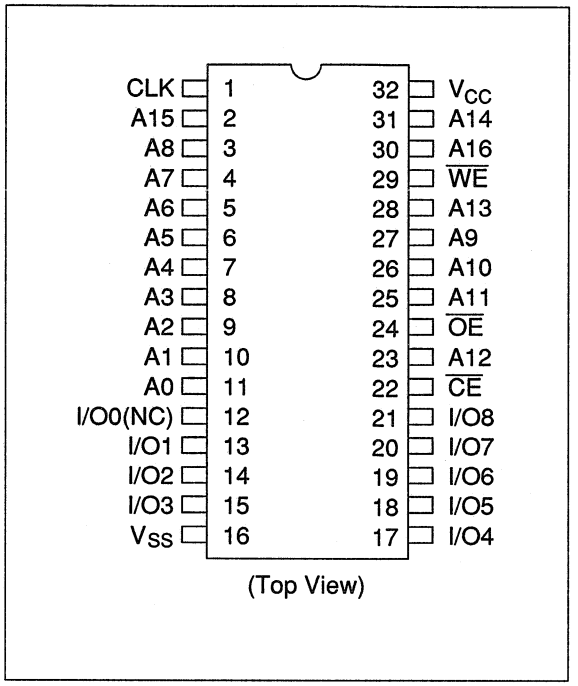
Main Characteristics

Item	Spec.	Remarks
Clock cycle time	20 ns (min)	
Clock to data valid	10 ns (max)	
Power dissipation	825 mW (max)	50 MHz

Ordering Information

Type No.	Clock cycle time	Package
HM62A9128JP–20	20 ns	32-pin 400 mil SOJ (CP-32D)
HM62A8128JP–20	20 ns	

Pin Arrangement



(Top View)

Pin Description

Pin name	Function
A0 – A16	Address
I/O0 – I/O8	Input/output
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
CLK	Clock input
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection (for x 8)

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

ECL RAM

HM10494 Series

16384-word × 4-bit Fully Decoded Random Access Memory

The HM10494 is ECL 10K compatible, 16384-word by 4-bits read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

Features

- 16384-word × 4-bit organization
- Fully compatible with 10K ECL level
- Address access time: 10/12 ns (max)
- Write pulse width: 6/8 ns (min)
- Low power dissipation: 800 mW (typ)
- Output obtainable by wired-OR (open emitter)

Ordering Information

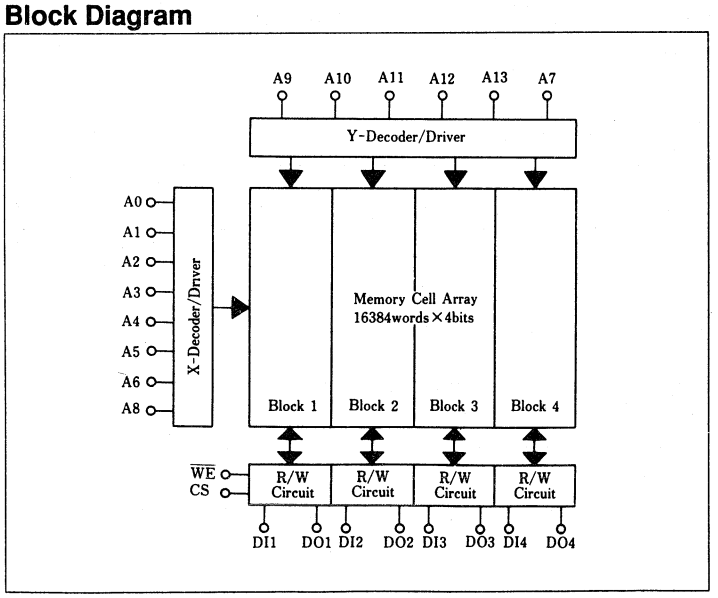
Type No.	Access Time	Package
HM10494-10	10 ns	400 mil 28-pin
HM10494-12	12 ns	Cerdip (DG-28N)
HM10494JP-12	12 ns	300 mil 28-pin Plastic SOJ (CP-28DN)

Function Table

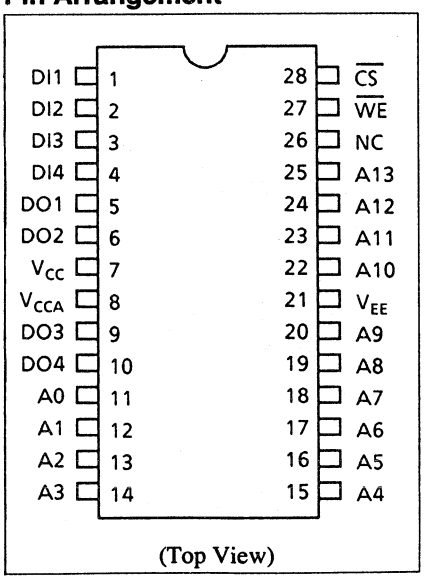
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*1	Read

Notes: ×; Irrelevant *1; Read Out Noninvert

Block Diagram



Pin Arrangement



(Top View)

Absolute Maximum Ratings (Tj = 125°C max[*1], Ta = 25°C[*2])

Item	Symbol	SOJ Rating	Cerdip Rating	Unit
Supply voltage	V_{EE} to V_{CC}	+0.5 to –7.0	+0.5 to –7.0	V
Input voltage	Vin	+0.5 to V_{EE}	+0.5 to V_{EE}	V
Output current	Iout	–30	–30	mA
Power dissipation	P_T	1.0	—	W
Operating temperature	Topr	0 to +75[*4]	—	°C
Storage temperature	Tstg	–55 to +125	–65 to +150	°C
Storage temperature	Tstg (Bias)[*3]	–10 to +85[*4]	–55 to +125	°C

Notes: 1. SOJ
2. Cerdip
3. Under bias (V_{EE} = –6 Vmin)
4. Case temperature; Tc

Electrical Characteristics

DC Characteristics (V_{EE}=–5.2 V, R_L=50Ω to –2.0 V, Tc=0 to +75°C[1] Ta=0 to +75°C[2], air flow exceeding 2 m/sec)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test Conditions	
Output Voltage	V_{OH}	–1000	—	–840	mV	Vin = V_{IHA} or V_{ILB}	0°C
		–960	—	–810			+25°C
		–900	—	–720			+75°C
	V_{OL}	–1870	—	–1665			0°C
		–1850	—	–1650			+25°C
		–1830	—	–1625			+75°C
Output Threshold Voltage	V_{OHC}	–1020	—	—	mV	Vin = V_{IHB} or V_{ILA}	0°C
		–980	—	—			+25°C
		–920	—	—			+75°C
	V_{OLC}	—	—	–1645			0°C
		—	—	–1630			+25°C
		—	—	–1605			+75°C
Input Voltage	V_{IH}	–1145	—	–840	mV	Guaranteed Input Voltage High for All Inputs	0°C
		–1105	—	–810			+25°C
		–1045	—	–720			+75°C
	V_{IL}	–1870	—	–1490		Guaranteed Input Voltage Low for All Inputs	0°C
		–1850	—	–1475			+25°C
		–1830	—	–1450			+75°C
Input Current	I_{IH}	—	—	220	μA	Vin = V_{IHA}	0 to +75°C
	I_{IL}	0.5	—	170		Vin = V_{ILB} $\overline{CS}$	0 to +75°C
		–50	—	—		Vin = V_{ILB} Others	0 to +75°C
Supply Current	I_{EE}	–200	—	—	mA	All Inputs and Outputs Open	Ta = 0°C
		–200	—	—			Ta = 75°C

Notes: 1. SOJ
2. Cerdip

AC Characteristics (V_{EE}=–5.2 V ±5%, Tc=0 to +75°C[1] Ta=0 to +75°C[2], air flow exceeding 2 m/sec)

Read Mode

Item	Symbol	HM10494-10 Min	Typ	Max	HM10494-12 Min	Typ	Max	Unit	Test Conditions
Chip Select Access Time	t_{ACS}	—	—	6	—	—	8	ns	
Chip Select Recovery Time	t_{RCS}	—	—	6	—	—	8	ns	
Address Access Time	t_{AA}	—	—	10	—	—	12	ns	

Write Mode

Item	Symbol	HM10494-10			HM10494-12			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Write Pulse Width	tw	6	—	—	8	—	—	ns	t_{WSA} = t_{WSA} min
Data Setup Time	t_{WSD}	2	—	—	2	—	—	ns	
Data Hold Time	t_{WHD}	2	—	—	2	—	—	ns	
Address Setup Time	t_{WSA}	2	—	—	2	—	—	ns	tw = tw min
Address Hold Time	t_{WHA}	2	—	—	2	—	—	ns	
Chip Select Setup Time	t_{WSCS}	2	—	—	2	—	—	ns	
Chip Select Hold Time	t_{WHCS}	2	—	—	2	—	—	ns	
Write Disable Time	t_{WS}	—	—	6	—	—	8	ns	
Write Recovery Time	t_{WR}	—	—	12	—	—	14	ns	

Notes: 1. SOJ
2. Cerdip

Rise/Fall Time

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Output Rise Time	tr	—	2	—	ns	
Output Fall Time	tf	—	2	—	ns	

Capacitance (SOJ)

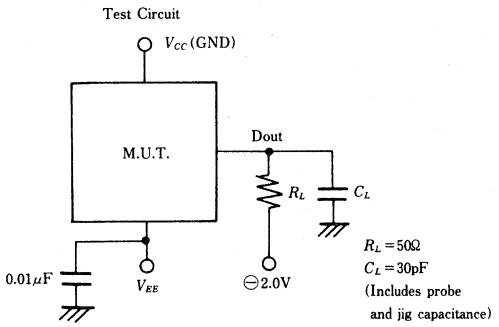
Item	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance	Cin	—	3	—	pF	$\overline{WE}$
		—	2	—	pF	Others
Output capacitance	Cout	—	3	—	pF	

Capacitance (Cerdip)

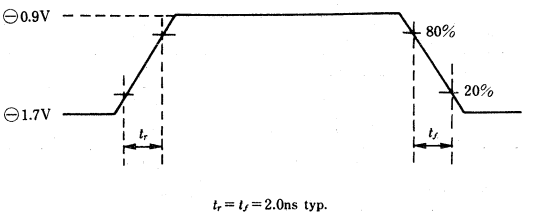
Item	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance	Cin	—	5	—	pF	$\overline{WE}$, $\overline{CS}$, DI1, DI2
		—	3	—	pF	Others
Output capacitance	Cout	—	3	—	pF	

Test Circuit and Waveforms

Loading Condition

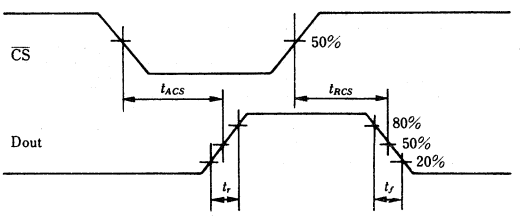


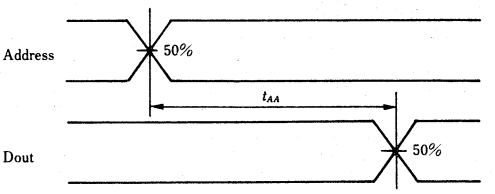
Input Pulse



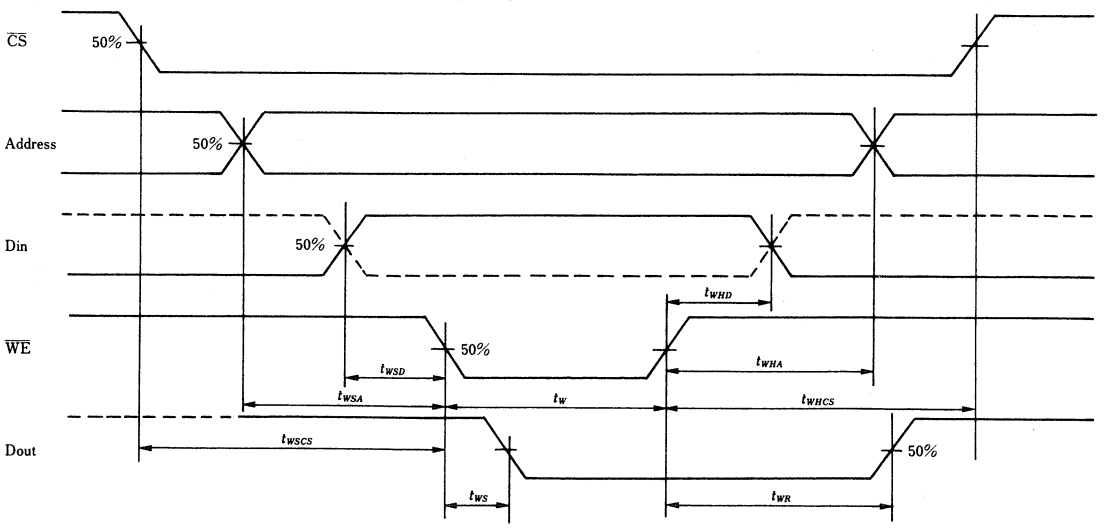
$t_r = t_f = 2.0$ns typ.

Read Mode





Write Mode



HM10490 Series

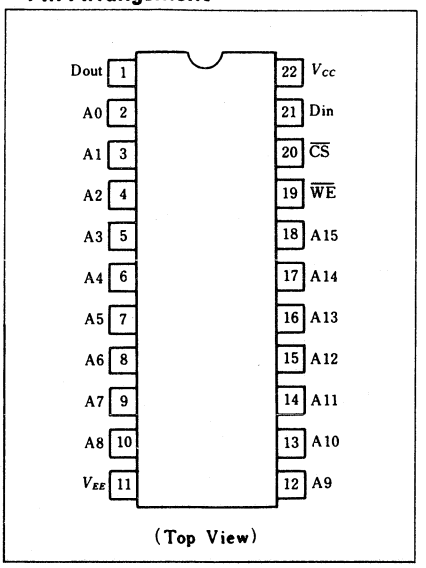
65536-words x 1-bit Fully Decoded Random Access Memory

The HM10490 is ECL 10k compatible, 65536-words by 1-bit, read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

Features

- 65,536-words x 1-bit organization
- Fully compatible with 10k ECL level
- Address access time . . . . . 10/12ns (max.)
- Write pulse width . . . . . 6/8ns (min.)
- Low power dissipation . . . . . 570mW (typ.)
- Output obtainable by wired-OR (open emitter)

Pin Arrangement



(Top View)

Ordering Information

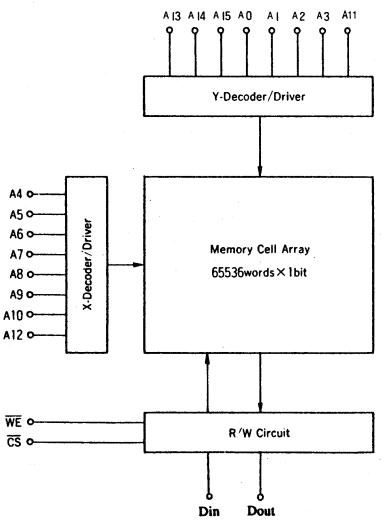
Type No.	Access Time	Package
HM10490-10	10 ns	300mil 22pin Cerdip (DG-22N)
HM10490-12	12 ns	

Function Table

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) ×: Irrelevant
*: Read Out Noninvert

Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	℃
Storage Temperature	T_{stg}(Bias)*	−55 to +125	℃

*Under Bias (V_{EE}=−6Vmin)

Electrical Characteristics

DC Characteristics (V_{EE} = -5.2V, R_L = 50Ω to -2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	min(B)	typ	max(A)	Unit	Test Condition	
Output Voltage	V_{OH}	-1000	—	-840	mV	$V_{in}=V_{IHA}$ or V_{ILB}	0°C
		-960	—	-810			+25°C
		-900	—	-720			+75°C
	V_{OL}	-1870	—	-1665			0°C
		-1850	—	-1650			+25°C
		-1830	—	-1625			+75°C
Output Threshold Voltage	V_{OHC}	-1020	—	—	mV	$V_{in}=V_{IHB}$ or V_{ILA}	0°C
		-980	—	—			+25°C
		-920	—	—			+75°C
	V_{OLC}	—	—	-1645			0°C
		—	—	-1630			+25°C
		—	—	-1605			+75°C
Input Voltage	V_{IH}	-1145	—	-840	mV	Guaranteed Input Voltage High for All Inputs	0°C
		-1105	—	-810			+25°C
		-1045	—	-720			+75°C
	V_{IL}	-1870	—	-1490		Guaranteed Input Voltage Low for All Inputs	0°C
		-1850	—	-1475			+25°C
		-1830	—	-1450			+75°C
Input Current	I_{IH}	—	—	220	μA	$V_{in}=V_{IHA}$	0 to +75°C
	I_{IL}	0.5	—	170		$\overline{CS}$ $V_{in}=V_{ILB}$	0 to +75°C
		-50	—	—		Others	
Supply Current	I_{EE}	-180	—	—	mA	All Inputs and Outputs Open.	0°C
		-180	—	—			+75°C

AC Characteristics (V_{EE} = -5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Read Mode

Item	Symbol	HM10490-10 min	typ	max	HM10490-12 min	typ	max	Unit	Test Condition
Chip Select Access Time	t_{ACS}	—	—	6	—	—	8	ns	
Chip Select Recoverry Time	t_{RCS}	—	—	6	—	—	8	ns	
Address Access Time	t_{AA}	—	—	10	—	—	12	ns	

Write Mode

Item	Symbol	HM10490-10 min	typ	max	HM10490-12 min	typ	max	Unit	Test Condition
Write Pulse Width	t_W	6	—	—	8	—	—	ns	$t_{WSA}=t_{WSAmin}$
Data Setup Time	t_{WSD}	2	—	—	2	—	—	ns	
Data Hold Time	t_{WHD}	2	—	—	2	—	—	ns	
Address Setup Time	t_{WSA}	2	—	—	2	—	—	ns	$t_W=t_{Wmin}$
Address Hold Time	t_{WHA}	2	—	—	2	—	—	ns	
Chip Select Setup Time	t_{WSCS}	2	—	—	2	—	—	ns	
Chip Select Hold Time	t_{WHCS}	2	—	—	2	—	—	ns	
Write Disable Time	t_{WS}	—	—	6	—	—	8	ns	
Write Recovery Time	t_{WR}	—	—	12	—	—	14	ns	

Rise/Fall Time

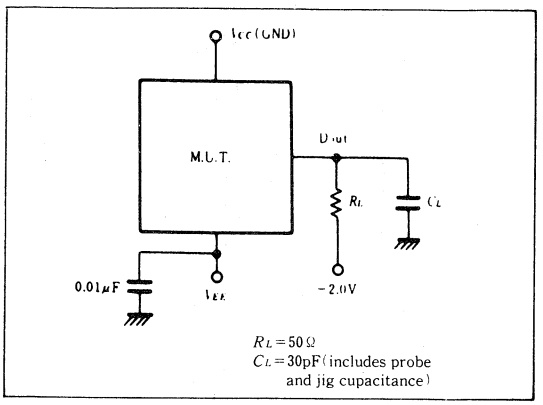
Item	Symbol	min(B)	typ	max(A)	Unit	Test Condition
Output Rise Time	t_r	—	2	—	ns	
Output Fall Time	t_f	—	2	—	ns	

Capacitance

Item	Symbol	min(B)	typ	max(A)	Unit	Test Condition
Input Capacitance	C_{in}	—	3	—	pF	
Output Capacitance	C_{out}	—	5	—	pF	

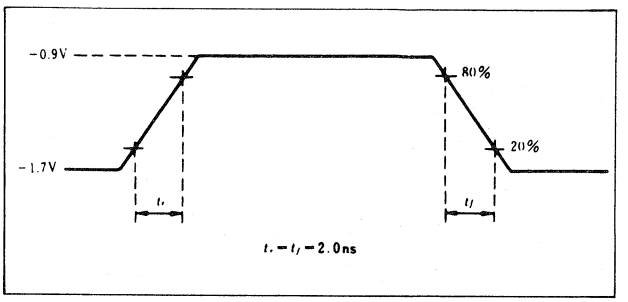
Test Circuit and Waveforms

Loading Condition

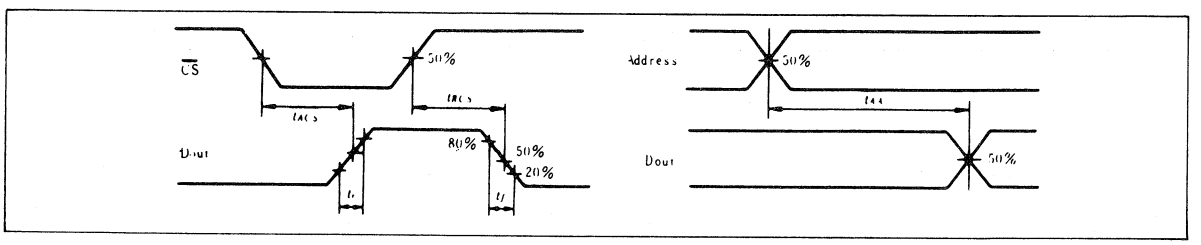


$R_L = 50\,\Omega$
$C_L = 30$pF (includes probe and jig cupacitance)

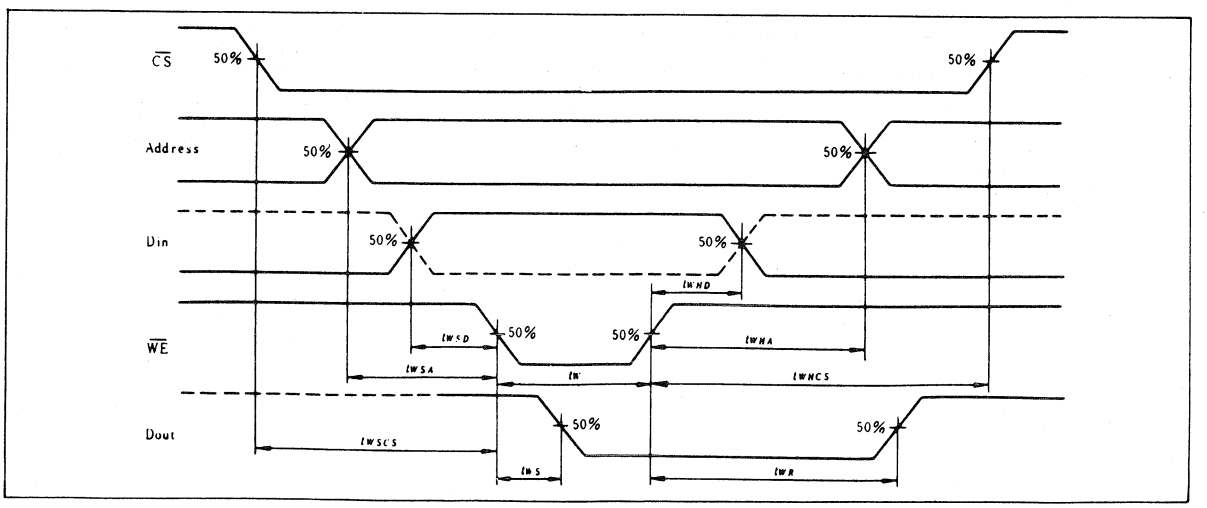
Input Pulse



Read Mode



Write Mode



HM10500-15

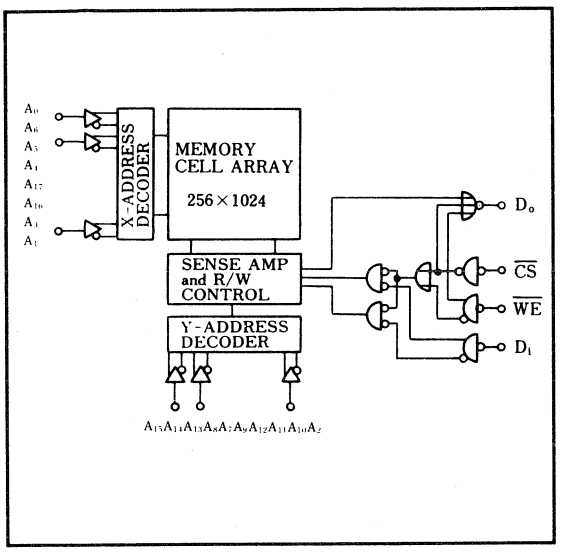
262144-words x 1-bit Fully Decoded Random Access Memory

HM10500-15 is ECL 10K compatible, 262144-words x 1-bit, read/write random access memory developed for high speed systems such as main memories for super computers.

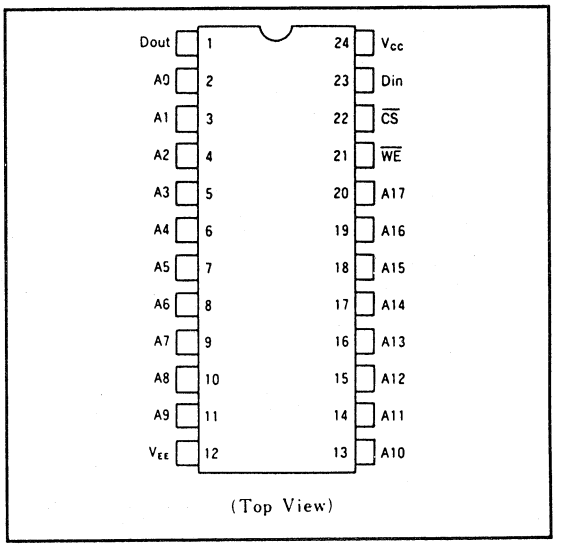
Features

- 262,144-words x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time : 15ns (max)
- Write pulse width : 10ns (min)
- Low power dissipation : 520mW (typ)
- Output obtainable by wired-OR (open emitter)

Block Diagram



Pin Arrangement



(Top View)

Function Table

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Dout*	Read

Notes) X : Irrelevant
* : Read Out Noninvert

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg} (Bias)*	−55 to +125	°C

* Under Bias (V_{EE} = −6Vmin)

Electrical Characteristics

DC Characteristics (V_{EE}=−5.2V, R_L=50Ω to −2.0V, Ta=0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	min (B)	typ	max (A)	Unit	Test Condition	
Output Voltage	V_{OH}	−1000	–	−840	mV	V_{in}=V_{IHA} or V_{ILB}	0°C
		−960	–	−810			+25°C
		−900	–	−720			+75°C
	V_{OL}	−1870	–	−1665			0°C
		−1850	–	−1650			+25°C
		−1830	–	−1625			+75°C
Output Threshold Voltage	V_{OHC}	−1020	–	–	mV	V_{in}=V_{IHB} or V_{ILA}	0°C
		−980	–	–			+25°C
		−920	–	–			+75°C
	V_{OLC}	–	–	−1645			0°C
		–	–	−1630			+25°C
		–	–	−1605			+75°C
Input Voltage	V_{IH}	−1075	–	−840	mV	Guaranteed Input Voltage High for All Inputs	0°C
		−1055	–	−810			+25°C
		−1045	–	−720			+75°C
	V_{IL}	−1870	–	−1550		Guaranteed Input Voltage Low for All Inputs	0°C
		−1850	–	−1525			+25°C
		−1830	–	−1475			+75°C
Input Current	I_{IH}	–	–	220	μA	V_{in}=V_{IHA}	0 to +75°C
	I_{IL}	0.5	–	170		$\overline{CS}$ — V_{in}=V_{ILB}	0 to +75°C
		−50	–	–		Others — V_{in}=V_{ILB}	
Supply Current	I_{EE}	−180	–	–	mA	All Inputs and Outputs Open, Test Pin 12	Ta=0°C
		−180	–	–			Ta=75°C

AC Characteristics (V_{EE}=−5.2V±5%, Ta=0 to +75°C, air flow exceeding 2m/sec)

Read Mode

Item	Symbol	min	typ	max	Unit	Test Condition
Chip Select Access Time	t_{ACS}	–	–	15	ns	
Chip Select Recovery Time	t_{RCS}	–	–	10	ns	
Address Access Time	t_{AA}	–	–	15	ns	

Write Mode

Item	Symbol	min	typ	max	Unit	Test Condition
Write Pulse Width	t_W	10	–	–	ns	t_{WSA}=2ns
Data Setup Time	t_{WSD}	2	–	–	ns	
Data Hold Time	t_{WHD}	3	–	–	ns	
Address Setup Time	t_{WSA}	2	–	–	ns	t_W=10ns
Address Hold Time	t_{WHA}	3	–	–	ns	
Chip Select Setup Time	t_{WSCS}	2	–	–	ns	
Chip Select Hold Time	t_{WHCS}	3	–	–	ns	
Write Disable Time	t_{WS}	–	–	10	ns	
Write Recovery Time	t_{WR}	–	–	18	ns	

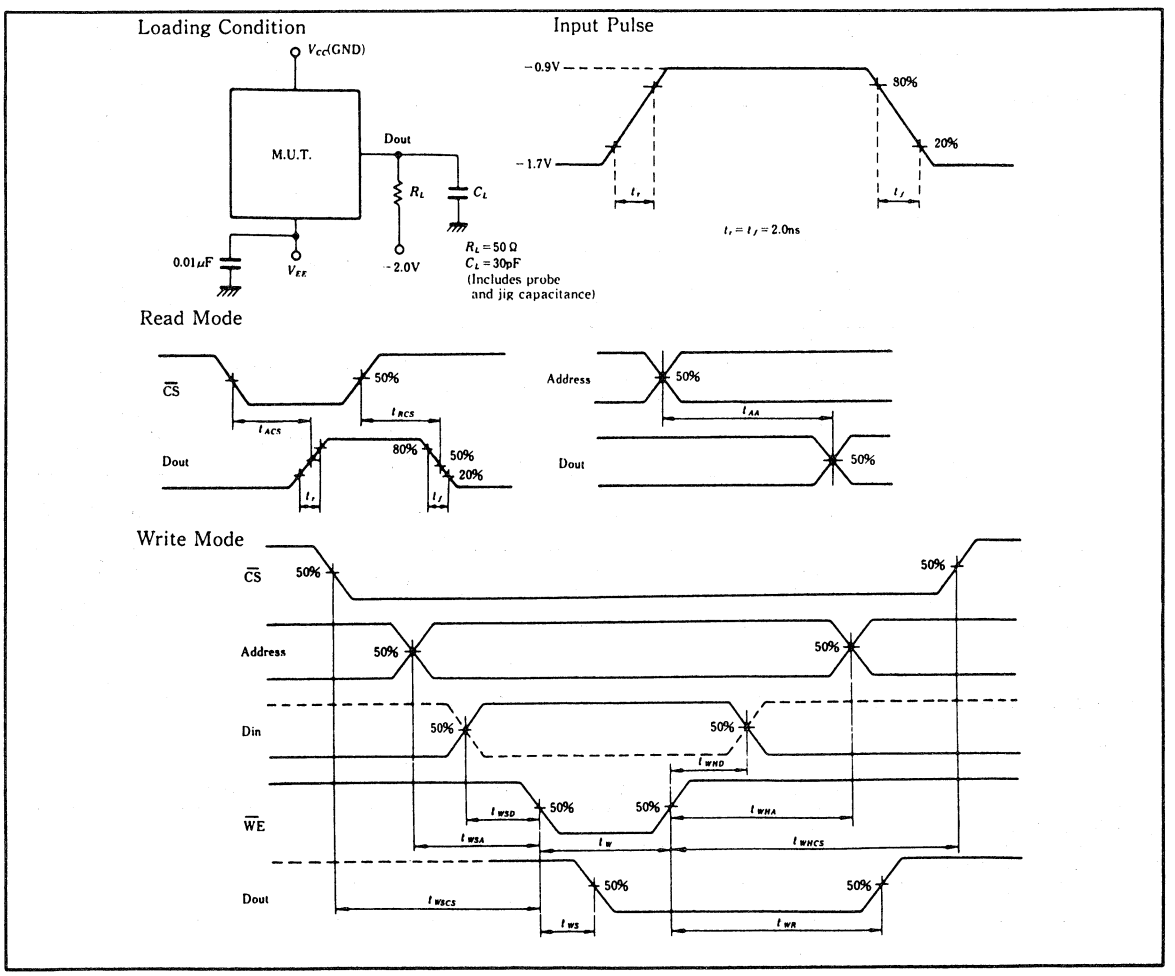
Rise/Fall Time

Item	Symbol	min	typ	max	Unit	Test Condition
Output Rise Time	t_r	–	2	–	ns	
Output Fall Time	t_f	–	2	–	ns	

Capacitance

Item	Symbol	min	typ	max	Unit	Test Condition
Input Capacitance	C_{in}	–	3	–	pF	
Output Capacitance	C_{out}	–	5	–	pF	

Test Circuit and Waveforms



HM100494/HM101494 Series

16384-Word × 4-Bit Fully Decoded Random Access Memory

The HM100494/HM101494 are ECL 100K compatible, 16384-words by 4-bits read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

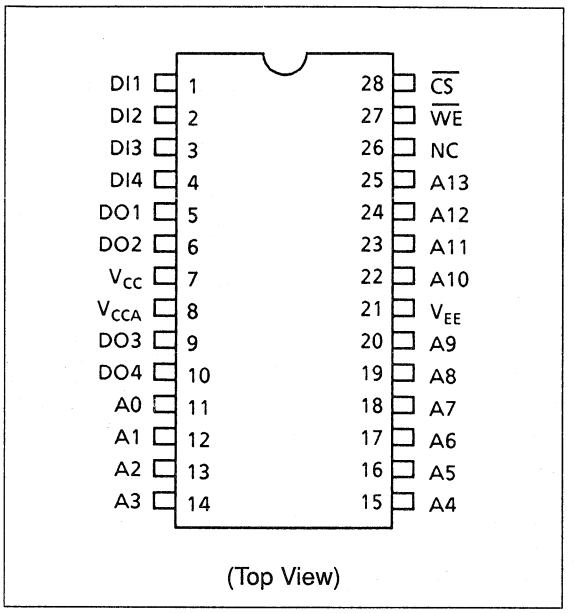
Features

- 16384 × 4-bits organization
- Fully compatible with 100k ECL level
- Address access time: 8/10/12 ns (max)
- Write pulse width: 5/6/8 ns (min)
- Low power dissipation:
  - 100K: 650 mW (typ)
  - 101K(10/12 ns): 730 mW (typ)
  - 101K(8 ns): 800 mW (typ)
- Output obtainable by wired-OR (open emitter)

Ordering Information

Type No.	Access time	Package
HM100494JP-10	10 ns	300-mil 28-pin plastic SOJ (CP-28DN)
HM100494JP-12	12 ns	
HM101494JP-8	8 ns	
HM101494JP-10	10 ns	
HM101494JP-12	12 ns	
HM101494-10	10 ns	400-mil 28-pin cerdip (DG-28N)
HM101494-12	12 ns	
HM101494F-8	8 ns	28-pin ceramic flat (FG-28D)

Pin Arrangement

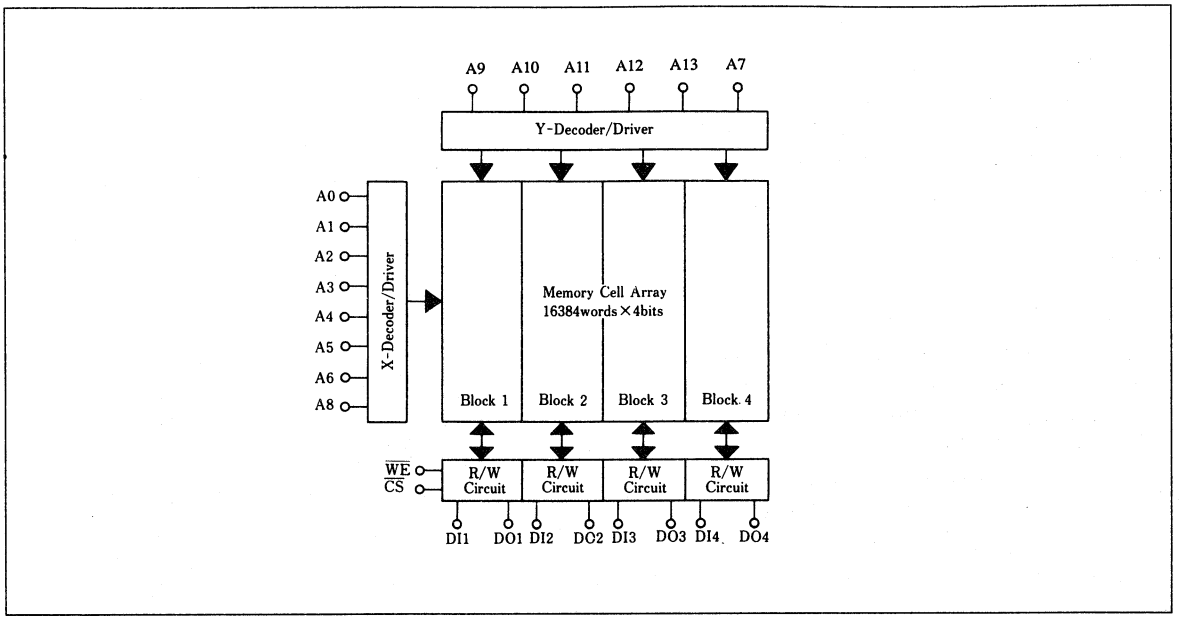


(Top View)

Pin Description

Pin name	Function
A0 – A13	Address input
DI1 – DI4	Data input
DO1 – DO4	Data output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}/V_{CCA}	Ground
V_{EE}	Supply voltage

Block Diagram



Function Table

Input

$\overline{CS}$	$\overline{WE}$	Din	Output	Mode
H	X*1	X*1	L	Not selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X*1	Dout*2	Read

Notes: 1. Irrelevant
2. Read out noninvert

Absolute Maximum Ratings (Tj = 125°C max*1, Ta = 25°C*2)

Item	Symbol	SOJ Rating	Cerdip, ceramic flat Rating	Unit
Supply voltage	V_{EE} to V_{CC}	+0.5 to –7.0	+0.5 to –7.0	V
Input voltage	Vin	+0.5 to V_{EE}	+0.5 to V_{EE}	V
Output current	Iout	–30	–30	mA
Power dissipation	P_T	1.0	—	W
Operating temperature	Topr	0 to + 85*4	—	°C
Storage temperature	Tstg	–55 to +125	–65 to +150	°C
Storage temperature	Tstg (Bias)*3	–10 to +85*4	–55 to +125	°C

Notes: 1. SOJ
2. Cerdip, ceramic flat
3. Under bias (V_{EE} = –6 Vmin)
4. Case temperature; Tc

DC Characteristics (V_{EE} = –4.5 V*1, V_{EE} = –5.2 V*2, R_L = 50Ω to –2.0 V, Tc = 0 to +85°C*1, *3, Tc = 0 to +75°C*2, *3, Ta = 0 to +75°C*2, *4 air flow exceeding 2 m/sec)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test conditions
Output voltage	V_{OH}	–1025	–955	–880	mV	Vin = V_{IHA} or V_{ILB}
	V_{OL}	–1810	–1715	–1620	mV	
Output threshold voltage	V_{OHC}	–1035	—	—	mV	Vin = V_{IHB} or V_{ILA}
	V_{OLC}	—	—	–1610	mV	
Input voltage	V_{IH}	–1165	—	–880	mV	Guaranteed input voltage High/low for all inputs
	V_{IL}	–1810	—	–1475	mV	
Input current	I_{IH}	—	—	220	µA	Vin = V_{IHA}
	I_{IL}	0.5	—	170	µA	$\overline{CS}$ Vin = V_{ILB}
		–50	—	—	µA	Others
Supply current (8 ns)	I_{EE}	–220	—	—	mA	All inputs and outputs open
Supply current (10/12 ns)	I_{EE}	–200	—	—	mA	All inputs and outputs open

Notes: 1. 100K type
2. 101K type
3. SOJ, Ceramic flat
4. Cerdip

AC Characteristics

(V_{EE} = –4.5 V ± 5%*1, V_{EE} = –5.2 V ± 5%*2, Tc = 0 to +85°C*1, *3, Tc = 0 to +75°C*2, *3, Ta = 0 to +75°C*2, *4 air flow exceeding 2 m/sec)

Read Mode

		HM101494-8			HM100494-10/12 HM101494-10/12				
Item	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test conditions
Chip select access time	t_{ACS}	—	—	6	—	—	6/8	ns	
Chip select recovery time	t_{RCS}	—	—	6	—	—	6/8	ns	
Address access time	t_{AA}	—	—	8	—	—	10/12	ns	

Write Mode

		HM101494-8			HM100494-10/12 HM101494-10/12				
Item	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test conditions
Write pulse width	t_W	5	—	—	6/8	—	—	ns	$t_{WSA} = t_{WSA}$ min
Data setup time	t_{WSD}	1	—	—	2/2	—	—	ns	
Data hold time	t_{WHD}	2	—	—	2/2	—	—	ns	
Address setup time	t_{WSA}	1	—	—	2/2	—	—	ns	$t_W = t_W$ min
Address hold time	t_{WHA}	2	—	—	2/2	—	—	ns	
Chip select setup time	t_{WSCS}	1	—	—	2/2	—	—	ns	
Chip select hold time	t_{WHCS}	2	—	—	2/2	—	—	ns	
Write disable time	t_{WS}	—	—	6	—	—	6/8	ns	
Write recovery time	t_{WR}	—	—	10	—	—	12/14	ns	

Rise/Fall Time

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Output rise time	t_r	—	2	—	ns	
Output fall time	t_f	—	2	—	ns	

Notes: 1. 100K type
2. 101K type
3. SOJ, Cramic flat
4. Cerdip

Capacitance (SOJ)

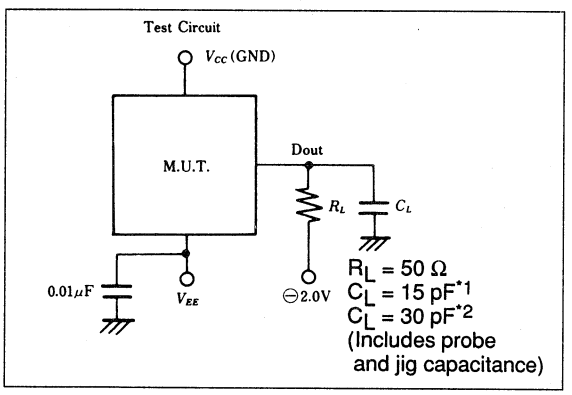
Item	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance	Cin	—	3	—	pF	$\overline{WE}$
		—	2	—	pF	Others
Output capacitance	Cout	—	3	—	pF	

Capacitance (Cerdip, Ceramic Flat)

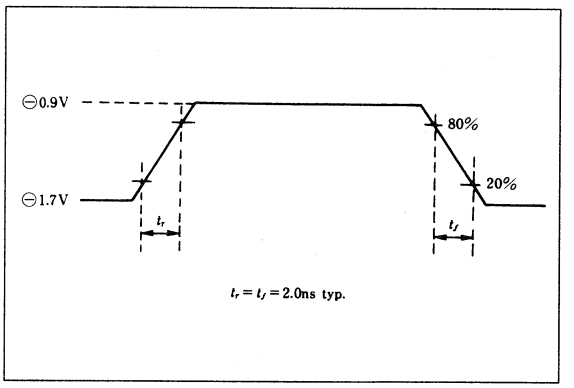
Item	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance	Cin	—	5	—	pF	$\overline{WE}$, $\overline{CS}$, DI1, DI2
		—	3	—	pF	Others
Output capacitance	Cout	—	3	—	pF	

Test Circuit and Waveforms

Loading Condition

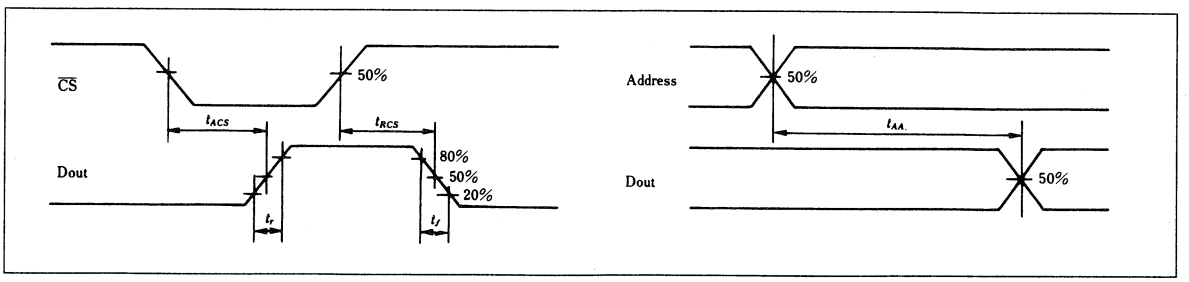


Input Pulse

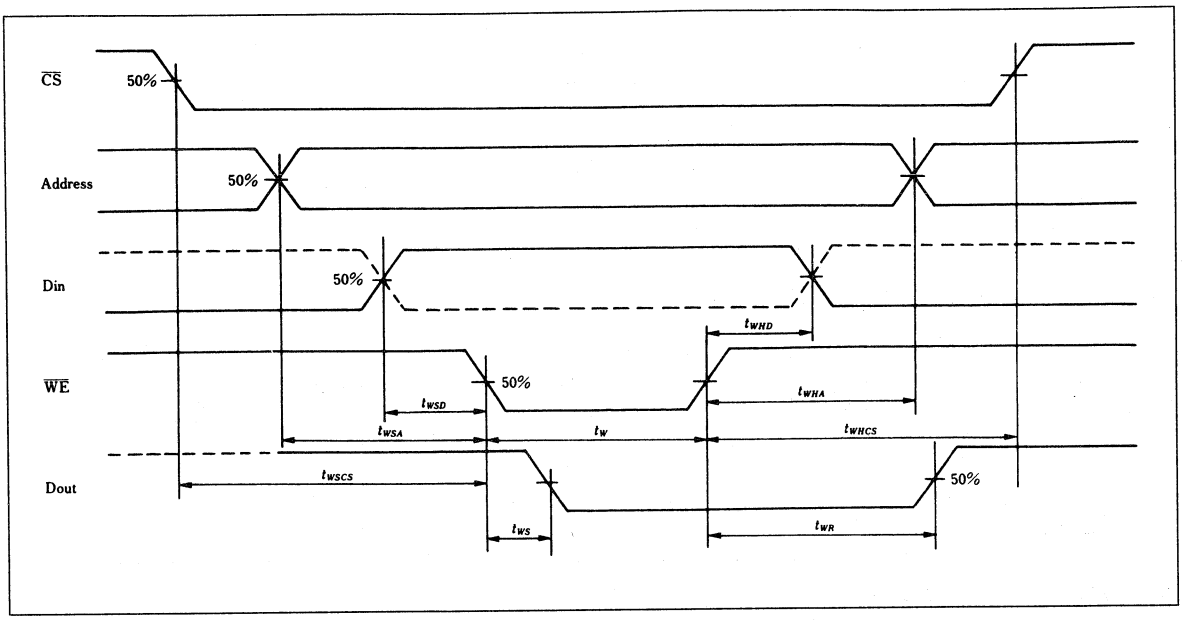


Notes: 1. 8 ns
2. 10/12 ns

Read Mode



Write Mode


CS
Address
Din
WE
Dout
50%
50%
50%
50%
50%
tWHD
tWSD
tWSA
tW
tWHA
tWHCS
tWSCS
tWS
tWR

HM101490 Series

65536-Word × 1-Bit Fully Decoded Random Access Memory

The HM101490 is ECL 100K compatible, 65536-word by 1-bit read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

Features

- 65536 × 1-bit organization
- Fully compatible with 100K ECL level
- Address access time: 10/12 ns (max)
- Write pulse width: 6/8 ns (min)
- Low power dissipation: 570 mV (typ)
- Output obtainable by wired-OR (open emitter)

Ordering Information

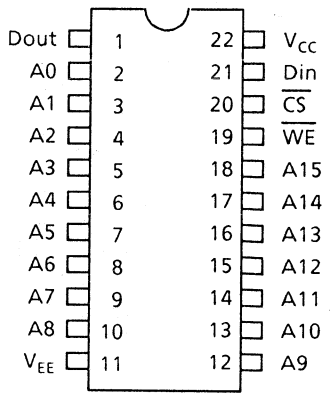
Type No.	Access time	Package
HM101490JP-10	10 ns	300-mil 24-pin plastic SOJ (CP-24D)
HM101490JP-12	12 ns	
HM101490-10	10 ns	300-mil 22-pin cerdip (DG-22N)
HM101490-12	12 ns	

Pin Description

Pin name	Function
A0 – A15	Address input
Din	Data input
Dout	Data output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Ground
V_{EE}	Supply voltage

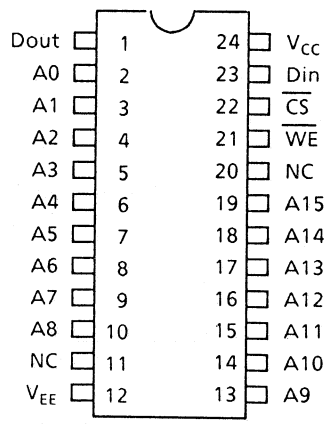
Pin Arrangement

HM101490 Series



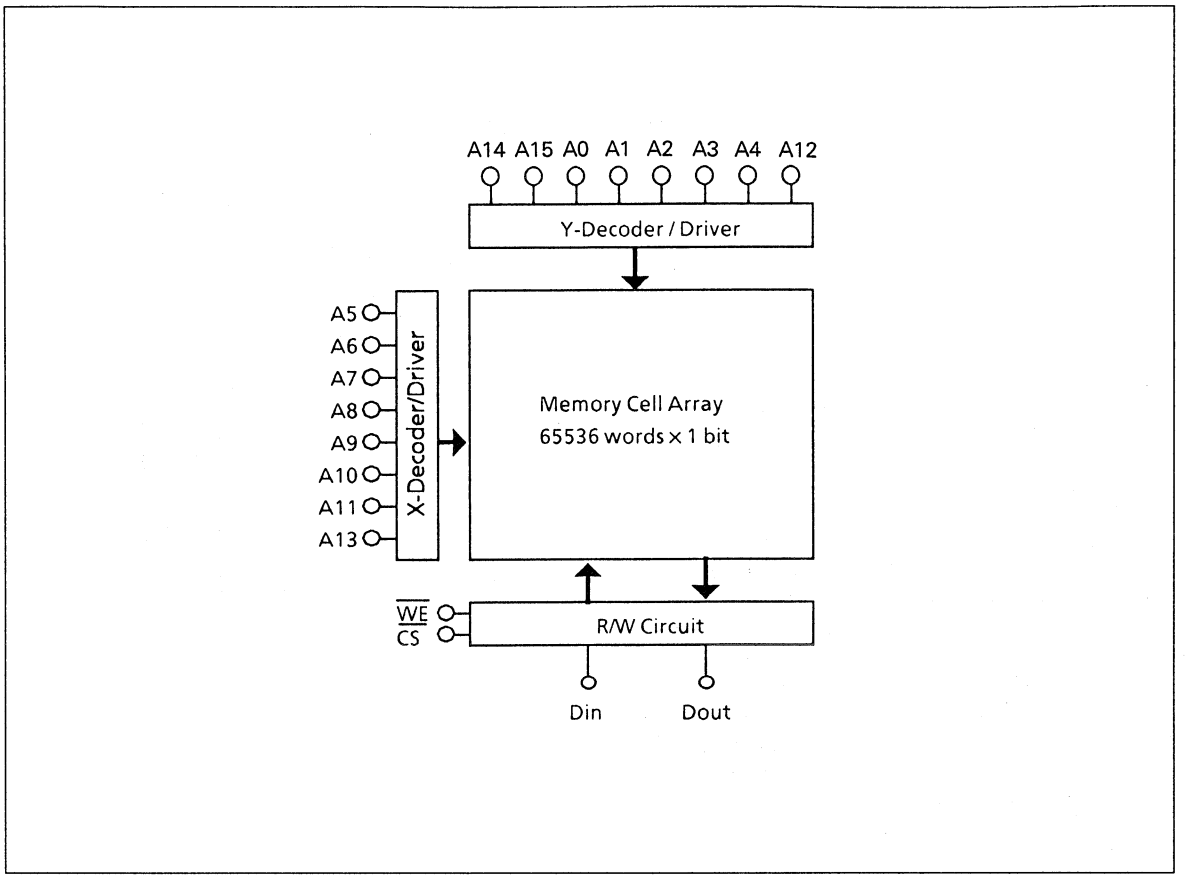
(Top View)

HM101490JP Series



(Top View)

Block Diagram



Function Table

Input

$\overline{CS}$	$\overline{WE}$	Din	Output	Mode
H	×*1	×*1	L	Not selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×*1	Dout*2	Read

Notes: 1. Irrelevant
2. Read out noninvert

Absolute Maximum Ratings (Tj = 125°C max[*1], Ta = 25°C[*2])

Item	Symbol	SOJ Rating	Cerdip Rating	Unit
Supply voltage	V_{EE} to V_{CC}	+0.5 to –7.0	+0.5 to –7.0	V
Input voltage	Vin	+0.5 to V_{EE}	+0.5 to V_{EE}	V
Output current	Iout	–30	–30	mA
Power dissipation	P_T	1.0	—	W
Operating temperature	Topr	0 to +85[*4]	—	°C
Storage temperature	Tstg	–55 to +125	–65 to +150	°C
Storage temperature	Tstg (Bias)[*3]	–10 to +85[*4]	–55 to +125	°C

Note: 1. SOJ
2. Cerdip
3. Under Bias (V_{EE} = –6 V min)
4. Case temperature : Tc

DC Characteristics (V_{EE} = –5.2 V, R_L = 50 Ω to –2.0 V, Tc = 0 to +75°C[*1], Ta = 0 to +75°C[*2] air flow exceeding 2 m/sec)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test conditions	
Output voltage	V_{OH}	–1025	–955	–880	mV	Vin = V_{IHA} or V_{ILB}	
	V_{OL}	–1810	–1715	–1620	mV		
Output threshold voltage	V_{OHC}	–1035	—	—	mV	Vin = V_{IHB} or V_{ILA}	
	V_{OLC}	—	—	–1610	mV		
Input voltage	V_{IH}	–1165	—	–880	mV	Guaranteed input voltage High/low for all inputs	
	V_{IL}	–1810	—	–1475	mV		
Input current	I_{IH}	—	—	220	µA	Vin = V_{IHA}	
	I_{IL}	0.5	—	170	µA	Vin = V_{ILB}	$\overline{CS}$
		–50	—	—	µA		Others
Supply current	I_{EE}	–180	—	—	mA	All inputs and outputs open	

Notes: 1. SOJ
2. Cerdip

AC Characteristics (V_{EE} = –5.2 V ± 5%, Tc = 0 to +75°C*1, Ta = 0 to +75°C*2 air flow exceeding 2 m/sec)

Read Mode

Item	Symbol	HM101490-10 Min	HM101490-10 Typ	HM101490-10 Max	HM101490-12 Min	HM101490-12 Typ	HM101490-12 Max	Unit	Test conditions
Chip select access time	t_{ACS}	—	—	6	—	—	8	ns	
Chip select recovery time	t_{RCS}	—	—	6	—	—	8	ns	
Address access time	t_{AA}	—	—	10	—	—	12	ns	

Write Mode

Item	Symbol	HM101490-10 Min	HM101490-10 Typ	HM101490-10 Max	HM101490-12 Min	HM101490-12 Typ	HM101490-12 Max	Unit	Test conditions
Write pulse width	t_W	6	—	—	8	—	—	ns	$t_{WSA} = t_{WSA}$ min
Data setup time	t_{WSD}	2	—	—	2	—	—	ns	
Data hold time	t_{WHD}	2	—	—	2	—	—	ns	
Address setup time	t_{WSA}	2	—	—	2	—	—	ns	$t_W = t_W$ min
Address hold time	t_{WHA}	2	—	—	2	—	—	ns	
Chip select setup time	t_{WSCS}	2	—	—	2	—	—	ns	
Chip select hold time	W_{HCS}	2	—	—	2	—	—	ns	
Write disable time	t_{WS}	—	—	6	—	—	8	ns	
Write recovery time	t_{WR}	—	—	12	—	—	14	ns	

Notes: 1. SOJ
2. Cerdip

Rise/Fall Time

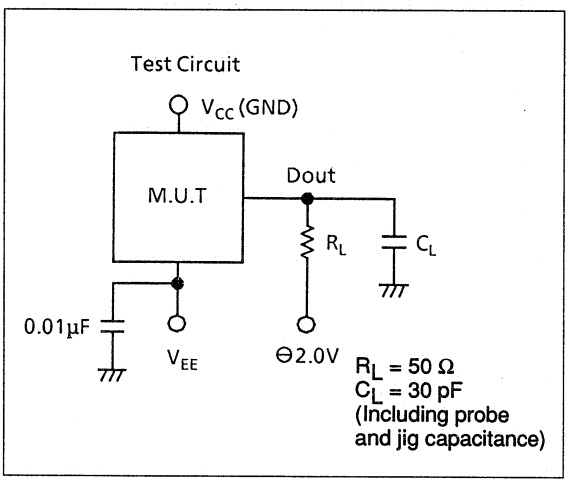
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Output rise time	t_r	—	2	—	ns	
Output fall time	t_f	—	2	—	ns	

Capacitance

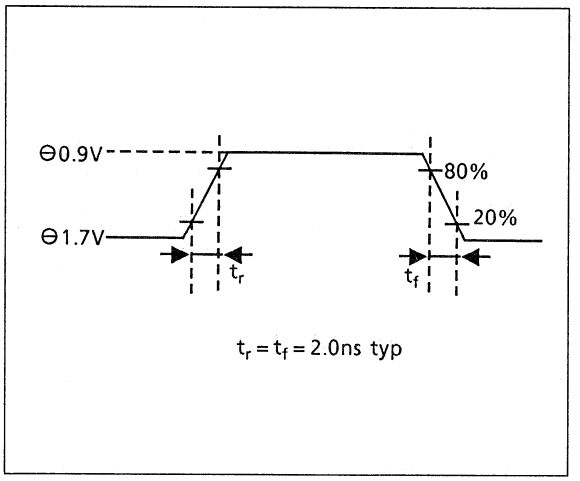
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	3	—	pF	
Output capacitance	Cout	—	5	—	pF	

Test Circuit and Waveforms

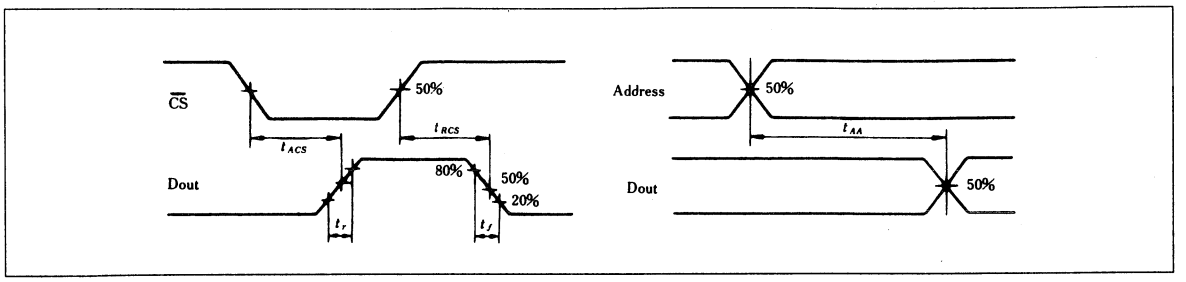
Loading Condition



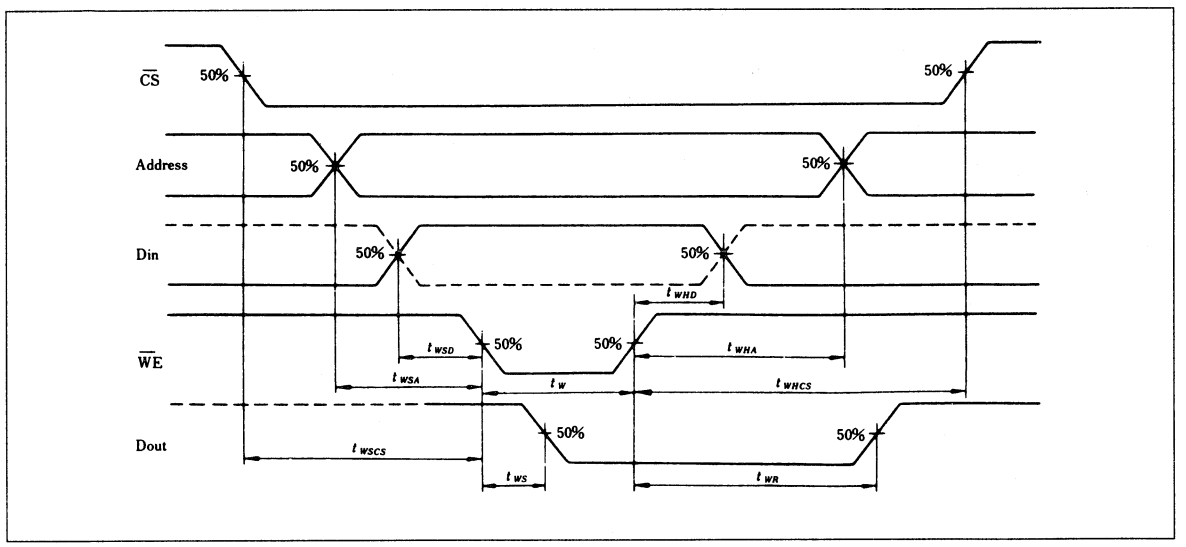
Input Pulse



Read Mode



Write Mode



HM100504/HM101504 Series

65536-Word × 4-Bit Random Access Memory

The HM100504/HM101504 are ECL 100K compatible, 65536-words by 4-bits read/write random access memory developed for high speed systems such as cache and control/buffer storage.

Features

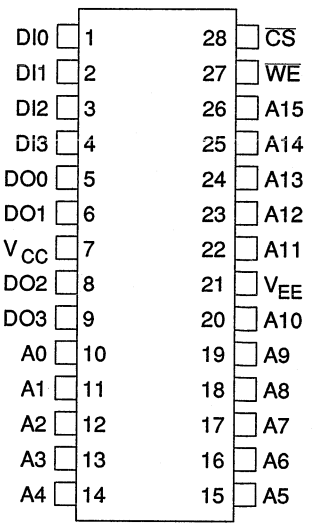
- 65536-word × 4-bit organization
- Fully compatible with 100K ECL level
- 0.8 µm Hi-BiCMOS process
- Address access time: 10/12 ns (max)
- Write pulse width: 8/10 ns (min)
- Low power dissipation: 100K: 650 mW (typ)
  101K: 750 mW (typ)
- Output obtainable by wired-OR (open emitter)

Ordering Information

Type No.	Access time	Package
HM100504JP-10	10 ns	400-mil 32-pin plastic SOJ (CP-32D)
HM100504JP-12	12 ns	
HM101504JP-10	10 ns	
HM101504JP-12	12 ns	
HM100504F-10	10 ns	28-pin ceramic flat (30 mil lead pitch) (FG-28DA)
HM100504F-12	12 ns	
HM101504F-10	10 ns	
HM101504F-12	12 ns	

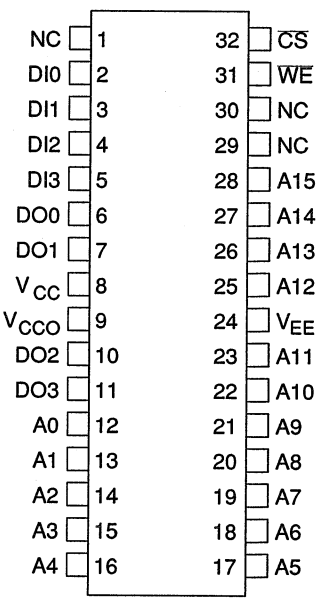
Pin Arrangement

HM100504F/HM101504F Series



(Top View)

HM100504JP/HM101504JP Series

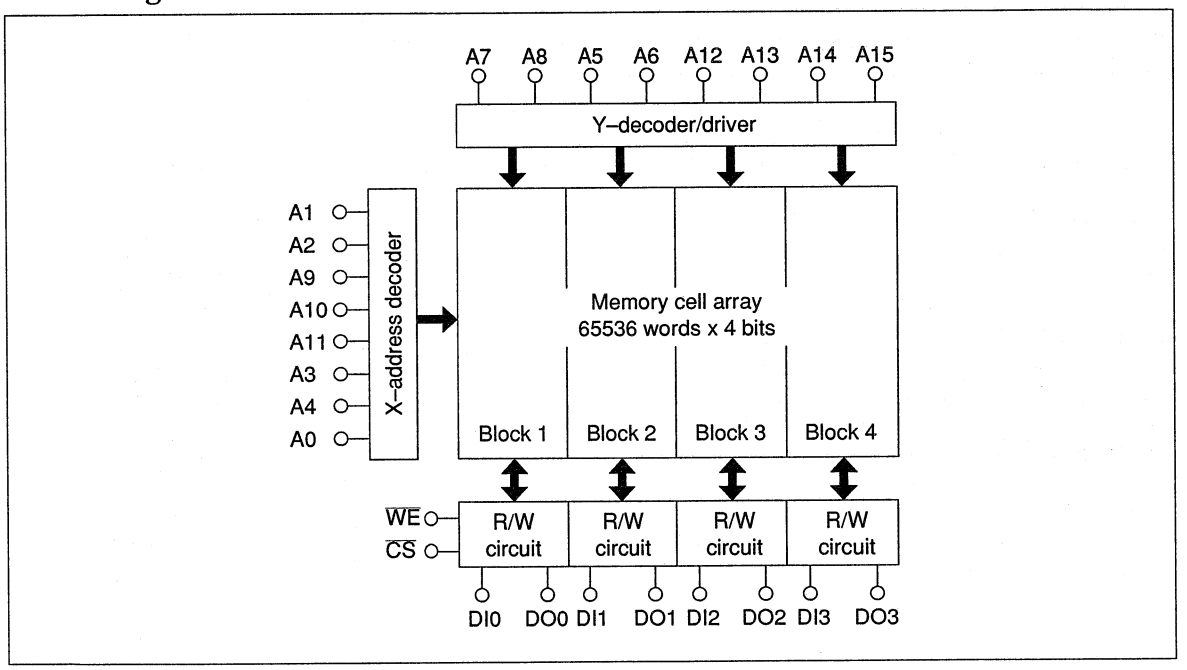


(Top View)

Pin Description

Pin name	Function
A0 – A15	Address input
DI0 – DI3	Data input
DO0 – DO3	Data output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Ground
V_{EE}	Supply voltage

Block Diagram



Function Table

Input				
$\overline{CS}$	$\overline{WE}$	Din	Output	Mode
H	× *1	× *1	L	Not selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	× *1	Dout *2	Read

Notes: 1. Irrelevant
2. Read out noninvert

Absolute Maximum Rating (Tj = 125°C max*1, Ta = 25°C*2)

Item	Symbol	SOJ Rating	Ceramic flat Rating	Unit
Supply voltage	V_{EE} to V_{CC}	+0.5 to –7.0	+0.5 to –7.0	V
Input voltage	Vin	+0.5 to V_{EE}	+0.5 to V_{EE}	V
Output current	Iout	–30	–30	mA
Power dissipation	PT	1.2	—	W
Operating temperature	Topr	0 to +85*4	—	°C
Storage temperature	Tstg	–55 to + 125	–65 to + 150	°C
Storage temperature	Tstg (Bias) *3	–10 to + 85*4	–55 to + 125	°C

Notes: 1. SOJ
2. Ceramic flat
3. Under bias (VEE = –6 V min)
4. Case temperature

DC Characteristics (V_{EE} = –4.5 V*1, V_{EE} = –5.2 V*2, R_L = 50Ω to –2.0 V, Tc = 0 to +85°C*1, Tc = 0 to +75°C*2)

Item	Symbol	Min(B)	Typ	Max(A)	Unit	Test condition	
Output voltage	V_{OH}	–1025	–955	–880	mV	Vin = V_{IHA} or V_{ILB}	
	V_{OL}	–1810	–1715	–1620	mV		
Output threshold voltage	V_{OHC}	–1035	—	—	mV	Vin = V_{IHB} or V_{ILA}	
	V_{OLC}	—	—	–1610	mV		
Input voltage	V_{IH}	–1165	—	–880	mV	Guaranteed input voltage High/low for all inputs	
	V_{IL}	–1810	—	–1475	mV		
Input current	I_{IH}	—	—	220	µA	Vin = V_{IHA}	
	I_{IL}	0.5	—	170	µA	Vin = V_{ILB}	$\overline{CS}$
		–50	—	—	µA		Others
Supply current	I_{EE}	–200	—	—	mA	All inputs and outputs open	

AC Characteristics (V_{EE} = –4.5 V ± 5%*1, V_{EE} = –5.2 V ± 5%*2, Tc = 0 to +85°C*1, Tc = 0 to +75°C*2)

Read Mode

		HM101504-10 HM100504-10			HM101504-12 HM100504-12				
Item	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test condition
Chip select access time	t_{ACS}	—	—	6	—	—	7	ns	
Chip select recovery time	t_{RCS}	—	—	6	—	—	7	ns	
Address access time	t_{AA}	—	—	10	—	—	12	ns	

Notes: 1. 100K type
2. 101K type

Write Mode

Item	Symbol	HM101504-10 HM100504-10 Min	Typ	Max	HM101504-12 HM100504-12 Min	Typ	Max	Unit	Test condition
Write pulse width	t_W	8	—	—	10	—	—	ns	$t_{WSA} = t_{WSA}$ min
Data setup time	t_{WSD}	0	—	—	0	—	—	ns	
Data hold time	t_{WHD}	2	—	—	2	—	—	ns	
Address setup time	t_{WSA}	0	—	—	0	—	—	ns	$t_W = t_W$ min
Address hold time	t_{WHA}	2	—	—	2	—	—	ns	
Chip select setup time	t_{WSCS}	0	—	—	0	—	—	ns	
Chip select hold time	t_{WHCS}	2	—	—	2	—	—	ns	
Write disable time	t_{WS}	—	—	6	—	—	7	ns	
Write recovery time	t_{WR}	—	—	12	—	—	14	ns	

Rise/Fall Time

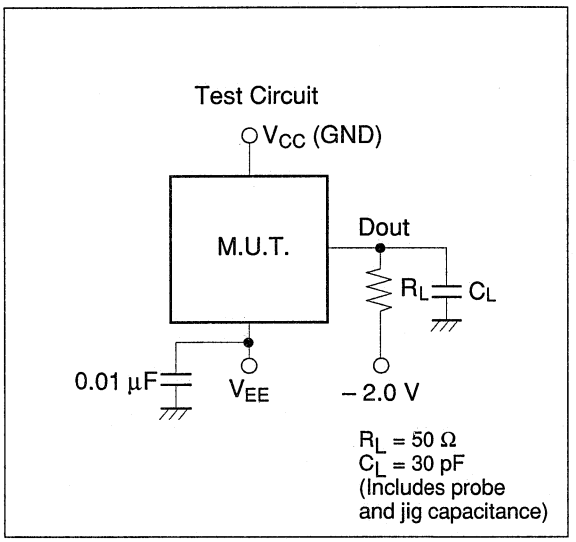
Item	Symbol	Min	Typ	Max	Unit	Test condition
Output rise time	t_r	—	2	—	ns	
Output fall time	t_f	—	2	—	ns	

Capacitance

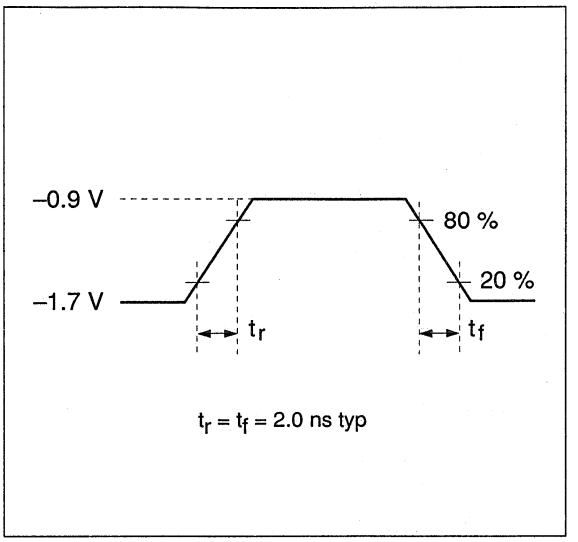
Item	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance	Cin	—	3	—	pF	
Output capacitance	Cout	—	5	—	pF	

Test Circuit and Waveforms

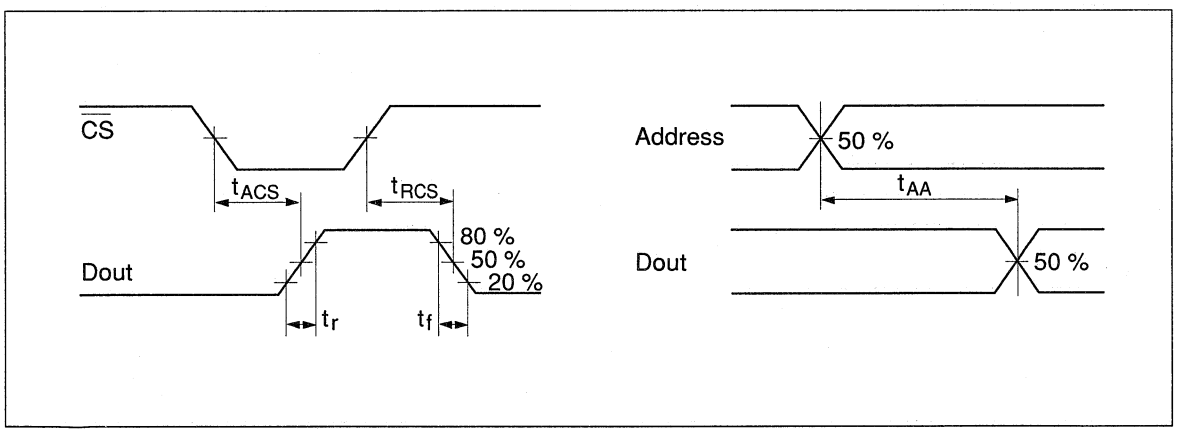
Test Condition



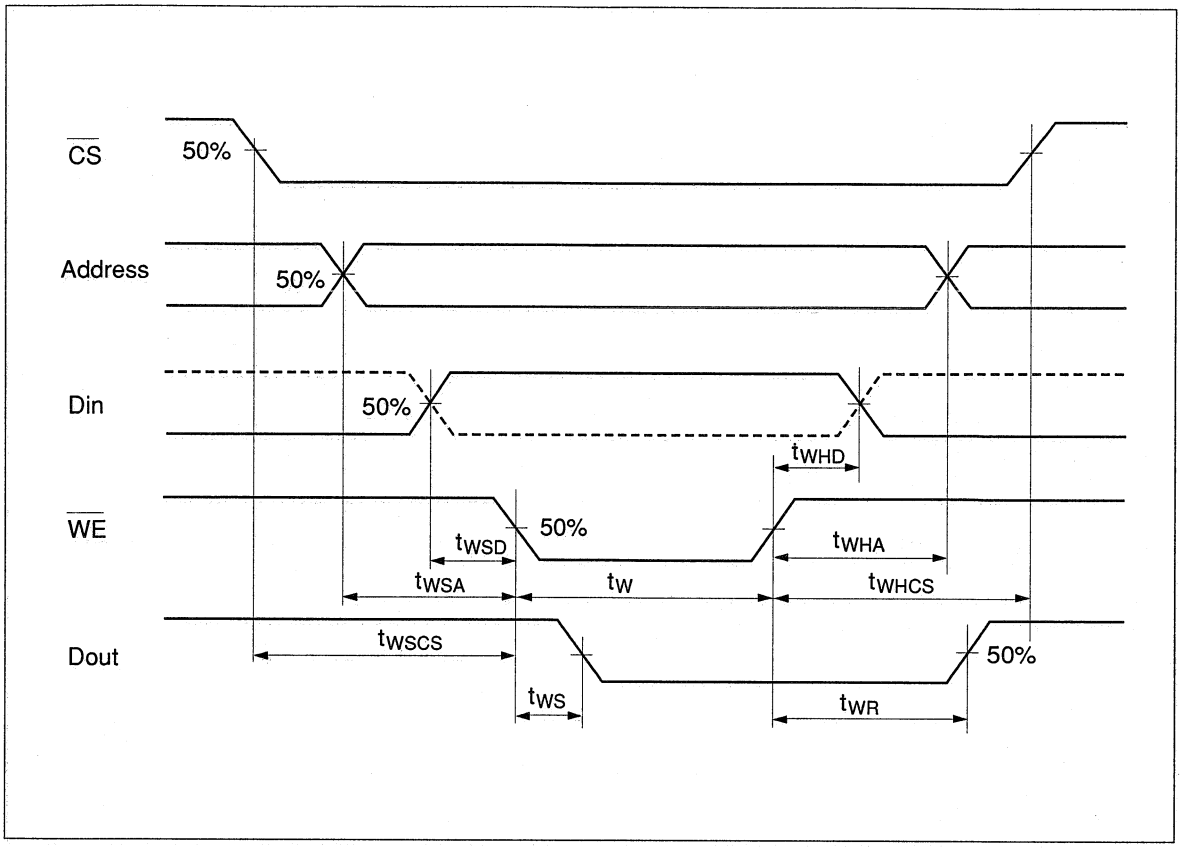
Input Pulse



Read Mode



Write Mode


CS
Address
Din
WE
Dout
50%
50%
50%
50%
50%
tWHD
tWSD
tWSA
tW
tWHA
tWHCS
tWSCS
tWS
tWR

HM100500/HM101500 Series

262144-Word × 1-Bit Fully Decoded Random Access Memory

The HM100500/HM101500 are ECL 100K compatible, 262144-word × 1-bit read/write random access memory developed for high speed systems such as main memories for super computers.

Features

- 262144-word × 1-bit organization
- Fully compatible with 100K ECL level
- Address access time: 15/18 ns (max)
- Write pulse width: 10 ns (min)
- Low power dissipation: 500 mV (typ)
- Output obtainable by wired-OR (open emitter)

Ordering Information

Type No.	Access time	Package
HM100500CG-18	18 ns	28-pin LCC (CG-28B)
HM100500-18	18 ns	24-pin DIP (DG-24V)
HM100500F-18	18 ns	24-pin FPG (FG-24A)
HM101500-15	15 ns	24-pin DIP (DG-24V)
HM101500F-15	15 ns	24-pin FPG (FG-24A)

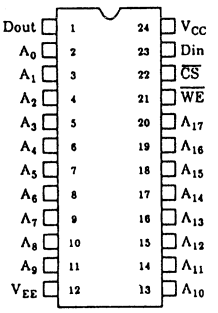
Function Table

Input				
$\overline{CS}$	$\overline{WE}$	Din	Output	Mode
H	×	×	L	Not selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*1	Read

Notes: ×; Irrelevant *1; Read out noninvert

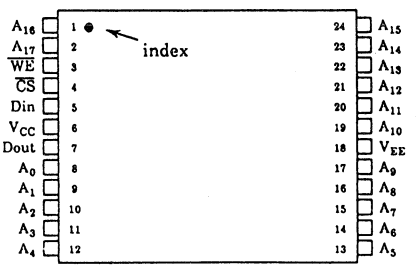
Pin Arrangement

DG-24V



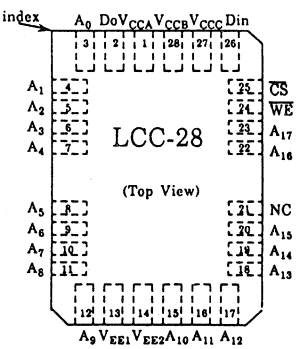
(Top View)

FG-24A



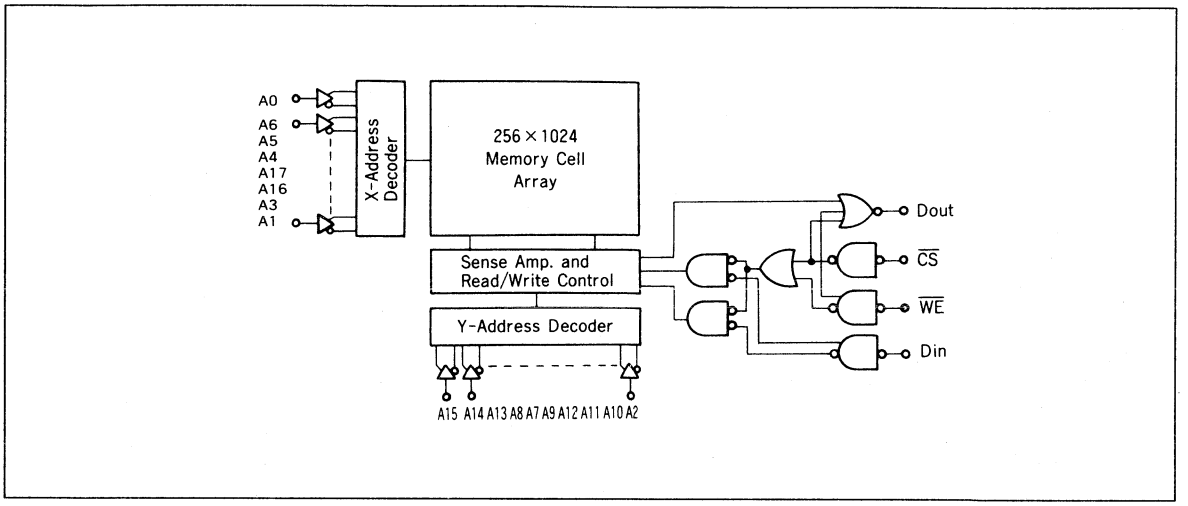
(Top View)

CG-28B



(Top View)

Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply voltage	V_{EE} to V_{CC}	+0.5 to –7.0	V
Input voltage	Vin	+0.5 to V_{EE}	V
Output current	Iout	–30	mA
Storage temperature	Tstg	–65 to +150	°C
Storage temperature	Tstg (Bias)*1	–55 to +125	°C

Note: *1; Under bias (V_{EE} = –6 V min)

DC Characteristics

(V_{EE} = –4.5V*1, V_{EE} = –5.2 V*2, R_L = 50 Ω to –2.0 V, Tc = 0 to +85°C*1, *3, Tc = 0 to +75°C*2, *3, Ta = 0 to +85°C*1, *4, Ta = 0 to +75°C*2, *4 air flow exceeding 2 m/sec)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test conditions
Output voltage	V_{OH}	–1025	–955	–880	mV	Vin = V_{IHA} or V_{ILB}
	V_{OL}	–1810	–1715	–1620	mV	
Output threshold voltage	V_{OHC}	–1035	—	—	mV	Vin = V_{IHB} or V_{ILA}
	V_{OLC}	—	—	–1610	mV	
Input voltage	V_{IH}	–1165	—	–880	mV	Guaranteed input voltage high/low for all inputs
	V_{IL}	–1810	—	–1475	mV	
Input current	I_{IH}	—	—	220	µA	Vin = V_{IHA}
	I_{IL}	0.5	—	170	µA	Vin = V_{ILB} $\overline{CS}$
		–50	—	—		Others
Supply current	I_{EE}	–160*1 –200*2	—	—	mA	All inputs and outputs open

Notes
1. 100 K type
2. 101 K type
3. Ceramic flat, LCC
4. Cerdip

AC Characteristics

(V_{EE} = –4.5V ± 5%*1, V_{EE} = –5.2 V ± 5%*2, Tc = 0 to +85°C*1, *3, Tc = 0 to +75°C*2, *3, Ta = 0 to +85°C*1, *4, Ta = 0 to +75°C*2, *4 air flow exceeing 2 m/sec)

Read Mode

		HM100500			HM101500				
Item	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test conditions
Chip select access time	t_{ACS}	—	—	18*5	—	—	15	ns	
		—	—	15*6					
Chip select recovery time	t_{RCS}	—	—	18*5	—	—	10	ns	
		—	—	10*6					
Address access time	t_{AA}	—	—	18	—	—	15	ns	

Write Mode

Item	Symbol	HM100500 Min	HM100500 Typ	HM100500 Max	HM101500 Min	HM101500 Typ	HM101500 Max	Unit	Test conditions
Write pulse width	t_W	10	—	—	10	—	—	ns	t_{WSA} = 2 ns
Data setup time	t_{WSD}	2	—	—	2	—	—	ns	
Data hold time	t_{WHD}	3	—	—	3	—	—	ns	
Address setup time	t_{WSA}	2	—	—	2	—	—	ns	t_W = 10 ns
Address hold time	t_{WHA}	3	—	—	3	—	—	ns	
Chip select setup	t_{WSCS}	2	—	—	2	—	—	ns	
Chip select hold time	t_{WHCS}	3	—	—	3	—	—	ns	
Write disable time	t_{WS}	—	—	15*5	—	—	10	ns	
		—	—	10*6					
Write recovery time	t_{WR}	—	—	21	—	—	18	ns	

Notes
1. 100 K type
2. 101 K type
3. Ceramic flat, LCC
4. Cerdip
5. HM100500CG
6. HM100500/F

Rise/Fall Time

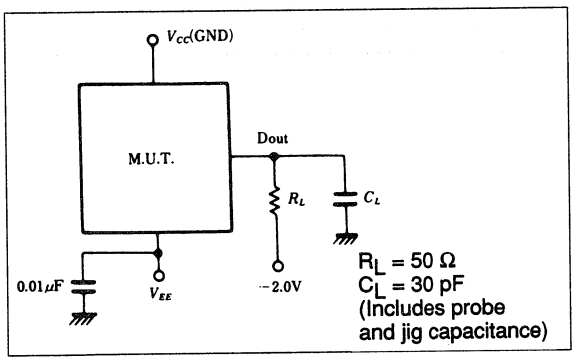
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Output rise time	t_r	—	2	—	ns	
Output fall time	t_f	—	2	—	ns	

Capacitance

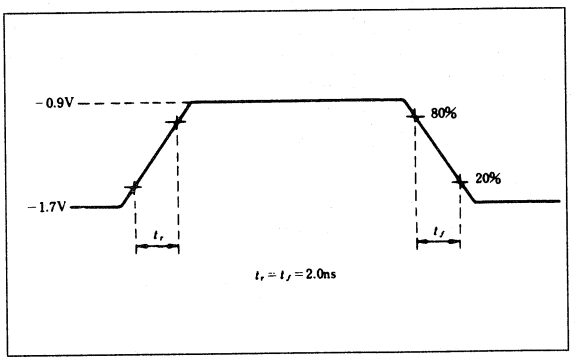
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	3	—	pF	
Output capacitance	Cout	—	5	—	pF	

Test Circuit and Waveforms

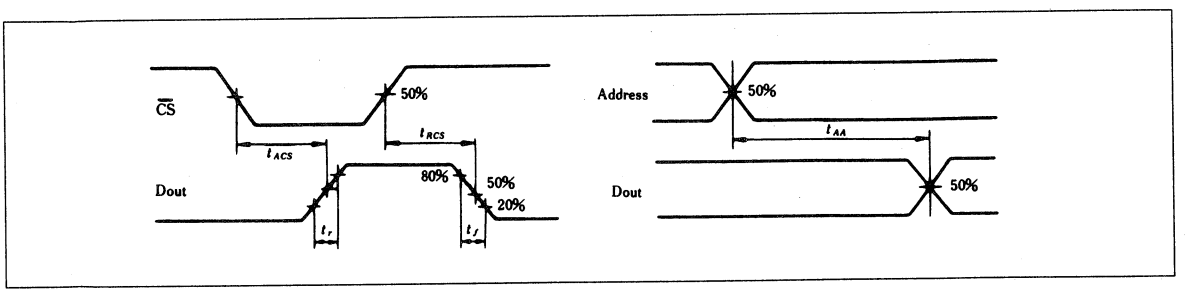
Loading Condition



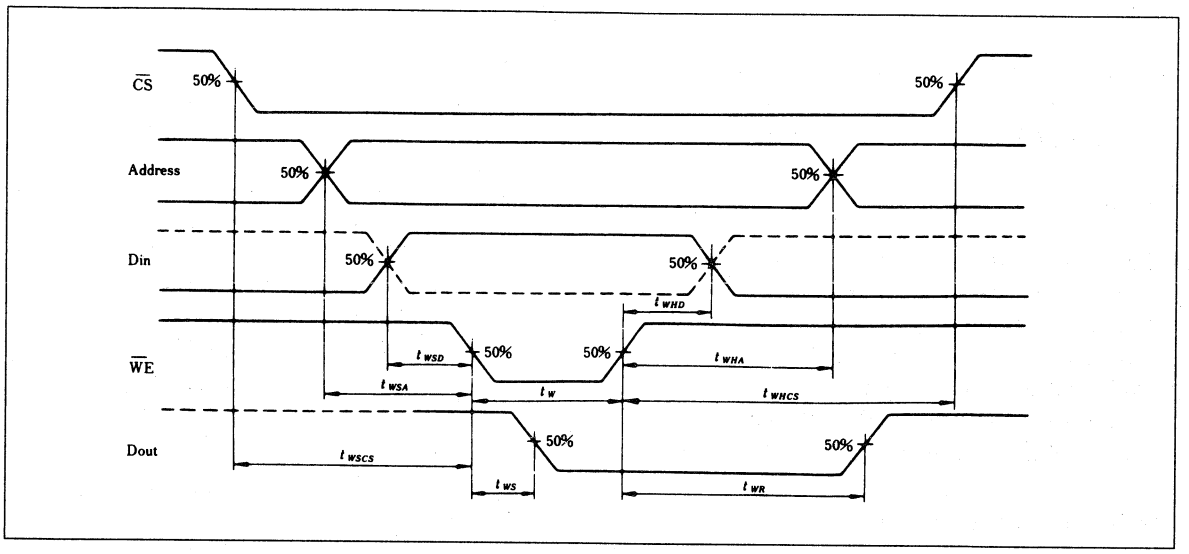
Input Pulse



Read Mode



Write Mode


$\overline{CS}$
Address
Din
$\overline{WE}$
Dout
50%
t_{WSD}
t_{WSA}
t_{WSCS}
t_{WS}
t_{WHD}
t_{WHA}
t_{W}
t_{WHCS}
t_{WR}

HM101514 Series — Preliminary

262,144-word × 4-bit Random Access Memory

The Hitachi HM101514 is ECL 100 K compatible, 262,144 words by 4 bits read/write random access memory developed for high speed systems.

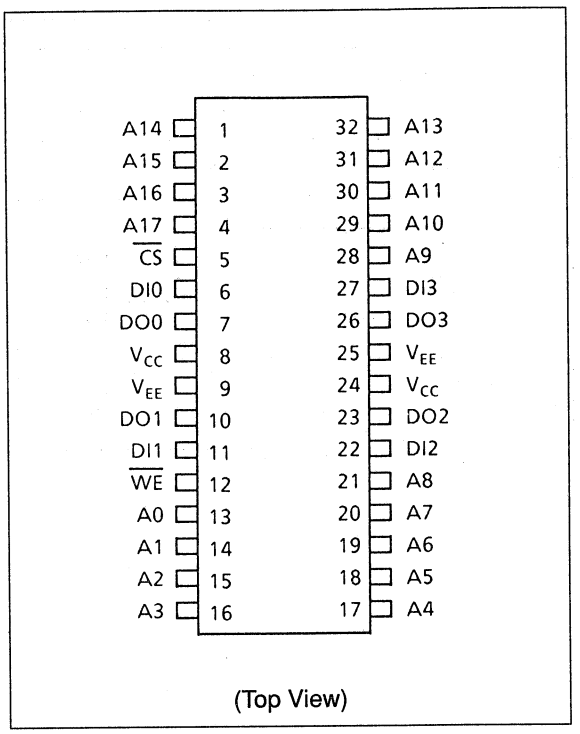
Features

- 262,144-words × 4 bit organization
- Fully compatible with 100 K ECL level
- 0.8 µm Hi-BiCMOS process
- Address access time: 15 ns max
- Write pulse width: 9 ns min
- Low power dissipation: 800 mW typ
- Output obtainable by wired-OR (open emitter)

Ordering Information

Type No.	Access time	Package
HM101514F-15	15 ns	32-pin ceramic flat (30 mil lead pitch) (FG-32D)
HM101514JP-15	15 ns	400-mil 32-pin plastic SOJ (CP-32D)

Pin Arrangement



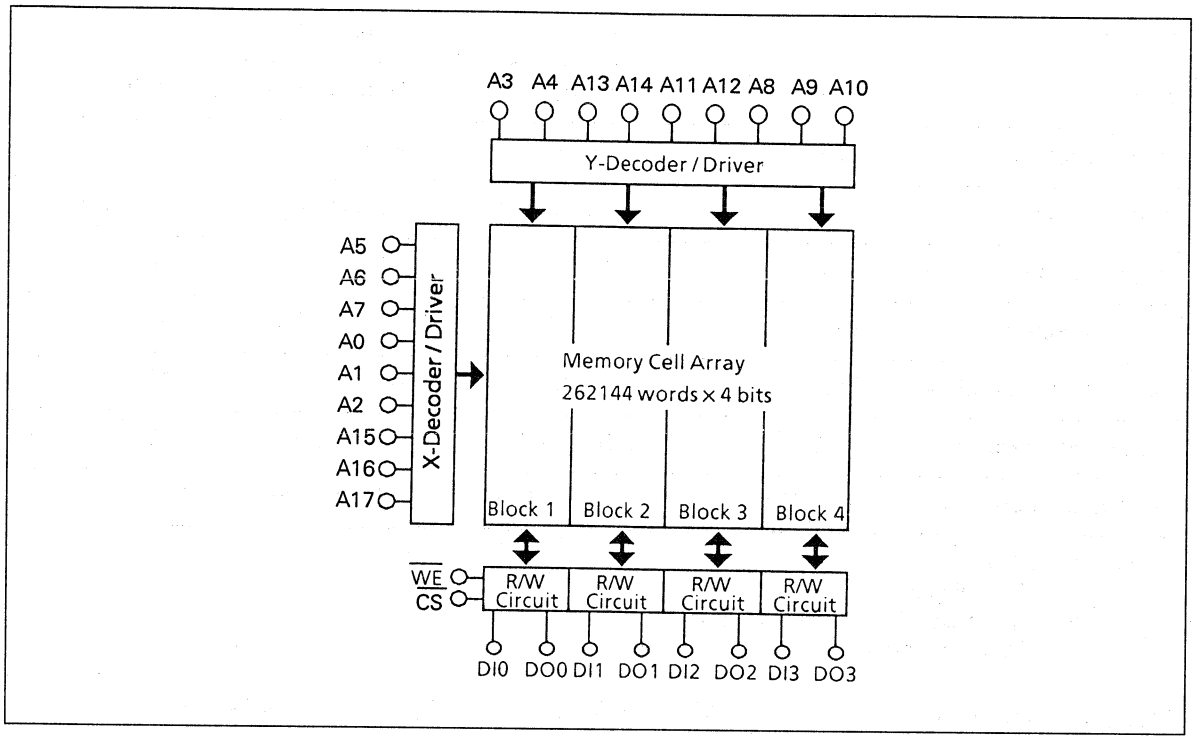
(Top View)

Pin Description

Pin name	Function
A0 – A17	Address input
DI0 – DI3	Data input
DO0 – DO3	Data output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Ground
V_{EE}	Supply voltage

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Block Diagram



Function Table

Input

$\overline{CS}$	$\overline{WE}$	Din	Output	Mode
H	X*1	X*1	L	Not selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X*1	Dout*2	Read

Notes: 1. Irrelevant.
2. Read out noninvert.

Absolute Maximum Rating (Tj = 125°C max*1, Ta = 25°C*2)

Item	Symbol	SOJ Rating	Ceramic flat Rating	Unit
Supply voltage	V_{EE} to V_{CC}	+0.5 to –7.0	+0.5 to –7.0	V
Input voltage	Vin	+0.5 to V_{EE}	+0.5 to V_{EE}	V
Output current	Iout	–30	–30	mA
Power dissipation	P_T	1.2	—	W
Operating temperature	Topr	0 to +85*4	—	°C
Storage temperature	Tstg	–55 to +125	–65 to +150	°C
Storage temperature	Tstg (Bias)*3	–10 to +85*4	–55 to +125	°C

Notes: 1. SOJ
2. Ceramic flat
3. Under bias (V_{EE} = –6.0 V min)
4. Case temperature

DC Characteristics (V_{EE} = –5.2 V, R_L = 50 Ω to –2.0 V, Tc = 0 to +75°C)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test condition	
Output voltage	V_{OH}	–1025	–955	–880	mV	Vin = V_{IHA} or V_{ILB}	
	V_{OL}	–1810	–1715	–1620	mV		
Output threshold voltage	V_{OHC}	–1035	—	—	mV	Vin = V_{IHB} or V_{ILA}	
	V_{OLC}	—	—	–1610	mV		
Input voltage	V_{IH}	–1165	—	–880	mV	Guaranteed input voltage High/low for all inputs	
	V_{IL}	–1810	—	–1475	mV		
Input current	I_{IH}	—	—	220	µA	Vin = V_{IHA}	
	I_{IL}	0.5	—	170	µA	Vin = V_{ILB}	$\overline{CS}$
		–50	—	—	µA		Others
Supply current	I_{EE}	–200	—	—	mA	All outputs open	

AC Characteristics (V_{EE} = –5.2 V ± 5%, Tc = 0 to +75°C)

Read Mode

Item	Symbol	Min	Typ	Max	Unit	Test condition
Chip select access time	t_{ACS}	—	—	10	ns	
Chip select recovery time	t_{RCS}	—	—	10	ns	
Address access time	t_{AA}	—	—	15	ns	

Write Mode

Item	Symbol	Min	Typ	Max	Unit	Test condition
Write pulse width	t_W	9	—	—	ns	$t_{WSA} = t_{WSA}$ min
Data setup time	t_{WSD}	3	—	—	ns	
Data hold	t_{WHD}	3	—	—	ns	
Address setup time	t_{WSA}	3	—	—	ns	$t_W = t_W$ min
Address hold time	t_{WHA}	3	—	—	ns	
Chip select setup time	t_{WSCS}	3	—	—	ns	
Chip select hold time	t_{WHCS}	3	—	—	ns	
Write disable time	t_{WS}	—	—	15	ns	
Write recovery time	t_{WR}	—	—	18	ns	

Rise/Fall Time

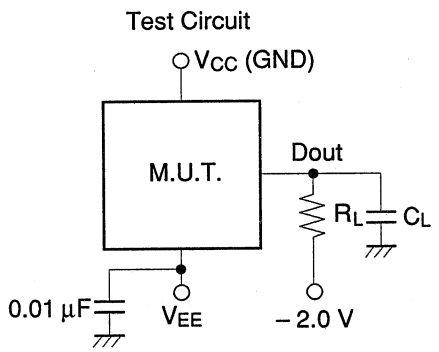
Item	Symbol	Min	Typ	Max	Unit	Test condition
Output rise time	t_r	—	1.5	—	ns	
Output fall time	t_f	—	1.5	—	ns	

Capacitance

Item	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance	Cin	—	3	—	pF	
Output capacitance	Cout	—	5	—	pF	

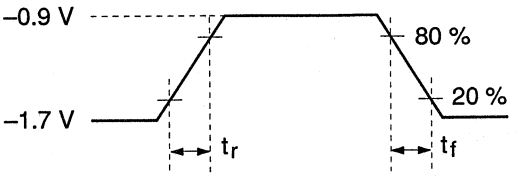
Test Circuit and Waveforms

Loading Condition



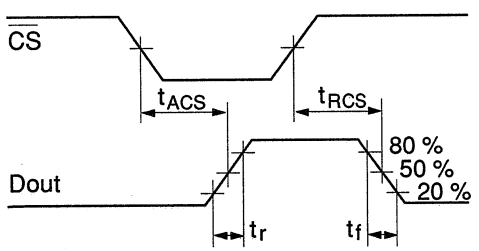
R_L = 50 Ω
C_L = 30 pF
(Includes probe and jig capacitance)

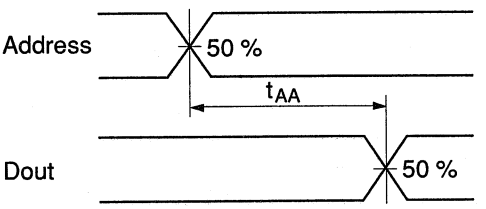
Input Pulse



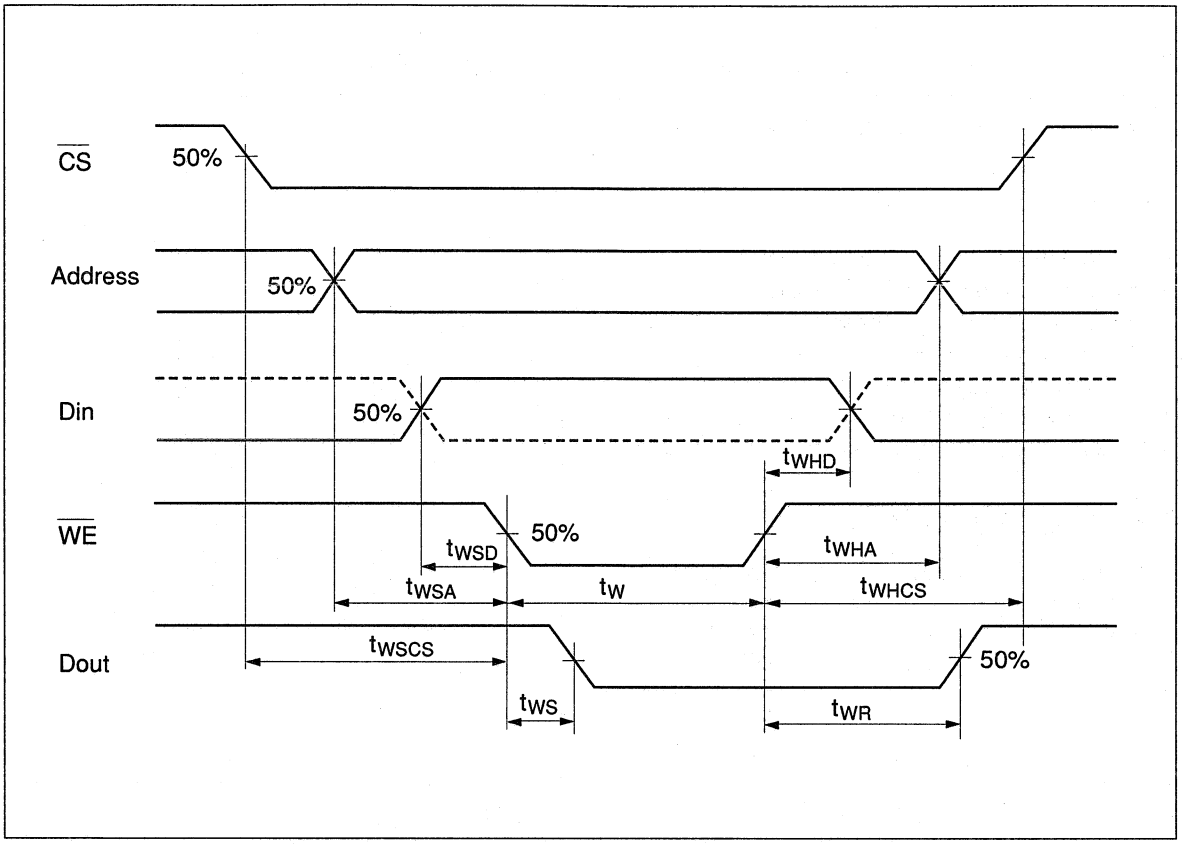
$t_r = t_f$ = 2.0 ns typ

Read Mode





Write Mode


CS
Address
Din
WE
Dout
50%
50%
50%
50%
50%
tWHD
tWSD
tWSA
tW
tWHA
tWHCS
tWSCS
tWS
tWR

HM101510 Series

1,048,576-word × 1-bit Random Access Memory

The Hitachi HM101510 is ECL 100 K compatible, 1,048,576 words by 1 bits read/write random access memory developed for high speed systems.

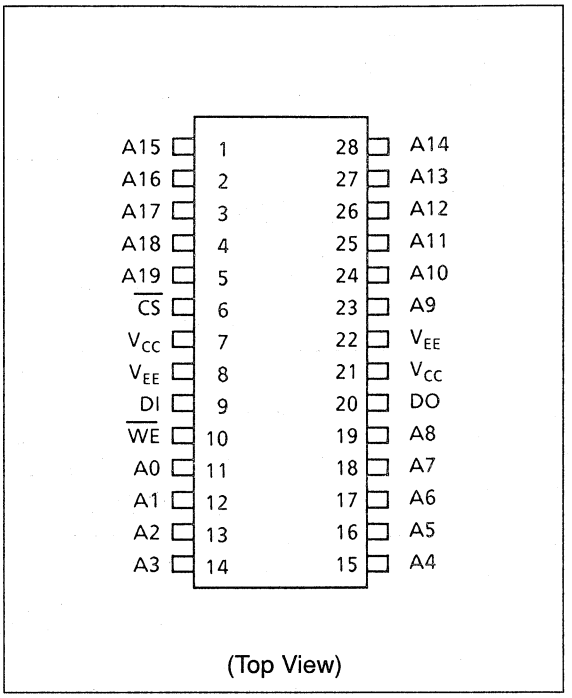
Features

- 1,048,576-words × 1 bit organization
- Fully compatible with 100 K ECL level
- 0.8 µm Hi-BiCMOS process
- Address access Time: 15 ns max
- Write pulse width: 9 ns min
- Low power dissipation: 700 mW typ
- Output obtainable by wired-OR (open emitter)

Ordering Information

Type No.	Access time	Package
HM101510F-15	15 ns	28 pin ceramic flat (30 mil lead pitch) (FG-28DB)

Pin Arrangement

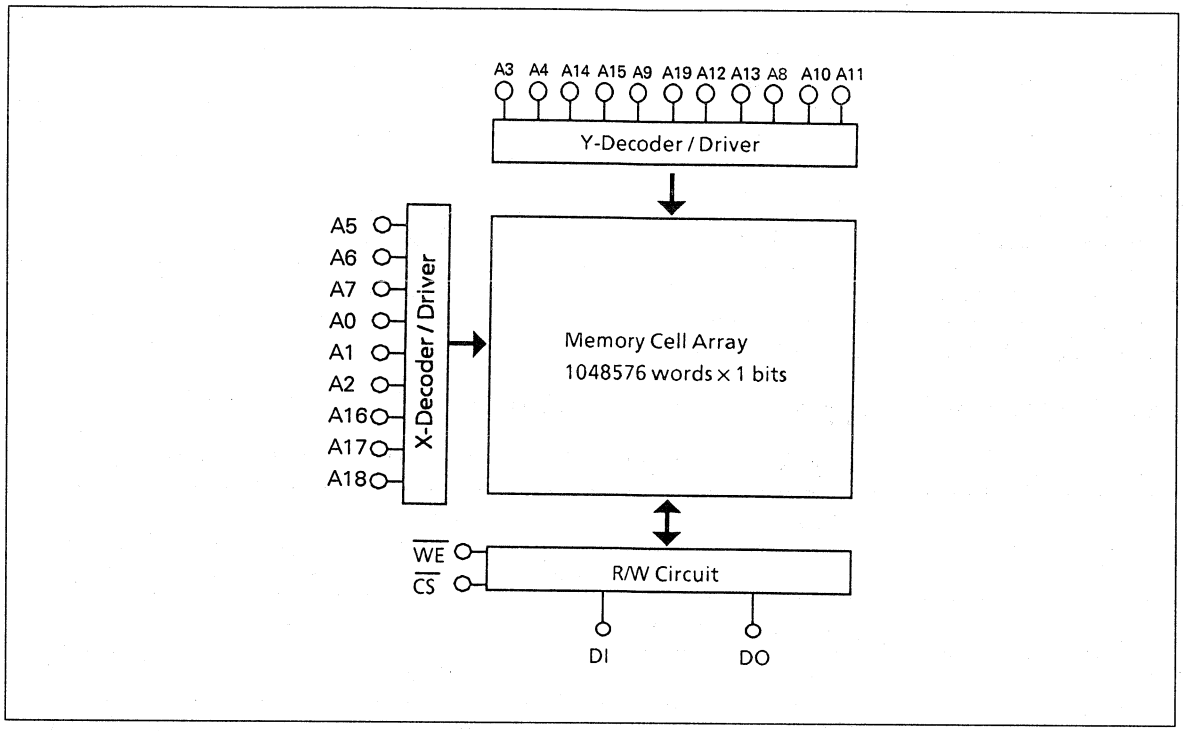


(Top View)

Pin Description

Pin name	Function
A0 – A19	Address input
DI	Data input
DO	Data output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Ground
V_{EE}	Supply voltage

Block Diagram



Function Table

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	X*1	X*1	L	Not selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X*1	Dout*2	Read

Notes: 1. Irrelevant
2. Read out noninvert

Absolute Maximum Rating (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply voltage	V_{EE} to V_{CC}	+0.5 to –7.0	V
Input voltage	Vin	+0.5 to V_{EE}	V
Output current	Iout	–30	mA
Storage temperature	Tstg	–65 to +150	°C
Storage temperature	Tstg (Bias)*1	–55 to +125	°C

Note: 1. Under bias (V_{EE} = –6.0 V min)

DC Characteristics (V_{EE} = –5.2 V, R_L = 50 Ω to –2.0 V, Tc = 0 to +75°C)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test condition
Output voltage	V_{OH}	–1025	–955	–880	mV	Vin = V_{IHA} or V_{ILB}
	V_{OL}	–1810	–1715	–1620	mV	
Output threshold voltage	V_{OHC}	–1035	—	—	mV	Vin = V_{IHB} or V_{ILA}
	V_{OLC}	—	—	–1610	mV	
Input voltage	V_{IH}	–1165	—	–880	mV	Guaranteed input voltage
	V_{IL}	–1810	—	–1475	mV	High/low for all input
Input current	I_{IH}	—	—	220	µA	Vin = V_{IHA}
	I_{IL}	0.5	—	170	µA	Vin = V_{ILB} $\overline{CS}$
		–50	—	—	µA	Others
Supply current	I_{EE}	–180	—	—	mA	All outputs open

AC Characteristics (V_{EE} = –5.2 V ± 5%, Tc = 0 to +75°C)

Read Mode

Item	Symbol	Min	Typ	Max	Unit	Test condition
Chip select access time	t_{ACS}	—	—	10	ns	
Chip select recovery time	t_{RCS}	—	—	10	ns	
Address access time	t_{AA}	—	—	15	ns	

Write Mode

Item	Symbol	Min	Typ	Max	Unit	Test condition
Write pulse width	t_W	9	—	—	ns	$t_{WSA} = t_{WSA}$ min
Data setup time	t_{WSD}	3	—	—	ns	
Data hold	t_{WHD}	3	—	—	ns	
Address setup time	t_{WSA}	3	—	—	ns	$t_W = t_W$ min
Address hold time	t_{WHA}	3	—	—	ns	
Chip select setup time	t_{WSCS}	3	—	—	ns	
Chip select hold time	t_{WHCS}	3	—	—	ns	
Write disable time	t_{WS}	—	—	15	ns	
Write recovery time	t_{WR}	—	—	18	ns	

Rise/Fall Time

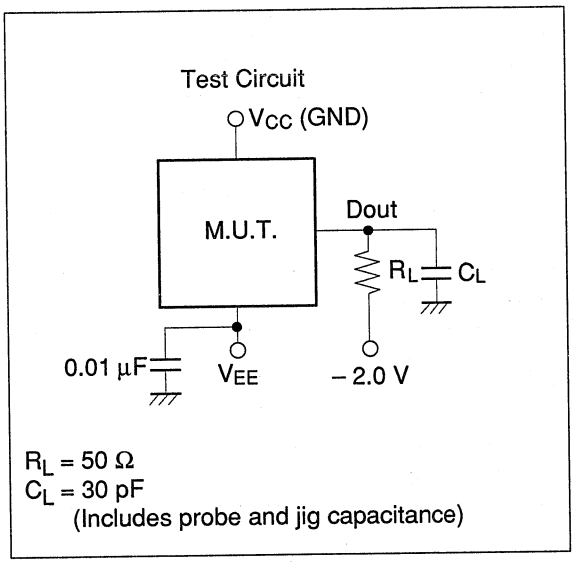
Item	Symbol	Min	Typ	Max	Unit	Test condition
Output rise time	t_r	—	1.5	—	ns	
Output fall time	t_f	—	1.5	—	ns	

Capacitance

Item	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance	Cin	—	3	—	pF	
Output capacitance	Cout	—	5	—	pF	

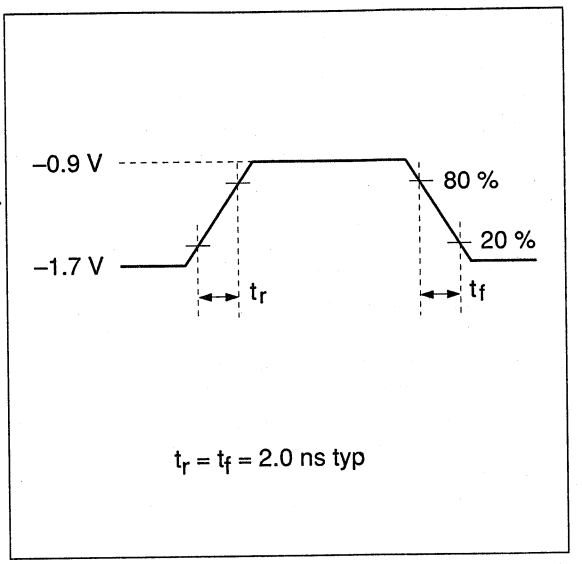
Test Circuit and Waveforms

Loading Condition



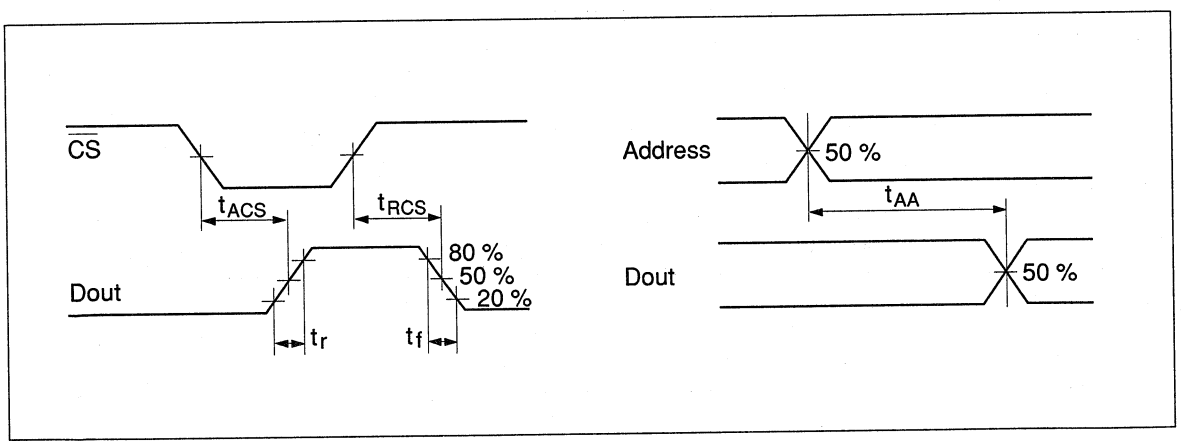
R_L = 50 Ω
C_L = 30 pF
(Includes probe and jig capacitance)

Input Pulse

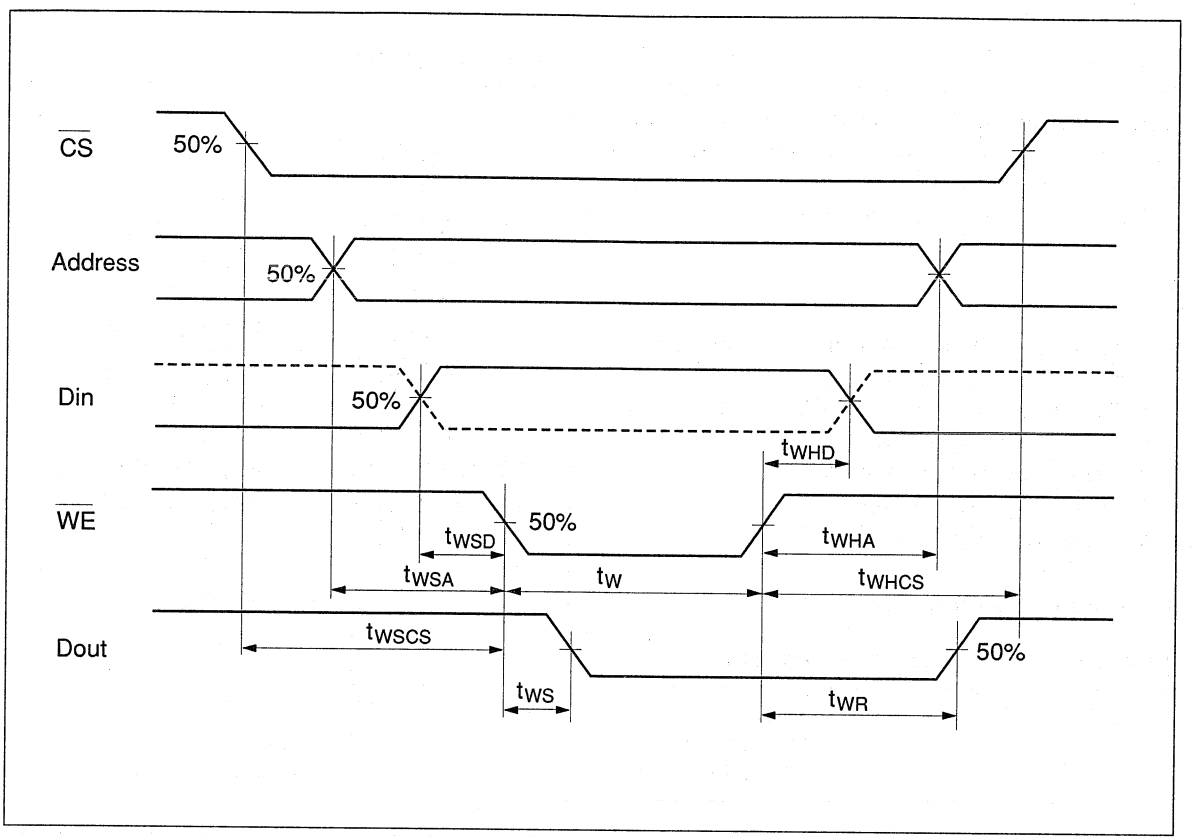


$t_r = t_f$ = 2.0 ns typ

Read Mode



Write Mode


CS
Address
Din
WE
Dout
50%
50%
50%
50%
tWHD
tWSD
tWSA
tW
tWHA
tWHCS
tWSCS
tWS
tWR

HM101513 Series

262,144-word × 4-bit / 524,288-word × 2-bit Random Access Memory

The Hitachi HM101513 is ECL 100 K compatible, reconfigarable 262,144 words by 4 bits or 524,288 words by 2 bits read/write random access memory developed for high speed systems. With the DI1/MODE pin held at V_{EE}, the organization becomes from 256 k × 4 to 512 k × 2.

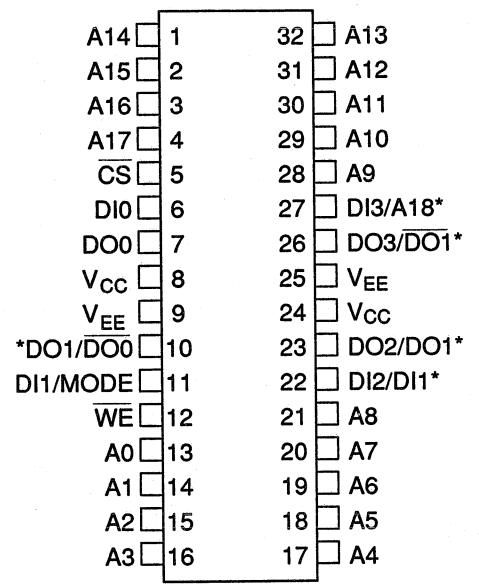
Features

- Reconfigaratible 262,144-words × 4 bit/524,288-words × 2 bit organization
- Fully compatible with 100 K ECL level
- 0.8 µm Hi-BiCMOS process
- Address access time: 15 ns max
- Write pulse width: 9 ns min
- Low power dissipation: 800 mW typ

Ordering Information

Type No.	Access time	Package
HM101513F-15	15 ns	32-pin ceramic flat (30 mil lead pitch)

Pin Arrangement



(Top View)

* : 256 k × 4/512 k × 2

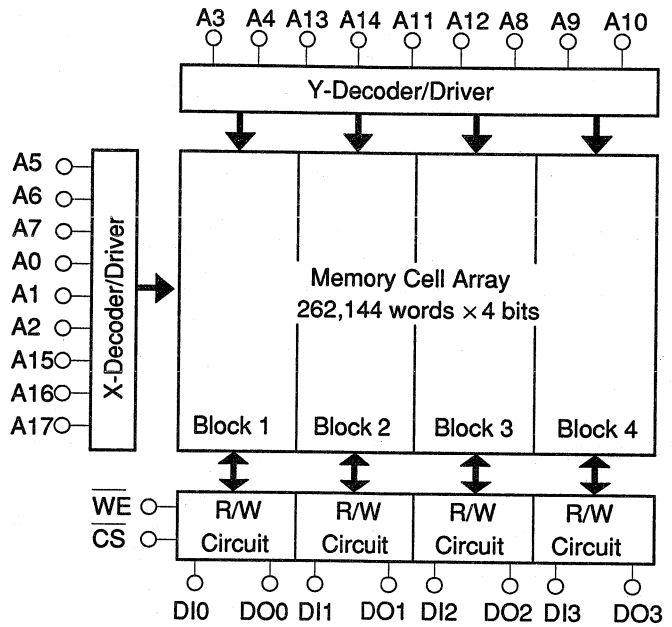
Pin Description

Pin name	Function
A0 – A18	Address input
DI0 – DI3	Data input
DO0 – DO3, $\overline{DO0}$ – $\overline{DO1}$	Data output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Ground
V_{EE}	Supply voltage
MODE	Mode select

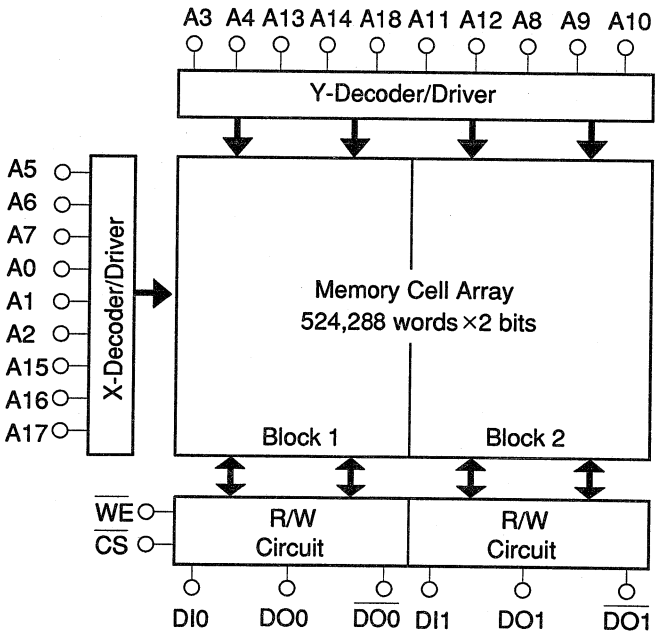
Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Block Diagram

• 256 k × 4 Organization



• 512 k × 2 Organization



Function Table

Input					
$\overline{CS}$	$\overline{WE}$	Din	Output	$\overline{Output}$	Mode
H	X*1	X*1	L	H	Not selected
L	L	L	L	H	Write "0"
L	L	H	L	H	Write "1"
L	H	X*1	Dout*2	$\overline{Dout}$*3	Read

Notes: 1. Irrelevant.
2. Read out noninvert.
3. Read out invert.

Absolute Maximum Rating (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply voltage	V_{EE} to V_{CC}	+0.5 to –7.0	V
Input voltage	Vin	+0.5 to V_{EE}	V
Output current	Iout	–30	mA
Storage temperature	Tstg	–65 to +150	°C
Storage temperature	Tstg (Bias)*1	–55 to +125	°C

Note: 1. Under bias (V_{EE} = –6.0 V min).

DC Characteristics (V_{EE} = –5.2 V, R_L = 50 Ω to –2.0 V, Tc = 0 to +75°C)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test condition	
Output voltage	V_{OH}	–1025	–955	–880	mV	Vin = V_{IHA} or V_{ILB}	
	V_{OL}	–1810	–1715	–1620	mV		
Output threshold voltage	V_{OHC}	–1035	—	—	mV	Vin = V_{IHB} or V_{ILA}	
	V_{OLC}	—	—	–1610	mV		
Input voltage	V_{IH}	–1165	—	–880	mV	Guaranteed input voltage High/low for all inputs	
	V_{IL}	–1810	—	–1475	mV		
Input current	I_{IH}	—	—	220	µA	Vin = V_{IHA}	
	I_{IL}	0.5	—	170	µA	Vin = V_{ILB}	$\overline{CS}$
		–50	—	—	µA		Others
Supply current	I_{EE}	–200	—	—	mA	All outputs open	

AC Characteristics (V_{EE} = –5.2 V ± 5%, Tc = 0 to +75°C)

Read Mode

Item	Symbol	Min	Typ	Max	Unit	Test condition
Chip select access time	t_{ACS}	—	—	10	ns	
Chip select recovery time	t_{RCS}	—	—	10	ns	
Address access time	t_{AA}	—	—	15	ns	

Write Mode

Item	Symbol	Min	Typ	Max	Unit	Test condition
Write pulse width	t_W	9	—	—	ns	$t_{WSA} = t_{WSA}$ min
Data setup time	t_{WSD}	3	—	—	ns	
Data hold	t_{WHD}	3	—	—	ns	
Address setup time	t_{WSA}	3	—	—	ns	$t_W = t_W$ min
Address hold time	t_{WHA}	3	—	—	ns	
Chip select setup time	t_{WSCS}	3	—	—	ns	
Chip select hold time	t_{WHCS}	3	—	—	ns	
Write disable time	t_{WS}	—	—	15	ns	
Write recovery time	t_{WR}	—	—	18	ns	

Rise/Fall Time

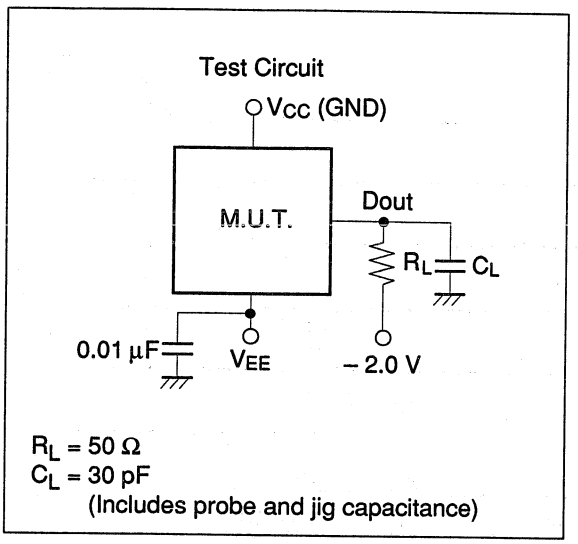
Item	Symbol	Min	Typ	Max	Unit	Test condition
Output rise time	t_r	—	1.5	—	ns	
Output fall time	t_f	—	1.5	—	ns	

Capacitance

Item	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance	Cin	—	3	—	pF	
Output capacitance	Cout	—	5	—	pF	

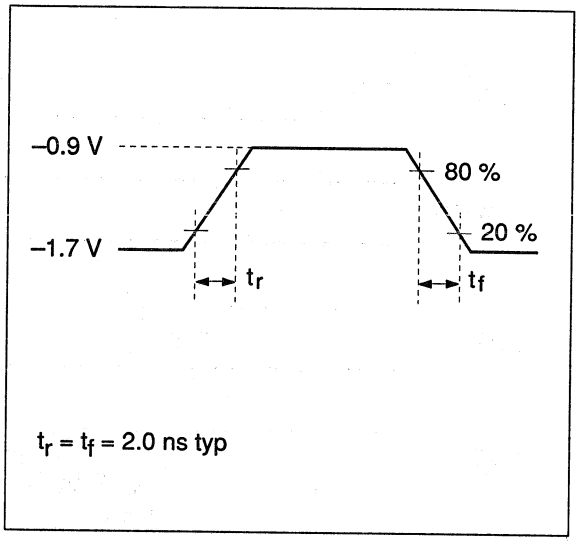
Test Circuit and Waveforms

Loading Condition



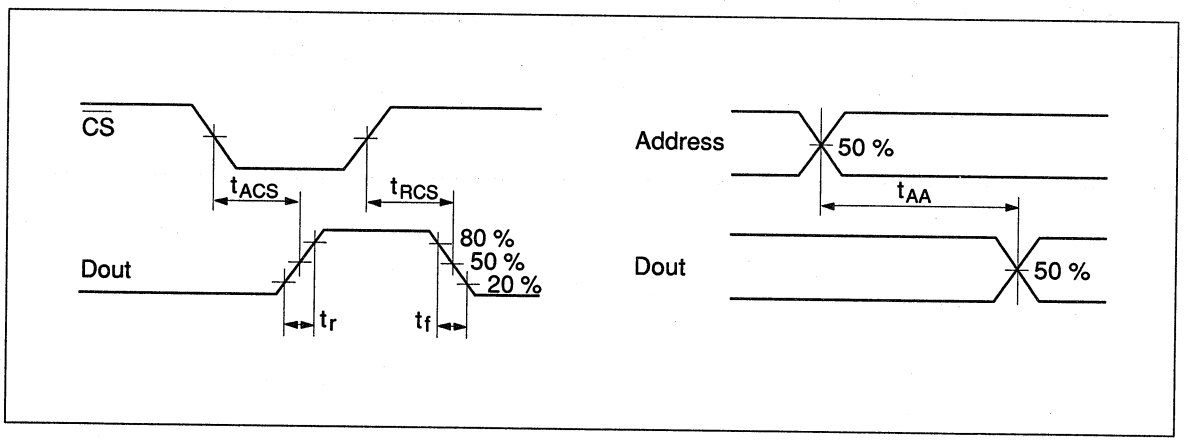
R_L = 50 Ω
C_L = 30 pF
(Includes probe and jig capacitance)

Input Pulse

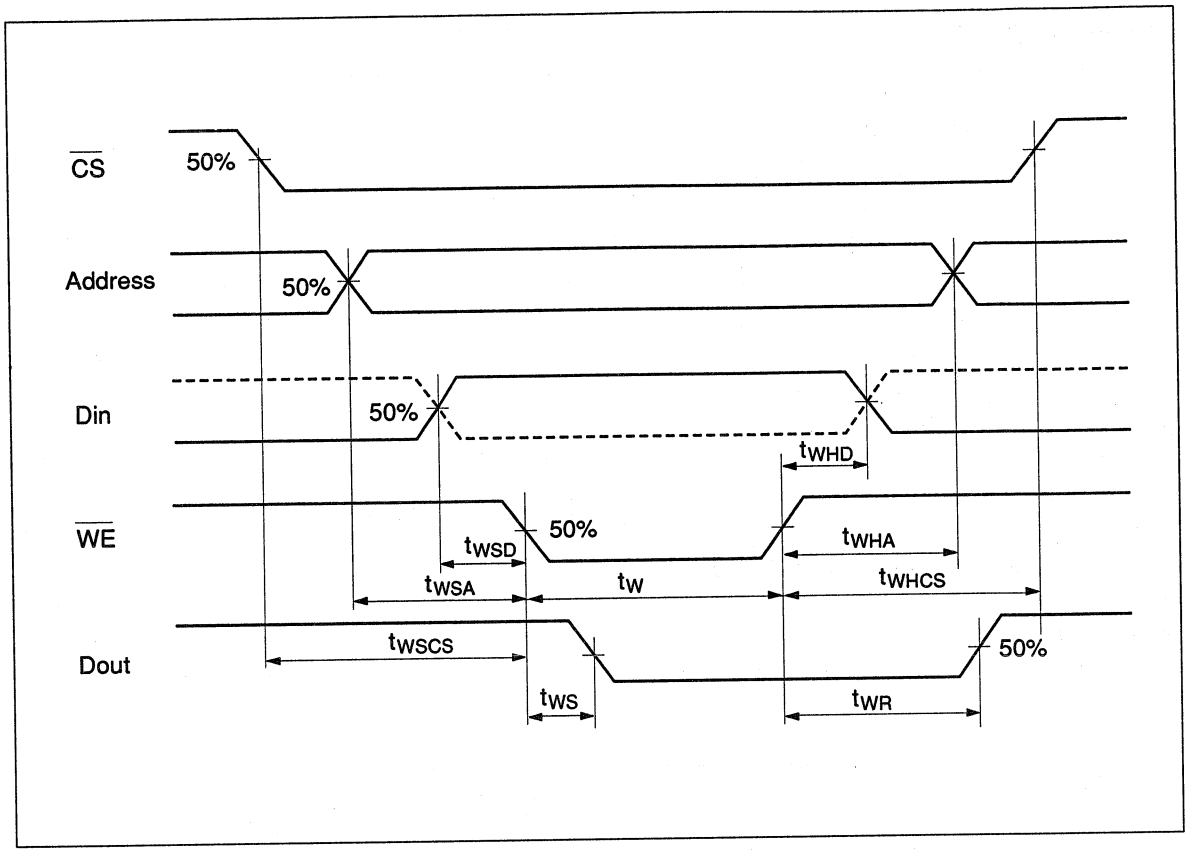


$t_r = t_f$ = 2.0 ns typ

Read Mode



Write Mode


CS
Address
Din
WE
Dout
50%
50%
50%
50%
50%
tWHD
tWSD
tWSA
tW
tWHA
tWHCS
tWSCS
tWS
tWR

HM101515 Series

262,144-words × 4-bits Fully Decoded Random Access Memory

Description

The HM101515 is ECL 100K compatible, 262,144-word by 4-bit read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

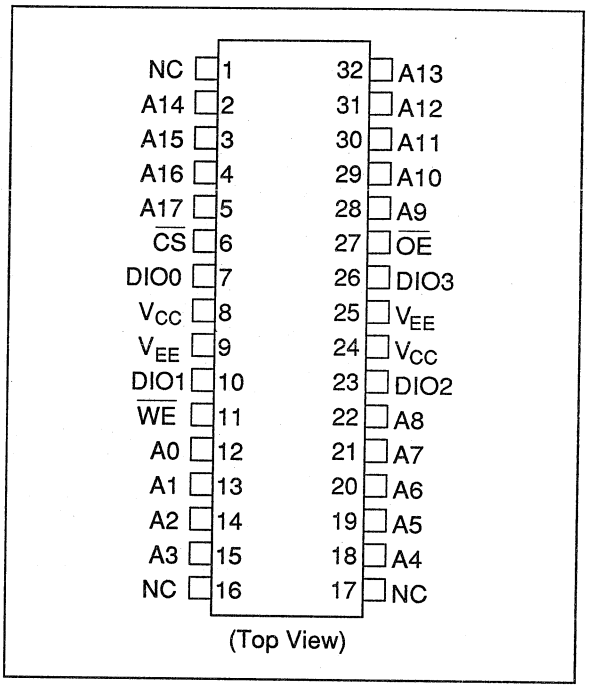
Features

- 262,144 × 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: 15 ns (max)
- Write pulse width: 9 ns
- Low power dissipation: 800 mW (typ)
- Common I/O

Ordering Information

Type No.	Access Time	Package
HM101515F-15	15 ns	32-pin ceramic flat (30-mil lead pitch) (FG-32D)

Pin Arrangement

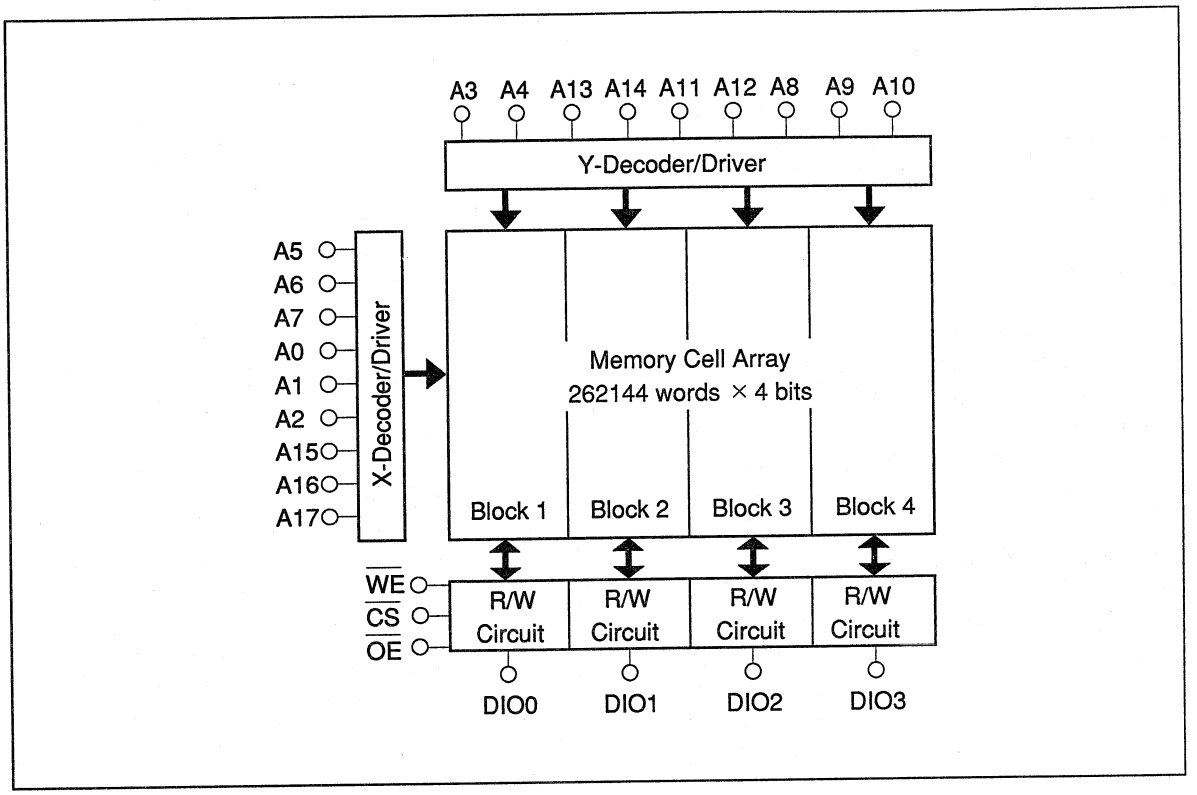


(Top View)

Pin Description

Pin Name	Function
A0–A17	Address input
DIO0–DIO3	Data input/output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
V_{CC}	Ground
V_{EE}	Supply voltage

Block Diagram



Function Table

Input			I/O		
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	DI	DO	Mode
H	x	x	x	L	Not selected
L	L	x	L	L	Write 0
L	L	x	H	L	Write 1
L	H	L	L	DI (Note)	Read
L	H	H	x	L	Output disable

x: Don't care

Note: Write data = Read data

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{EE} to V_{CC}	+0.5 to –7.0	V
Input voltage	Vin	+0.5 to V_{EE}	V
Output current	Iout	–30	mA
Storage temperature	Tstg	–65 to +150	°C
Storage temperature (bias)	Tstg (Bias) (Note)	–55 to +125	°C

Note: Under bias (V_{EE} = –6.0 V min.)

Electrical Characteristics

DC Characteristics (V_{EE} = –5.2 V, R_L = 50 Ω to –2.0 V, Tc = 0 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	
Output voltage	V_{OH}	–1025	–955	–880	mV	V_{in} = V_{IH}(max) or V_{IL}(min)	
	V_{OL}	–1810	–1715	–1620	mV		
Output threshold voltage	V_{OHC}	–1035	—	—	mV	V_{in} = V_{IH}(min) or V_{IL}(max)	
	V_{OLC}	—	—	–1610	mV		
Input voltage	V_{IH}	–1165	—	–880	mV	Guaranteed input voltage high/low for all inputs	
	V_{IL}	–1810	—	–1475	mV		
Input current	I_{IH}	—	—	220	µA	V_{in} = V_{IH}(max)	
	I_{IL}	0.5	—	170	µA	V_{in} = V_{IL}(min)	$\overline{CS}$, $\overline{OE}$
		–50	—	—	µA		Others
Supply current	I_{EE}	–200	—	—	mA	All outputs open	

AC Characteristics (V_{EE} = –5.2 V ± 5%, Tc = 0 to +75°C)

Read Mode

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Chip select access time	t_{ACS}	—	—	10	ns	
Chip select recovery time	t_{RCS}	—	—	10	ns	
Address access time	t_{AA}	—	—	15	ns	
Output enable access time	t_{AOE}	—	—	10	ns	
Output enable recovery time	t_{ROE}	—	—	10	ns	

Write Mode

Item	Symbol	Min	Typ	Max	Unit	Test condition
Write pulse width	t_W	9	—	—	ns	$t_{WSA} = t_{WSA}$ min
Data setup time	t_{WSD}	9	—	—	ns	
Data hold	t_{WHD}	3	—	—	ns	
Address setup time	t_{WSA}	3	—	—	ns	$t_W = t_W$ min
Address hold time	t_{WHA}	3	—	—	ns	
Chip select setup time	t_{WSCS}	3	—	—	ns	
Chip select hold time	t_{WHCS}	3	—	—	ns	
Write disable time	t_{WS}	—	—	15	ns	
Write recovery time	t_{WR}	—	—	18	ns	
Address setup time	t_{CSA}	3	—	—	ns	$\overline{CS}$ control
Address hold time	t_{CHA}	3	—	—	ns	$\overline{CS}$ control
Write pulse width	t_{CW}	9	—	—	ns	$\overline{CS}$ control

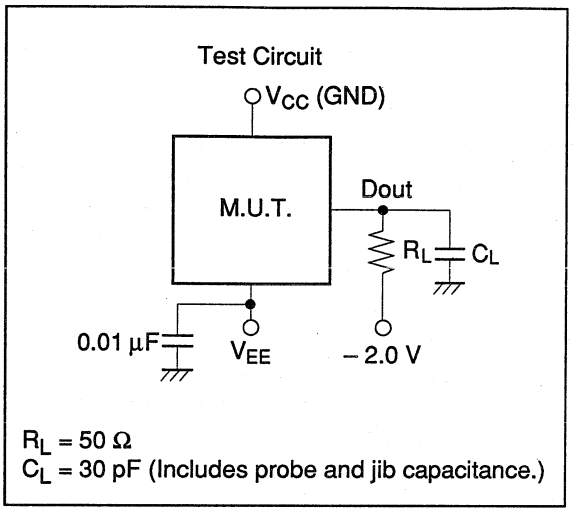
Rise/Fall Time

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Output rise time	t_r	—	1.5	—	ns	
Output fall time	t_f	—	1.5	—	ns	

Capacitance

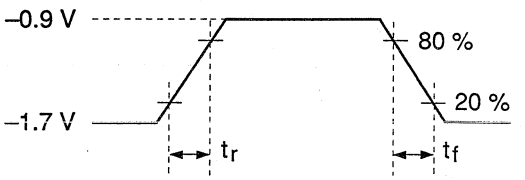
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Input capacitance	Cin	—	3	—	pF	
Output capacitance	Cout	—	5	—	pF	

AC Test Condition



R_L = 50 Ω
C_L = 30 pF (Includes probe and jib capacitance.)

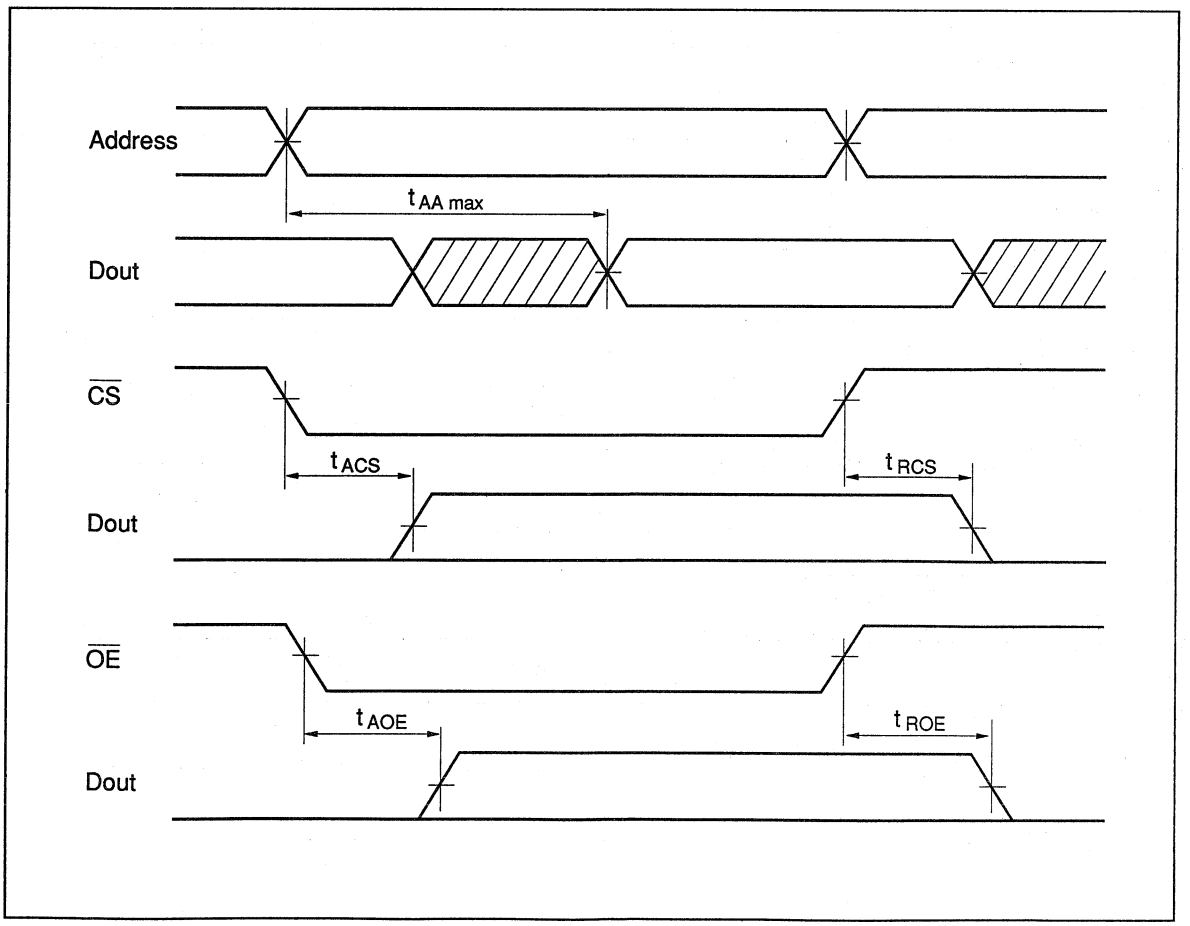
Input Pulse



tr = tf = 2.0 ns typ

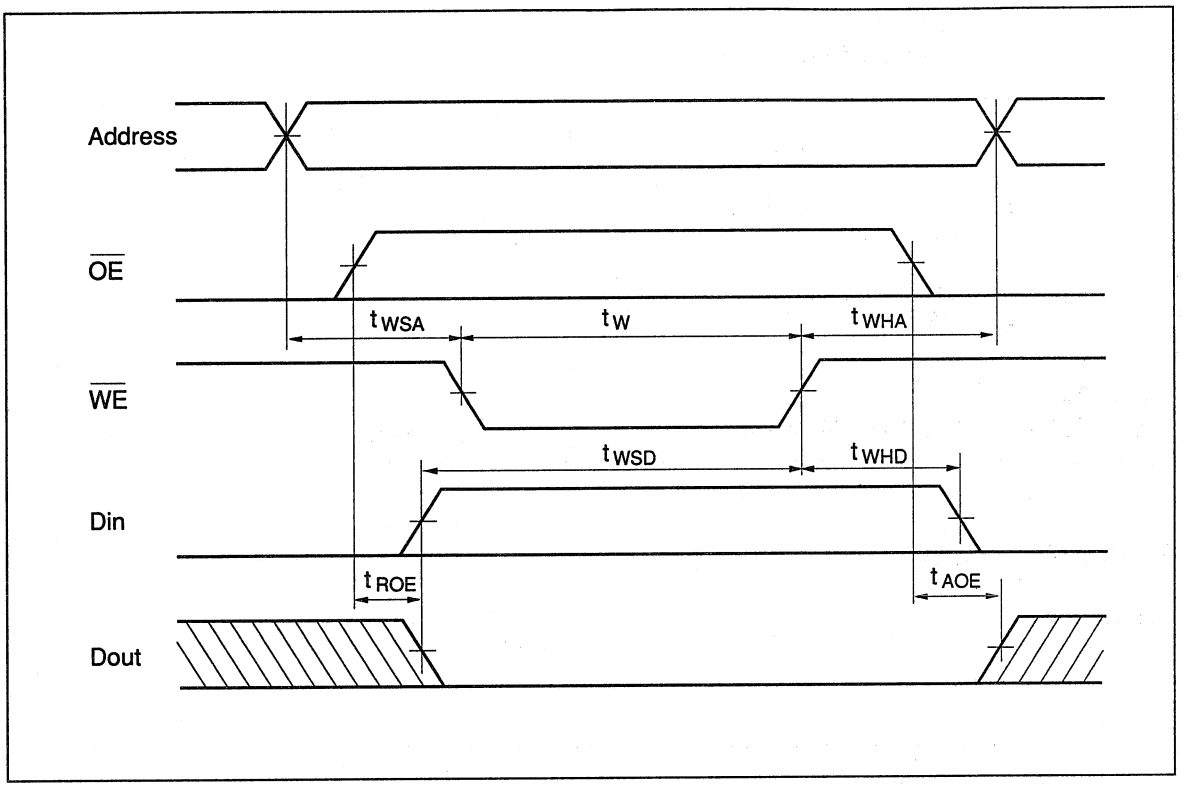
Timing Waveforms

Read Mode

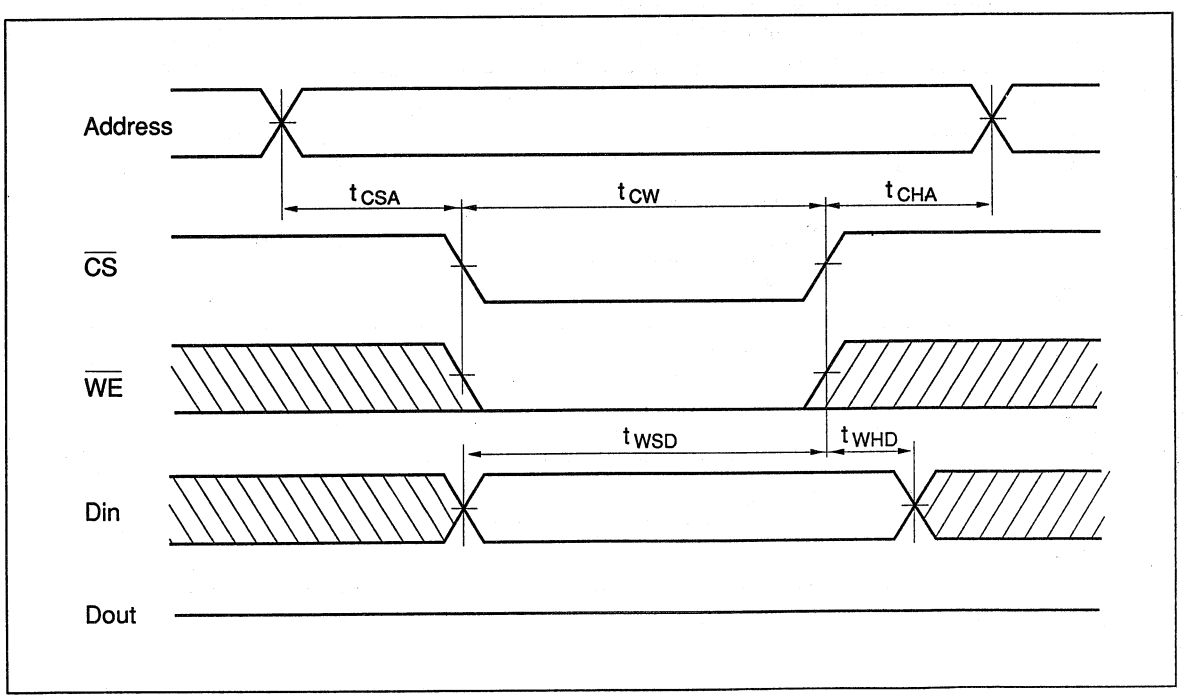


Write Mode

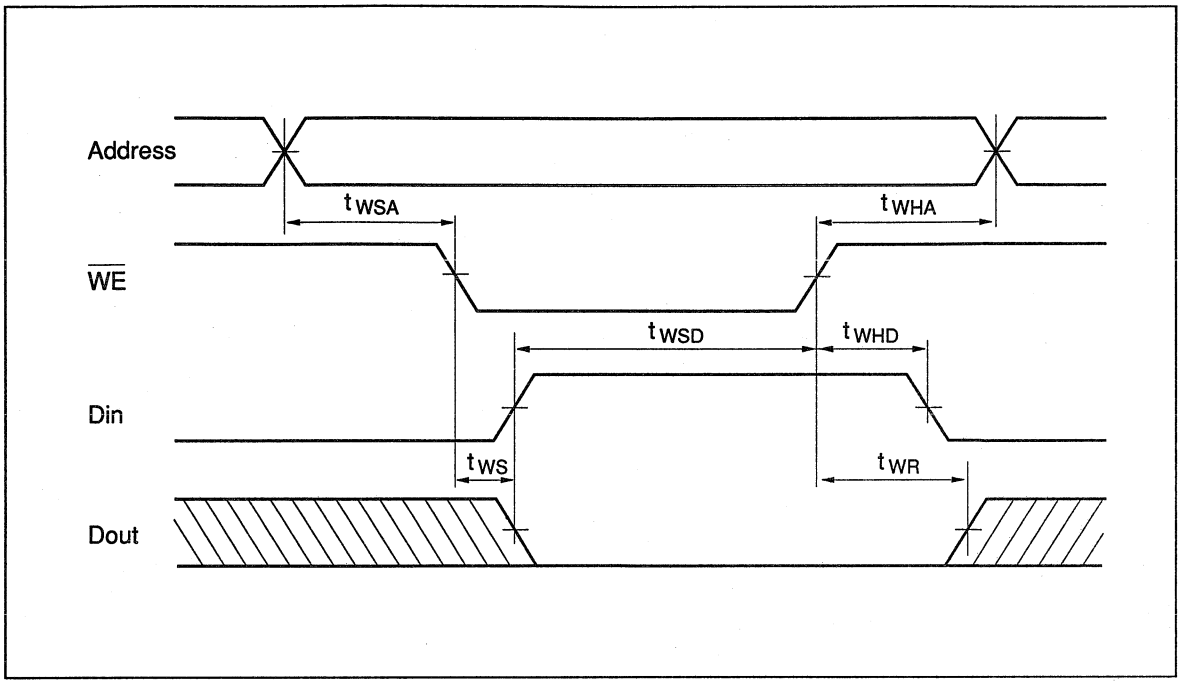
$\overline{OE}$ Control



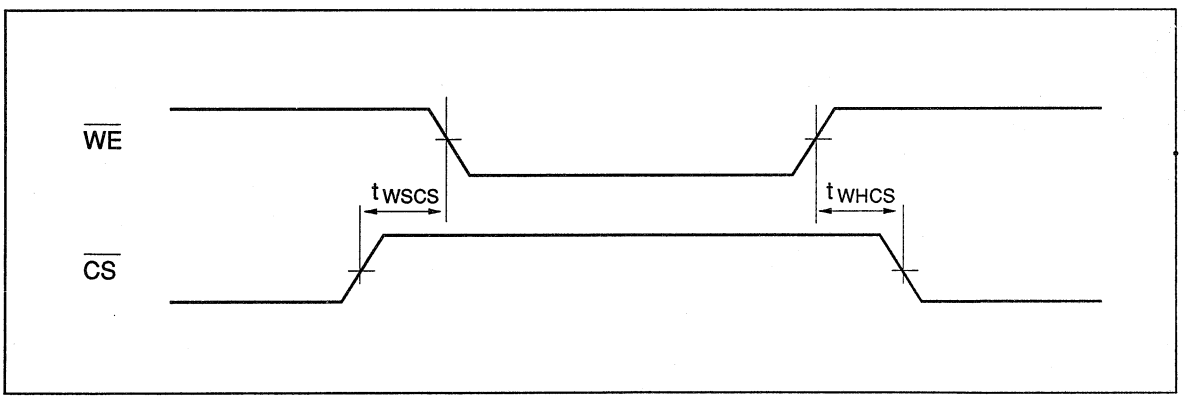
$\overline{CS}$ Control



$\overline{WE}$ Control



Write Disable Mode



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